

## Comparison of Sheet-Resistance Measurements Obtained By Standard and Small-Area Four-Point Probing

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### ABSTRACT

A modification of the standard four-point probing technique has been developed for measuring the sheet resistance of conducting films. Although the areas of unpatterned film that are required by the new modified technique are significantly less than those normally required with standard four-point probing, the values of sheet resistance provided by the two methods are found to match. The long term goal of this work is to improve the effectiveness of electrical critical-dimension (ECD) metrology in a special application, preferably without committing large surface areas of conducting film exclusively for the purpose of sheet-resistance measurement.<sup>1</sup>

### 1 INTRODUCTION

#### 1.1 Statement of Purpose

The specific purpose of this work is to investigate the use of a modified four-point probe technique for the extraction of sheet-resistance from film regions having significantly less area than those required for the practice of *standard* four-point probe methods. The motivation is to verify measurements of sheet resistance obtained from four-terminal sheet resistors in a special implementation in which the smaller film areas would have significant advantages. The end goal is to provide a means of verifying four-terminal sheet-resistor measurements made as part of a special ECD metrology application that enables counting lattice-plane fringes produced by high energy electron diffraction.

#### 1.2 Summary Technical Approach

The approach that has been adopted is to design, fabricate, and measure a test chip having four-terminal sheet resistors,<sup>1</sup> unpatterned film areas of lateral extent sufficient to permit sheet-resistance extraction by standard four-point probe methods,<sup>2</sup> as well as smaller unpatterned areas from which to determine sheet resistance by the new modified four-point probe

technique.

#### 1.3 Electrical Test Structure Metrology For Linewidth Reference Materials

ECD metrology generally does not provide absolute critical dimension (CD) measurements. However, its nanometer-level repeatability and very competitive cost make it well suited as a secondary reference in the linewidth certification of reference features. That is, ECD metrology has the potential to serve as a means of certifying physical CD standards, otherwise known as CD reference materials, if its traceability to absolute measurements can be established.

Fabricating CD reference materials by patterning the reference features in silicon-on-insulator (SOI) films having a (110) surface orientation is of special interest. A distinguishing and very advantageous property of this implementation is that the reference features are replicated with rectangular cross sections and with planar, atomically smooth, sidewalls.<sup>3</sup> The primary, absolute, reference-feature linewidth-certification method is High-Resolution Transmission-Electron Microscopy (HRTEM), which enables counting lattice-plane fringes produced by high energy electron diffraction.<sup>4</sup> Whereas this method is sufficiently accurate for all future road-map requirements, it is considered too costly for high-volume applications such as the certification of the reference materials for calibrating CD metrology instruments of all different types used by the integrated circuit manufacturing industry. What is needed is a secondary means of certification, which can be referenced to the HRTEM absolute measurements, and for which the nanometer-level repeatability of ECD metrology is well suited. The proposed certification strategy is to make ECD measurements of sets of reference features repeated at multiple die sites on an SOI wafer. HRTEM inspections of reference features at a limited number of die sites provide a sample of absolute measurements to correlate with the full-wafer population of ECD measurements. The degree of correlation between the sample and the

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ECD measurements facilitates an estimate of the errors in the linewidths of the electrically-tested reference features at all other die sites on the wafer. This makes possible their use as CD reference materials, at an acceptable cost.

#### 1.4 Complications in Measuring Sheet Resistance with Four-Terminal Sheet Resistors Patterned in (110) SOI Material

The general importance of sheet-resistance measurement in ECD metrology is that any error in the determination of sheet-resistance directly impacts the error of the accompanying electrical linewidth metrology. A 1% error in sheet resistance generates a 10-nm error in the corresponding electrical linewidth of a 1- $\mu\text{m}$  feature. Typically, four-terminal sheet resistors, such as those shown in Figure 1, are used to provide the measurements of local sheet resistance required for ECD determination.<sup>5</sup> One complication of patterning electrical test structures in (110) SOI material is the formation of (111)-plane facets between features of the four-terminal sheet resistors.<sup>6</sup> The non-planar current flow that the facets permit during  $\langle V/I \rangle$  measurements generates systematic errors in the extracted sheet-resistance values when the latter are estimated by available algorithms, which are developed exclusively for planar structures. In addition, in the SOI implementation, irregularities of the interface of the surface silicon to the oxide barrier below the facets may generate random errors in four-terminal sheet-resistor measurements.<sup>7</sup> Although methods to manage the facet-induced systematic errors are being developed,<sup>8</sup> it is considered prudent to verify four-terminal sheet-resistor measurements for the stated purpose with other known methods, such as four-point probing.

A potential advantage of four point probing is that it is entirely unaffected by the existence of the facets which form at acute inside corners in the intended

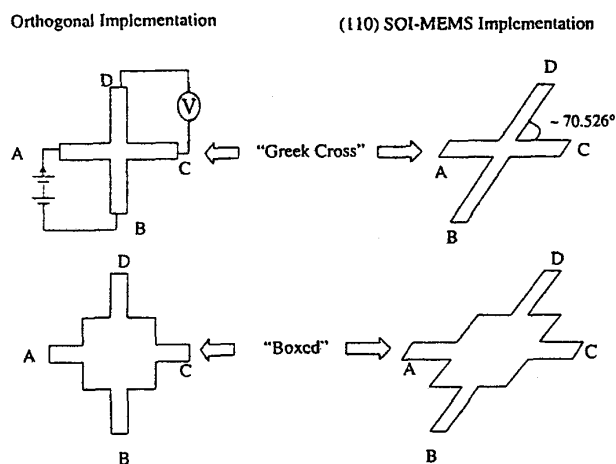


Figure 1. Typically, four-terminal sheet resistors are used to provide measurements of local sheet resistance required for ECD determination.

implementation. The new method, with its spatial resolution higher than that afforded by standard four-point probe metrology, could, of course, be useful in other applications featuring film materials, such as polysilicon or aluminum.

#### 1.5 Limitations of Standard Four-Point Probing for the Intended Application

Although standard four-point probe methods are well established, their usefulness in the intended ECD-metrology application has up to now been compromised by requirements for an unpatterned film area which is significantly greater than preferred. Standard four-point probe techniques typically require films extending for tens of millimeters. In the modification to four-point probing being disclosed here, sheet resistance is extracted from four-point probe arrays matching the dimensions of those used on standard  $2 \times n$  probe cards, namely 160  $\mu\text{m}$ . This offers the opportunity to measure local sheet resistance during ECD testing simply by dropping probe sets on patterned areas of lateral extent as small as several hundred micrometers.

## 2 IMPLEMENTATION OF THE MODIFIED TECHNIQUE

### 2.1 Current-Flow Modeling and $\langle V/I \rangle$ Simulation Results

The new modified technique provides sheet-resistance values by reconciling four-point-probe  $\langle V/I \rangle$  measurements made on finite areas of a film of unknown sheet resistance with the results of modeling the measurements with three-dimensional current-flow simulations. The high consumption of computer resources by current-flow modeling in three dimensions prevents its routine real-time use for the intended application. In addition, the complexities of setup and computation require highly-specialized skills. However, in principle, once computations for a selected set of cases have been performed, the results can be saved and reconciled with four-point probe measurements made on various films to provide their unknown sheet resistance.

This brings up the question of just what the probe-location/film-boundary configuration might be for the referenced set of cases selected for current-flow modeling and  $\langle V/I \rangle$  simulation. In this context, the probe-location/film-boundary configuration means a set of dimensional parameters that uniquely specifies the boundaries of the film, the four probe-point locations relative to the boundary, and the film thickness. Clearly, there is an infinite number of possibilities. However, for the purpose of this preliminary investigation, we have chosen, for reasons related to test-feature orientation in the (110) SOI implementation, to "standardize"  $\langle V/I \rangle$  measurements with a square array of four probes centrally located in parallelogram-shaped

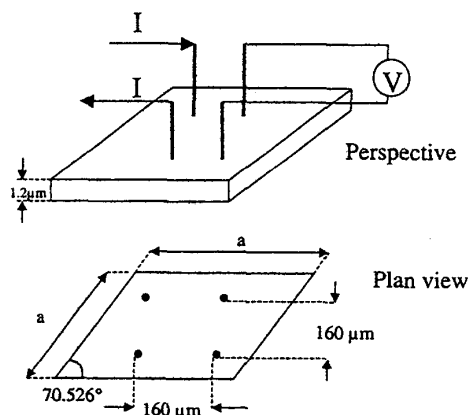


Figure 2. A square array of four probes is centrally located in parallelogram-shaped areas which are patterned in the surface film.

areas which are patterned in the surface film and have lateral dimensions larger than, but of the order of, the probe separation, as illustrated in Figure 2.

The shape of the parallelograms is dictated by the silicon-lattice crystallography.<sup>9</sup> Their sizes are selected according to the series:  $(1/a)$ ,  $(1/a)^{1/2}$ ,  $(1/a)^{1/4}$ ,  $(1/a)^{1/8}$ ,  $(1/a)^{1/16}$  with base-side  $a$  equal to  $0.004541 \mu^{-1}$ , that is, (251.57; 474.30; 697.03; 919.77; 1142.50)  $\mu\text{m}$ . The probe separation is selected to be  $160 \mu\text{m}$ . This value corresponds to the spacing of probe tips of a NIST-standard  $2 \times n$  probe card widely used in ECD metrology. The value of the material resistivity,  $\rho$ , was selected to be  $1000 \Omega\text{-cm}$ . The film thickness used in the current-flow simulations is  $1.2 \mu\text{m}$ . Selecting this particular probe-location/film-boundary configuration and material resistivity is quite arbitrary; however, the dimensions happen to conform closely with one intended design specification of the test chip.

The current flow modeling to simulate the  $\langle V/I \rangle$  measurements is procedurally similar to that used previously for simulating the extraction of sheet resistance from four-terminal sheet resistors<sup>8</sup>. In this case, a virtual current,  $I$ , is forced with uniform density

Table 1. Results for  $\langle V/I \rangle$  obtained from current-flow modeling.

Size (mm)	$V_1/I_1$ (ohms)	$V_3/I_3$ (ohms)
251.577	0.1732293	0.1845667
474.308	0.1356207	0.1389050
697.039	0.1152216	0.1167120
919.770	0.1054254	0.1070281
1142.502	0.1011013	0.1012068

between two probe tips at the adjacent corners of the 4-point probe array, as shown in Figure 3. The potential,  $V$ , induced across the other two probes is calculated from three-dimensional current-flow modeling. Because of rotational symmetry,  $V_1$  and  $V_2$  in Figure 3 are equal, and likewise are  $V_2$  and  $V_4$ . Thus, modeling needs only to be conducted for voltages  $V_1$  and  $V_3$ . Results of the  $\langle V/I \rangle$  simulations obtained from the current-flow modeling are shown in Table 1.

## 2.2 Scope of an Illustrative Special Case of Determining Unknown Sheet Resistance from $\langle V/I \rangle$ Measurements

In special cases, one of which is illustrated here, the determination of the unknown sheet resistance from  $\langle V/I \rangle$  measurements is facilitated through two fundamental relationships. The first relationship is that, if all dimensions of the probe-location/film-boundary configuration remain the same, each  $\langle V/I \rangle$  value varies

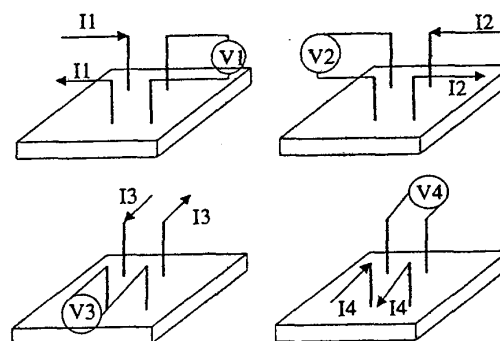


Figure 3. A virtual current,  $I$ , is forced with uniform density between two probe tips at the adjacent corners of the 4-point probe array, and the potential,  $V$ , induced across the other two probes is calculated from three-dimensional current-flow modeling.

directly as the resistivity of the film material. The second relationship is that, as all dimensions are scaled, resistivity remaining constant, any  $\langle V/I \rangle$  measurement varies inversely with the scaling. In order to take advantage of the second relationship, it is necessary that the probe-location/film-boundary configuration used for the measurements is a scaling of the simulated one.

## 2.3 Reconciliation of $\langle V/I \rangle$ Measurements and Simulation Results in the Illustrative Special Case

Ideally, if the conditions of the special case are observed, unknown material resistivity and, consequently, film sheet resistance should be

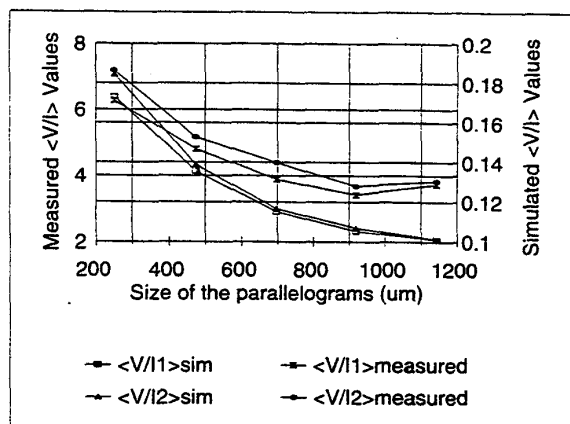


Figure 4. Comparison of measurement and simulation of the corresponding  $\langle V/I \rangle_m$  and  $\langle V/I \rangle_s$ .

determinable from the ratio of the measurement of any single  $\langle V/I \rangle$  value made on any of the available parallelograms and the corresponding simulated value. However, experience suggests that matching the simulated and measured values simultaneously for all five parallelograms, and four  $\langle V/I \rangle$  values for each, would be statistically prudent. Accordingly, for the purposes of the special case, unknown resistivity, from which sheet resistance is readily obtained, is achieved by selecting the value of  $\rho_m$ , which minimizes the quantity  $Q$ , given by

$$Q = \sum_{i=1}^4 \sum_{j=1}^5 \left( \langle V/I \rangle_{m,i,j} - \frac{\rho_m}{\rho_s} \cdot \frac{h_s}{h_m} \cdot \langle V/I \rangle_{s,i,j} \right)^2 \quad (1)$$

In Eq. (1),  $\langle V/I \rangle_{m,i,j}$  is the value of  $\langle V/I \rangle_i$  as measured on parallelogram  $j$ , where  $j$  ranges, in this case, from 1 to 5. Correspondingly,  $\langle V/I \rangle_{s,i,j}$  is the value of  $\langle V/I \rangle_i$  as simulated for parallelogram  $j$ . The quantities  $h_m$  and  $h_s$  are the thicknesses of the measured and simulated films, respectively. The respective material resistivities are  $\rho_m$  and  $\rho_s$ . We have already stated that  $\rho_s$  and  $h_s$  were arbitrarily selected to be 1000  $\Omega\text{-cm}$  and 1.2  $\mu\text{m}$  respectively and that  $\langle V/I \rangle_{s,1,j} = \langle V/I \rangle_{s,2,j}$  and

Table 2.  $\langle V/I \rangle$  measurement results.

Size (mm)	$V_1/I_1$ (ohms)	$V_2/I_2$ (ohms)	Average of $V_1/I_1$ & $V_2/I_2$	$V_3/I_3$ (ohms)	$V_4/I_4$ (ohms)	Average of $V_3/I_3$ & $V_4/I_4$
11.29	6.262	6.289	6.276	7.145	7.225	7.185
21.33	4.829	4.780	4.804	5.185	5.151	5.168
31.66	3.827	3.944	3.886	4.294	4.490	4.392
41.35	3.461	3.397	3.429	3.714	3.652	3.683
51.39	3.443	3.620	3.740	4.019	3.984	3.840

$\langle V/I \rangle_{s,3,j} = \langle V/I \rangle_{s,4,j}$ . The objective is now to determine  $\rho_m$  from Eq. (1).

In order to make a preliminary evaluation of the new modified sheet-resistance extraction technique,  $\langle V/I \rangle$  measurements were made on parallelogram-shaped structures with the appropriate aspect ratios patterned in silicon wafers having a thickness of 54.0  $\mu\text{m}$ . The scaling factor for a film of thickness 1.2  $\mu\text{m}$ , which was used for the simulations, is 45.0. In order to maintain the proportions of the modeled probe-location/film-boundary configuration the parallelograms were sized accordingly at (11.3; 21.3; 31.4; 41.4; 51.4) mm and the probes were located at the corners of a centrally-located square having a side of 7.2 mm. The measurement results are listed in Table 2. Through minimization of the quantity  $Q$  in Eq. (1), the sheet resistance of the wafers is found to be 30.41  $\Omega/\square$ . This value is close to the value of 29.95  $\Omega/\square$  obtained by making a standard four-point probe sheet-resistance measurement on the largest parallelogram. Scaling the simulated  $V/I$  values to the estimated resistivity of 30.41  $\Omega/\square$  enables the direct comparison of measurement and simulation of the corresponding  $\langle V/I \rangle_m$  and  $\langle V/I \rangle_s$ , as shown in Figure 4.

### 3 SUMMARY

The specific purpose of this work is to investigate the use of a modified four-point probe technique for the extraction of sheet-resistance from film regions having significantly less area than those required for the practice of standard four-point probe methods. The end goal is to provide a means of verifying four-terminal sheet-resistor measurements to improve the effectiveness of a special ECD metrology application. The approach that has been adopted is to design, fabricate, and measure a test chip having four-terminal sheet resistors, unpatterned film areas of lateral extent sufficient to permit sheet-resistance extraction by standard four-point probe methods, as well as smaller unpatterned areas from which to extract sheet resistance by the new modified four-point probe technique. The general importance of sheet-resistance measurement in ECD metrology is that any error in the determination of sheet-resistance generates comparable errors in the accompanying electrical linewidth metrology. The new modified technique provides sheet-resistance values by reconciling four-point probe  $\langle V/I \rangle$  measurements made on finite areas of a film of unknown sheet resistance with the results of modeling the measurements with three-dimensional current-flow simulations. Once computations for a selected set of cases have been performed, the results can be saved and reconciled with four-point probe measurements

made on various films to provide their unknown sheet resistance. A special case has been examined in which the sheet resistance of silicon films was determined to be  $30.41 \Omega/\square$  through application of the new modified technique. This value is close to that of  $29.95 \Omega/\square$  that was obtained from a standard four-point probe measurement on a larger area of material.

Of course, for a given film, the  $\langle V/I \rangle$  measurements do, in general, vary in a complex manner with the unpatterned film's boundaries and thickness, even when the probes' locations remain fixed. The variation with a film's boundaries is accentuated as the probe-array footprint increases and approaches the boundaries of the patterned film. The modified four-point probe metrology being reported here takes advantage of an exact knowledge of this behavior, but only, at this time, for scaled versions of the particular probe-location/film-boundary configuration which has been specified above. The need to know film thickness beforehand is more of a temporary inconvenience than a fundamental requirement. Clearly, more extensive current-flow modeling could provide values of  $\langle V/I \rangle_1$  and  $\langle V/I \rangle_2$  for a particular probe-array geometry as a function of both film boundary and thickness independently. One could then establish functional representations to accommodate film thickness as an independently variable quantity. The reconciliation could then be performed for cases in which only the film boundary and probe-array geometry would need to be scaled together. In fact, the measurement-simulation reconciliation would then be able to provide a separate estimate of the film thickness as well as material resistivity. However, evaluating these more general cases will consume further effort and will be reported on in the future.

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