Anomalous behavior of a quantized Hall plateau in a high-mobility Si metal-oxide-semiconductor field-effect transistor

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Measurements at 14 T and 340 mK of the quantized Hall resistance of the i = 4 plateau of a Si metal-oxide-semiconductor field-effect transistor (Si-MOSFET) made with a precision of 0.005 ppm and an accuracy of 0.015 ppm revealed unexpected irregularities. Smooth variations of ± 0.04 ppm were observed across the plateau even though the Si-MOSFET had a mobility of 1.2 m²/V s and a diagonal resistivity less than 0.002 ppm of the plateau resistivity. Furthermore, measurements over a period of several months indicated that the plateau shape is metastable. A variety of possible causes for these phenomena are discussed, but none provides a satisfactory explanation.

I. INTRODUCTION

The international practical electrical unit of resistance is now officially¹ based on the quantized Hall resistance of a two-dimensional electron gas at low temperatures and high magnetic fields in certain high-quality semiconductor interfaces.² The measured Hall resistance R_H has been shown to obey the formula

$$R_H = h/ie^2 \tag{1}$$

to a very high accuracy. Here h is Planck's constant, e is the electronic charge, and i is an integer. The quantized Hall effect has been extensively studied³ and it is known that, in contrast to the case of the Josephson effect, significant material-, size-, current-, and temperaturedependent corrections to Eq. (1) have been observed in many samples. In fact, until recently the question of whether Si metal-oxide-semiconductor field-effect transistor (Si-MOSFET) samples and GaAs/Al-Ga-As heterostructures yield the same value at accuracies exceeding 0.1 ppm had been an open question. Bliek et al.⁴ had reported agreement at the 0.03-ppm level of accuracy, while Kawaji et al.5,6 had found apparent discrepancies of up to 0.16 ppm, even when all known effects were accounted for. Delahaye and Bournaud⁷ reported agreement at the 0.01-ppm level of accuracy between four GaAs/Al-Ga-As heterostructures and a Si-MOSFET sample made by Kawaji. Hartland et al.⁸ have since made measurements nearly two orders of magnitude more accurate than Bliek and found complete agreement at the 3.5×10^{-10} parts level between two GaAs/Al-Ga-As heterostructures and a Si-MOSFET fabricated at the University of Southampton.

In this paper, we report measurements which indicate there are still unexplained aspects of the quantum Hall effect that can cause deviations of up to 0.4 ppm from the ideal behavior. We made high-accuracy measurements of the i = 4 plateau of a small, high-mobility Si-MOSFET utilizing the same apparatus which measures the Hall plateaus of a GaAs/Al-Ga-As heterostructure to maintain the U.S. national unit of electrical resistance. Even though the mobility of the sample exceeded 1 m²/V s and its diagonal resistivity was less than 0.002 ppm of the plateau value, the measured plateau was not flat, but smoothly varied ± 0.04 ppm around the theoretical value. Over a period of several months, the observed variations changed their character. In addition, if the apparatus was not protected during thunderstorm-induced electrical power disturbances, the entire plateau could shift to *higher* resistance by as much as 0.4 ppm in a metastable manner which required warming of the sample to bring it back to its original state of much smaller, reproducible variations.

In this paper, Secs. II, III, and IV describes the samples and measurement apparatus, Sec. V describes our results, and Secs. VI and VII give our analysis and conclusion.

II. SAMPLES AND GATE SUPPLY

A. Si-MOSFET

The silicon MOSFET sample, identified as 72-17H53-NB1, was obtained from S. Kawaji, Gakushuin University, Tokyo. Details of the fabrication technique have been described by Yagi,⁹ and will only be outlined here. The MOSFET was fabricated on a (100) plane of *p*-type silicon doped with $\approx 2 \times 10^{20}$ boron atoms/m³. To reduce leakage current from outside the gate area, a heavily boron-doped region (channel stop) was formed around the gate area by an ion implantation dose of 5×10^{18} boron atoms/m². Figure 1 shows a scale drawing of the top view of the chip containing the sample while Fig. 2 shows a cross-sectional schematic view of the silicon MOSFET. The 1.91 × 1.91 mm² silicon chip was mounted on a 12-pin, TO-8 header.

The zero-field mobility at 4 K as a function of gate voltage for our sample was very similar to that of an identically fabricated sample studied by Yoshihiro *et al.*¹⁵ At the 14-V gate voltage of the i = 4 plateau, the sample mobility reached a maximum of 1.2 m²/V s.

The contact resistances of this sample, measured at 14 T and 350 mK for $V_g = 14.4$ V using a four-terminal tech-

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FIG. 1. Top view of the Si-MOSFET chip showing the connections to the measured device.

nique for the current contacts and a three-terminal technique for the voltage contacts, are listed in Table I. The disparity between the contact resistance of the voltage and current contacts primarily reflects their difference in width. Also, for the voltage leads, the measurement necessarily included a small contribution from the side channel resistances.¹⁰ Consequently, the values given in Table I are upper limits to the true contact resistances of the voltage contacts.

B. Si-MOSFET gate supply

The semiautomated gate supply for the Si-MOSFET was built with 3 ppm/day stability and $10^{14} \Omega$ isolation from ground. Since the gate voltage is referenced to the



FIG. 2. Section view of the Si-MOSFET detailing contact and gate structure. Dimensions are not to scale. TABLE I. Contact resistances for the Si-MOSFET sample at 14 T and 350 mK. The contact locations are shown in Fig. 1.

Contact	Contact resistance (Ω)		
Drain	0.072		
<i>P</i> 1	15.1		
P2	15.1		
P3	14.2		
P4	13.5		
P5	13.9		
P6	13.2		
Source	0.076		

device source, the sample carrier density is actually determined by a combination of the applied gate voltage and the sample Hall voltage (which changes sign with the current). Consequently, a built-in offset adjustment which switches with current direction was included to compensate for this small ($\approx 0.4\%$) effect.

The gate supply was built using Hg batteries, an isolation amplifier, double-shielding, BPO (British Post Office) output connectors, and a fiber-optic control link. All critical subassemblies were mounted using Teflon supports. A schematic diagram is given in Fig. 3.

Output stability was assured by the use of a series connection of four PMI REF01 regulators, each driven by a 12.6-V Hg battery. The extreme isolation was attained while still allowing automatic control of the offset adjustment and simultaneously monitoring the output. A fiber-optic link was used for the offset control and a Burr-Brown ISO-106B isolation amplifier connected to the monitor circuit.

One concern during Si-MOSFET measurements is that there might be a leakage current through the sample from the gate voltage. To first order, such an effect would be discriminated against by the reversal of the sample current. If the supplied gate voltage is maintained constant, however, the actual potential that controls the electron concentration will have a component synchronous with the current. A leakage current from the gate to the drain of 1 pA will lead to an error of no more than 0.0008 ppm. At our nominal gate voltage of 15 V, this corresponds to a leakage resistance of $1.5 \times 10^{13} \Omega$. We directly measured all of our interwire leakage resistances at room temperature and found them to be greater than $10^{14} \Omega$. They are higher at low temperatures.

C. GaAs/Al-Ga-As heterostructure

The GaAs/Al-Ga-As heterostructure sample has been used for the maintenance of the U.S. national unit of electrical resistance. It was grown by Art Gossard at Bell Labs and configured by Dan Tsui at Princeton University. The GaAs/Al_xGa_{1-x}As sample was grown by molecular-beam epitaxy with x = 0.29. It was optimized for $R_H(4) = 6453.2$ - Ω steps to be near 6 T, having an electron density of approximately 5.6×10^{11} cm⁻². The zero magnetic-field mobility at 4.2 K is ≈ 11 m²/V s.



FIG. 3. Schematic diagram of the isolated gate bias supply.

A scale drawing of the Hall bar geometry of the GaAs/Al-Ga-As heterostructure is shown in Fig. 4 with a schematic section view shown in Fig. 5. The bar was defined using standard photolithographic and wet-etching techniques. The resulting Hall bar was ≈ 4.6 mm long and ≈ 0.4 mm wide. Three sets of Hall potential probes were placed along it as shown. The two outer probe sets were symmetrically displaced ± 1.0 mm along the channel from the center set. The layers had the following thicknesses: GaAs:Cr⁺, 500 μ m; GaAs channel layer, 60 nm;



FIG. 4. Top view of GaAs(7) showing current leads and three sets of voltage leads.

 $Al_x Ga_{1-x} As$ buffer layer, 10 nm; $Al_x Ga_{1-x} As:Si$ donor layer, 60 nm; GaAs cap, 10 nm; and GaAs:Si contact doping layer, 20 nm.

Electrical contacts were made to the two-dimensional (2D) electron gas by alloying indium into the heterostructures at 400 °C for 5 min in the presence of the Si-rich top layer. After contacting, that top layer was etched away to eliminate it as a parallel conduction path. The In contact region overlaps the edge of the mesa in order to prevent spurious current loops of 2D electrons from encircling the contacts. The back side of the chip was mounted directly on a TO-8 header using a tiny spot of Apiezon grease.

III. CRYOGENIC SYSTEM

A dilution refrigerator system with a 15.7-T persistentcurrent magnet and 25.4-mm-diam removable sample



FIG. 5. Section view of GaAs(7). The uppermost layer is etched off after providing a source for impurities during contact fabrication. probe was used for the comparisons. The sample was surrounded by one mole of liquid He³ which was cooled indirectly via the dilution refrigerator.

The 2.7-m-long sample probe was strung with six twisted pairs of 0.12-mm diam, Teflon-insulated copper Omega Engineering thermocouple reference wires. A set of matching tapered copper cones thermally anchored the wires at the mixing chamber temperature, 60 cm above the sample. Above that point, the residual vapor pressure of the He³ at the 320-345-mK operating temperature provides thermal contact between the wires and the walls of the probe, and between the probe and the walls of the probe sheath. The system was continuously maintained at its operating temperature for periods of weeks at a time. Thermal voltages on all voltage lead pairs were less than 0.5 μ V and varied by less than 10 nV per hour. The wires terminated at a TO-8 socket at the low end to receive the sample header and were isolated from each other and from ground by at least $10^{14} \Omega$.

The temperature was measured by a rhodium-iron thermometer calibrated against EPT-76 above 0.5 K and by a germanium thermometer calibrated below 0.5 K against the cryogenic temperature scale, CTS-1. The thermometers were located on a thermally isolated platform in a low-field (< 0.05 T) region 60 cm above the sample and connected to the sample region by a *separate* thermal path from that used for refrigeration. This arrangement, which is analogous to four-lead resistance measurement, avoids temperature errors caused by heat flowing from the sample to the refrigerator.

The magnetic-field value was calculated from the measured current using a calibration coefficient supplied by the manufacturer. Relative changes in magnetic field were monitored by a Hall sensor located on the top of the magnet. In persistent current mode the field decayed at a rate of 150 ppm/day at 14 T.

IV. MEASUREMENT SYSTEM

The measurement system consisted of an automated potentiometer utilizing a Leeds and Northrup 9829 linear amplifier as a null detector. A full description has been given by Marullo-Reetz and Cage.¹¹ For the Si-MOSFET measurements the current source was modified to produce 8.8 μ A instead of the 25 μ A used for the GaAs/Al-Ga-As heterostructures. Also, it was found that the inner guard grounding point needed to be moved to the null-detector input. (It had been at the roomtemperature end of the Hall voltage leads of the sample.) This was made necessary by the much greater sensitivity



FIG. 6. Histogram of 152 11-min measurements. The solid curve is a fitted Gaussian distribution with parameters shown.

of the Si-MOSFET to ac common-mode noise generated by the amplifier chopper.

Since the system voltage noise remained the same for both types of samples, the random error in the resistance measurement scaled inversely as the measurement current. Consequently, a $(25 \ \mu A/8.8 \ \mu A)^2 \approx 8$ times longer measurement time was required to attain the same error for the Si-MOSFET measurement as for the heterostructure measurement. In order to reduce the random error for measurements on the Si-MOSFET sample to ± 0.004 ppm, 18 h of integration were required. Figure 6 is a histogram of point 59 wherein 152 independent readings were made over a period of 28 h. The solid curve is a Gaussian distribution with the same mean and standard deviation as the data. It is apparent that the data are randomly distributed and that the use of day-long averages is justified.

Previous experience with this measurement system during GaAs-heterostructure measurements has indicated that, for unknown reasons, the potentiometer bridge balance depends slightly on whether the sample or the reference resistor is placed in the "sample" position of the bridge. We refer to this as the *interchange error*. Also, it is desirable to test if the automatic gate-voltage shift (described in Sec. II B) has any effect on the measured resistance. Accordingly, four sets of measurements as summarized in Table II were made to evaluate these effects. The interchange error evident from an examination of the data in Table II is seen to be $+0.019 \pm 0.005$ ppm. The interchange error similarly derived from the GaAs/Al-Ga-As heterostructure

TABLE II. Tests of measurement system for "interchange" and gate voltage shift effects.

Characteristic	Measurement conditions				
$V_{q}(\mathbf{V})$	14.53	14.55	14.55	14.57	
Configuration	normal	normal	interchanged	normal	
V_{q} shift	off	on	on 50%, off 50%	on	
No. of points	31	32	227	272	
$(R_H - h/4e^2)/R_H \text{ (ppm)}$	-0.025(8)	-0.020(10)	-0.008(4)	-0.027(3)	

measurements using $25 \ \mu$ A, $+0.0087 \pm 0.0016$ ppm, was somewhat smaller but of the same sign. All measurements reported in the following section have been corrected for the interchange error by adding 0.0095 ppm to data taken using the "normal" configuration and by subtracting 0.0095 ppm from data taken using the "interchanged" configuration.

Table II also shows that there was no detectable effect on plateau measurements of the automatic gate-voltage shifting. Later, however, the gate-voltage shifting was found to cause difficulties during R_x measurements, and it was disabled for all points after point 28, even including R_H measurements. Thus, for these points, the measured value is the average of the true values for gate voltages 26 mV (empirically determined) on either side of the nominal voltage for which they are plotted.

One important aspect of our experimental procedure should be stressed. Several maintenance activities interrupted the measurements between points. It was necessary to recharge the detector batteries for several hours each day, transfer liquid helium and let thermal transients die out for a few hours every second day, and replace the batteries in the gate bias supply every 5 days. During these maintenance periods the gate bias was turned off in order to stretch out the lifetime of the gate-bias supply batteries. Consequently, between most points, the potential well holding the two-dimensional electron gas was nonexistent for 3 to 8 h. The magnetic field, however, was left on continuously and the sample temperature remained below 350 mK.

V. RESULTS

A. Overview

Four months of nearly continuous measurements were made on the i = 4 plateau of the Si-MOSFET sample with an accuracy better than 0.01 ppm. During that time the plateau shape with respect to gate voltage was seen to change. Furthermore, even when stabilized in time, it was not flat, but rather had systematic fluctuations as a function of gate voltage which were of the order of 0.04 ppm around the nominal GaAs value. There was also a period of weeks when extremely irregular values were obtained that were up to 0.4 ppm above the GaAs value. This was initiated by a lightning-induced laboratory power failure and ended when the sample was "cleansed" by warming to 300 K overnight. The data described in the remainder of this subsection and in subsections VB and VC below were all taken after this "cleansing." Furthermore, whenever thunderstorm activity was forecast, the sample was disconnected from the measurement system and all of its leads were shorted to its grounded shield.

These results would not be so surprising except that the diagonal resistivity ρ_{xx} remained exceedingly small, on the order of 0.001 ppm of the Hall resistivity ρ_{xy} (the limit of our resolution). Nearly all measurements were made at temperatures below 350 mK, although no temperature effects were noticed even when the temperature rose to 750 mK. The measurement current was 8.83 μ A,



FIG. 7. Normalized Hall resistance R_H and longitudinal resistance R_x vs magnetic field for $V_q = 14.36$ V.



FIG. 8. Normalized Hall resistance R_H vs gate voltage V_g at a magnetic field of 14.0 T.



FIG. 9. An expanded plot of the i = 4 plateau at $V_g = 14.5$ V in Fig. 8.



FIG. 10. A further expansion of the plateau of Fig. 9.

the maximum deemed safe for the sample. Nearly all data were taken at a magnetic field of 14 T and gate voltages around 14.4 V.

The Hall resistance R_H and longitudinal resistance R_x for the Si-MOSFET sample under a gate bias $V_g = 14.36$ V are shown in Fig. 7 as a function of magnetic field up to the i = 4 plateau at 14.0 T. Here, the ordinate values are expressed in dimensionless form by plotting the resistance divided by the quantum value at i = 4, $h/4e^2$. In the classical regime at low fields where R_H is linear in field and R_x approaches a constant, the data yield a mobility of 1.3 m²/V s. At higher fields, R_x is seen to undergo quantum oscillations which drive it to zero at 7.3, 9.5, and 14 T. R_H is seen to produce well-defined plateaus at those field values, corresponding to i = 8, 6, and 4, respectively.

When the gate voltage is lowered while maintaining the magnetic field at 14.0 T, R_H and R_x vary as shown in Fig. 8. Here, the ordinate values are obtained by dividing the resistance by the quantum value at i = 1, h/e^2 . At these lower gate voltages, the carrier density is reduced and the i = 2 plateau occurs at $V_g = 7.7$ V. The i = 1plateau, however, cannot be observed because the channel mobility becomes too low at $V_q = 3.5$ V. All of the remaining discussion centers on the i = 4 plateau shown in this figure between $V_g = 14$ and 15 V. This region is shown in an expanded form in Figs. 9 and 10 which were obtained by connecting an x-y recorder to the output of the bridge null detector. They show the deviation of R_H from the theoretical i = 4 value. The remarkable rapidity with which the wings of the plateau reach the plateau value is clearly apparent from Fig. 10. At this level of precision, none of the irregularities we have observed on this plateau are visible.

B. Fluctuations in the plateau

When the plateau of Fig. 10 was examined with the full sensitivity of our measurement system, the data shown in Figs. 11 and 12 were obtained. Here each point typically represents the average of eighty 11-min measurements of the Hall resistance, designated as $R_H(3, 4)$, measured using connection P3 (see Fig. 1) as the "high" lead and



FIG. 11. The i = 4 plateau at full resolution after the sample had been below 0.5 K for two months. The corresponding ρ_{xx}/ρ_{xy} data are given in Fig. 15.

connection P4 as the "low" lead. The numbers next to each point identify that point and are sequential in time. The direction of the magnetic field was such that, in this case, the source was connected to the "low" current lead and the drain was connected to the "high" current lead. Measurements presented below which are represented by $R_H(4,3)$ have the voltage and current "low" and "high" leads reversed. (The measurement system, of course, in either case reverses the direction of the current regularly to avoid the effects of thermal EMF voltages.)

That Figs. 11 and 12, if superimposed, do not form a single curve is the result of the observed time variation of the plateau. In fact, data taken during the first week of refrigeration, points 29–32 of Fig. 12, clearly show a large change between point 29 and 30. Points 33 to 44, however, do form a relatively consistent, undulating curve. This is particularly evident for the data in Fig. 11, which were measured after the sample had been kept below 0.5 K for two months. The measured resistances for points 56 to 62 form a consistent, undulating curve whose range of fluctuation clearly exceeds the statistical



FIG. 12. High-resolution measurements of the plateau taken during the first month after a "cleansing" at room temperature. The corresponding ρ_{xx}/ρ_{xy} data are given in Fig. 14.



FIG. 13. Measurements of the plateau resistance using two other configurations of measurement connections to the sample. See Fig. 15 for the corresponding ρ_{xx}/ρ_{xy} values.

error bars of the individual points. This was true even though adjacent points were not measured sequentially. The time variation of the plateau was, therefore, not a factor for this group of points.

The undulations shown in Figs. 11 and 12 would actually be slightly greater if the automatic adjustment capability of the bias supply had not been disabled as described earlier in Sec. IV. Each point in these figures represents an average value of R_H for gate voltages 26 mV on either side of the plotted gate voltage.

During the month between the measurements of Figs. 11 and 12, measurements of the plateau were also made using other connections to the sample. These are shown in Fig. 13 wherein two points are $R_H(1,2)$ measurements and the remainder are $R_H(4,3)$. There is a strong expectation that $R_H(3,4) = R_H(4,3) = R_H(1,2)$ for a Hall device with negligible R_x . Any undulation in this group of data in the region of the plateau center is smaller than that in Figs. 11 and 12. However, the tailing off between $V_g = 14.55$ and 14.70 V, we believe, is not simply the onset of the plateau's upper edge because, as shown in the following subsection, R_x remained exceedingly small in this region.



FIG. 14. ρ_{xx}/ρ_{xy} vs V_g for the period of time when the plateau data of Fig. 12 were obtained. Here ρ_{xx} was obtained from $R_x(2, 6)$.



FIG. 15. ρ_{xx}/ρ_{xy} vs V_g for during the time when the plateau data of Figs. 11 and 13 were obtained. Here ρ_{xx} was obtained from $R_x(5, 1)$.

C. Measurements of diagonal resistivity, ρ_{xx}

What makes the measurements presented in the preceding section remarkable is the fact that this sample has an exceedingly low diagonal resistivity, ρ_{xx} . This is shown by the R_x vs V_g data presented in Figs. 14 and 15. Here, in order to facilitate correlation with the plateau measurements, the identification numbers of the ρ_{xx} points were formed by taking the point number of the preceding R_H measurement and adding an "a," "b," or "c." Also, we use here the intrinsic quantities $\rho_{xy} = R_H$ and, for our geometry, $\rho_{xx} \approx R_x/4$. The data in Figs. 14 and 15 were derived from measurements of $R_x(2, 6)$ and $R_x(5, 1)$, respectively.

These data show that $\rho_{xx}/\rho_{xy} \leq 0.002$ ppm at gate voltages where the fluctuations described above were observed. Furthermore, even during point 41 when $\rho_{xx}/\rho_{xy} \approx 0.007$ ppm, ρ_{xy} was within 0.010 ppm of the GaAs value. In general, we avoided the edges of the plateau, since on occasions when we accidentally selected a gate voltage which was off of the plateau, the effect on R_x and R_H was so great that high-accuracy measurements were pointless.



FIG. 16. Plateau measurements before a major electrical disturbance.

D. Observation of metastable plateaus

The metastable behavior mentioned in Sec. V A, which led to our "cleansing" of the sample at room temperature and subsequent isolation of it during times of possible thunderstorm activity, is a phenomenon which should be reported. It is especially peculiar that the Si-MOSFET sample exhibited metastable plateaus which were offset *above* the equilibrium plateau. This behavior may be related to the observations by Kawaji *et al.*^{5,6} and by Kinoshita *et al.*¹² of Si-MOSFET plateaus existing up to 0.16 ppm *above* the accepted $h/4e^2$ value. Unfortunately, since we could neither intentionally initiate nor control this behavior, the data we report here are fragmentary.

After cooling the Si-MOSFET sample for the first time, we left it at 1 K for a few days and then performed the various tests below 350 mK, verifying that ρ_{xx} was small, and obtaining the data in Table I and curves similar to Figs. 7-10.

Our first precision measurements at the center of the plateau were intended to compare the Si-MOSFET plateau value with that from GaAs(7). They are displayed in Figs. 16 and 17. Note that Fig. 17 has a very much coarser ordinate scale than Figs. 11, 12, and 13. Although the first few points are consistent with Figs. 11, 12, and 13, points 8, 9, and 11 deviate by more than 0.05 ppm and points 19 through 27 deviate by more than 0.1 ppm. (Point 17 is likely to be at the upper edge of the plateau.) The only high-precision measurements of R_x made during this time (points 26a and 27a) indicated that ρ_{xx}/ρ_{xy} was less than 0.009 ppm.

During the period when these measurements were made, we were unaware of the possible sensitivity to thunderstorm activity and did not try to halt the measurements and protect the sample during thunderstorms. A thunderstorm-induced power failure abruptly terminated the measurements constituting point 16, the final point plotted in Fig. 16. Power failures also occurred between points 8 and 9, 22 and 23, and 23 and 24. A check of Weather Service thunderstorm activity reports indicate thunderstorm activity occurred during points 3, 16, 17, 24, and 27, and between points 6 and 7, 8 and 9, 16



FIG. 17. Plateau measurements after the major electrical disturbance. Note that the ordinate in this figure spans twice the range as that of Fig. 16.

and 17, and 26 and 27. Note, however, that some of the displaced points shown in Fig. 17, specifically points 24, 25, and 26, still have very small statistical errors. The large uncertainties of many of the other points reflect our early termination of the measurement series rather than greater scatter of individual 11-min samples. It is possible that points 19 through 23 might have produced a single curve if longer averages had been taken.

Following point 27, we warmed the sample and left it at room temperature overnight, "cleansing" it. When it was cooled back below 1 K, the irregularities shown in Fig. 17 had disappeared, and we proceeded to make the measurements presented in Secs. V A–V C. For those measurements, great care was taken to protect the sample during periods of possible thunderstorm activity or system maintenance. The sample was disconnected from the measurement system and its contacts were shorted to its metallic probe casing.

VI. DISCUSSION

Our measurements have revealed two surprising features of the plateau in our Si-MOSFET sample: (i) a metastability which can make the plateau resistance take on values up to 0.4 ppm *higher* than the nominal value, and (ii) smooth undulations of the plateau resistance spanning a 0.05-ppm-wide range about the nominal value even though the diagonal resistivity is less than 0.002 ppm. We have been unable to find a convincing explanation for either phenomenon if indeed they are actually separate phenomena. In this section, we therefore simply point out published work which might shed light on our results.

A. Plateau metastability

It seems clear that the metastability we observed (see Sec. V D) is the same phenomenon that led Kawaji^{6,12} to report discrepancies between the values of h/e^2 determined by measurements on Si-MOSFET samples compared with those determined using GaAs/Al-Ga-As heterostructure samples. In both cases the resulting values from the Si-MOSFET samples were predominantly *higher* than those from the GaAs/Al-Ga-As samples, but in our case, the metastability was less rigid and more easily noted. This metastability persists irrespective of changes in the gate voltage, but is reset when the sample is warmed to room temperature.

Samples exhibiting the quantum Hall effect are known to be metastable in several ways which are fairly well understood. The Si donors in the Al-Ga-As:Si layer of GaAs/Al-Ga-As heterostructures are excited past the Al-Ga-As buffer layer into the depletion region by either optical excitation or by thermal activation¹³ during the cooldown from room temperature. Under the normal conditions for precision measurement ($T \leq 1.5$ K and no light) the resulting carrier concentration is frozen at a metastable value. Alternatively, donor traps in the Al-Ga-As layer can lead to metastable parallel conduction paths.¹⁴ Similarly, in Si-MOSFET, localized states in the SiO₂ layer near the SiO₂-Si interface metastably trap carriers.¹⁵ In fact, prior to making precision measurement on Si-MOSFET samples, it is customary to wait for several days after the initial cooldown for the samples to stabilize. This relaxation is governed by a phenomenon which evolves independently of the application of the gate voltage.

Other metastable phenomena, particularly in Si-MOSFET, have been reported which are not so well understood. Pudalov, Semenchinsky, and Edelman¹⁶ have reported surprisingly long relaxation times in measurements of the response of the two-dimensional electron gas to gate-voltage changes as the gate voltage is swept through the plateau region. They attribute this to the creation by potential irregularities of islands of a different filling factor which cannot readily equilibrate.

Metastable results could also be caused by different levels of persistent currents. Persistent currents can exist either as macroscopic currents associated with the (near) vanishing of ρ_{xx} or as phase-coherent mesoscopic currents. The former make it necessary to construct contacts which are not encircled by the two-dimensional electron gas.¹⁷ The phase-coherent persistent currents, based on a predicted lack of backscattering of edge currents,¹⁸ are the subject of a number of recent papers.¹⁹ Surprisingly long coherence lengths, up to 100 μ m, are reported.²⁰⁻²²

Mechanisms for metastability that uniformly change the electron density cannot shift the value of the plateau resistance. They simply cause a shift in the location of the plateaus with respect to magnetic field or gate voltage, and might change the plateau widths, but the plateau resistance remains quantized as long as the diagonal resistivity remains small.

Parallel conduction mechanisms will result in the plateau having a resistance *lower* than the nominal value. If the shunt is across the current leads, less current will flow through the sample than was supplied by the current source. Hence, the Hall voltage, and consequently the calculated Hall resistance, will be lowered. Because the Hall voltage contacts are connected by equipotentials to adjacent current leads, leakage across the voltage leads will have the same effect as leakage across the current leads.

On the other hand, it is also difficult to imagine how an explanation based on persistent currents can lead to successive points lying on an offset plateau. Between each point the gate voltage, and hence the two-dimensional electron gas density, was set to zero for several hours. That the offset points formed flat plateaus was more clearly evident in Kawaji's measurements²³ than in ours, since his data on the offset plateaus were highly repeatable and seemed to have no connection with thunderstorm activity.

Edge currents, which were originally described as skipping orbits at an abrupt potential barrier, are now better understood as simply an enhanced $\mathbf{E} \times \mathbf{B}$ drift at the electric fields defining the sample edges. This same effect also governs the bulk current, but when the Fermi level is between the bulk Landau levels, the scattering properties at the edges become important. The current on the low-potential edge flows counter to the net sample current.

In 1988, Büttiker¹⁸ pointed out a remarkable lack of backscattering for edge currents. Many authors are now stressing^{20,21,24,25} that the quantum Hall effect at lower current levels is controlled by edge currents, and that the exact details of the contacting process have measurable effects even in four-lead measurements.^{26,27} Applying the Büttiker mechanism to the general measurement geometry, Hirai and Komiyama²⁷ have determined that the error attributable to contact resistance can be estimated by

$$\frac{|\Delta R|}{h/i\epsilon^2} \le 2(i-1)^2 \delta_V^2 \delta_I,\tag{2}$$

where δ_V and δ_I are the resistances of the voltage and current contacts expressed as fractions of the plateau value, h/ie^2 . Equation (2) applies to R_H measurements made using contacts P3 and P4 which are separated from the source and drain contacts by unused voltage contacts P1, P2, P5, and P6.28 Using the contact resistances given in Table I for our Si-MOSFET sample, Eq. (2) indicates that the error in the plateau resistance resulting from this mechanism is less than 0.001 ppm. The measured value of R_H between P1 and P2 (point 46 in Fig. 13) shows no difference from those between P3 and P4 to within 0.005 ppm. This fact again contradicts the expectation based on Ref. 27. Actually, the assumption, upon which Eq. (2) is based that edge currents dominate in our Si-MOSFET sample when measured at 9 μ A, is probably invalid. It is likely that the edge currents saturate at a much lower current and that the actual contact-induced error related to the Büttiker mechanism is much less than 0.001 ppm.

Resistance plateaus that are slightly *higher* than the nominal quantized values mean that either more than the measured current passed through the sample or that the measured current was somehow more effective in producing a Hall voltage. If sample irregularities, perhaps near the edges, caused some of the current to pass through regions with i = 2 and the final Hall voltage reflected a sum of the voltages, then an apparently raised Hall resistance would result. Such a process, however, would require a revision of the conventional explanations of the exactness of the quantum Hall effect.

B. Plateau undulations

The striking feature of the undulations in the plateau of the Si-MOSFET we studied was that they occurred in spite of an exceedingly low diagonal resistivity. Earlier measurements on Si-MOSFET have established that small (< 1000 ppm) deviations of the plateau resistance in response to increased sample temperature, increased source-drain current, or nonoptimal localization are in direct proportion to the minimum diagonal resistivity, ρ_{xx}^{\min} . Specifically, for a given plateau the relation

$$\Delta \rho_{xy} / \rho_{xy} = -s \rho_{xx}^{\min} / \rho_{xy} \tag{3}$$

holds where s is an empirically determined quantity. For

Si-MOSFET of nearly identical construction to that of our measurements, Yoshihiro, *et al.*¹⁵ have found that $s \approx 0.15 \pm 0.04$. Hence, since we found that $\rho_{xx} = R_x/4 \leq 0.002$ ppm, the greatest irregularities on the plateau should be less than 0.0003 ppm. This is two orders of magnitude smaller than the observed undulations (Figs. 11 and 12).

It seems most likely that the key parameters governing the appearance of these undulations are sample size and measurement current. Hartland⁸ has recently made extremely precise measurements on a Si-MOSFET sample which yielded no unusual behavior and had the same quantized Hall resistance as GaAs/Al-Ga-As to within 0.0004 ppm. His sample was 3.3 times wider, had a three-times thicker (and perhaps more uniform) oxide, and somewhat lower mobility (65%) than ours. Also, its current capacity was six times greater allowing him to use a measurement current of 54 μ A. If we assume that the plateau undulations we measured are not the result of some subtle differences in the microscopic structure, we would have to conclude that these undulations disproportionately increase in magnitude as sample size or measurement current decrease. It seems unlikely that the small difference in mobility is important.

It is possible that the observed undulations are related to the "universal conductance fluctuation" phenomenon which comes about from the coherent interference of electrons with themselves as they undergo multipath scattering. Although this has been very thoroughly studied in metallic mesoscopic systems,²⁹ a similar phenomenon has been seen in macroscopic Si-MOSFET samples^{30,31} which were particularly well isolated from external noise. These resistivity fluctuations, seen in 100- μ m-wide samples, increased in magnitude as the current was *lowered*, increased dramatically with decreasing temperature, and decreased rapidly with increasing gate voltage. The magnetic-field dependence, however, was slight and *did not* show fluctuations, but rather simply revealed a negative magnetoresistance.

The fluctuation phenomenon observed by Kinoshita et al.,^{30,31} the edge current effects observed by Komiyama et al.,²¹ and the edge currents observed Kane, Tsui, and Weimann,²⁴ predominate at lower currents. As the current is increased above about $0.2 \ \mu A$, they begin to switch off and are relatively unimportant above 2 μ A. van Son³² and van Son and Klapwijk³³ have examined this crossover which occurs when the edge currents saturate at $ie(\omega_c/2\pi)/2 \approx 2 \ \mu A$ for i = 4 and B = 14 T. Here ω_c is the cyclotron frequency. This is a factor of 4 smaller than the current used in our experiment, and it is clearly desirable to make additional measurements at lower currents. Although this is practical using existing precision measurement systems, unambiguous measurements will require a very stable device and be quite time consuming. Several months will be needed, taking data at a rate of one point per week, to map out just one plateau.

The difference in sample width by a factor of 3.3 between our sample and Hartland's must also be treated as a possible reason for our contradictory results. Since the fluctuations in mesoscopic samples are on the order of 10^7 times greater than these undulations, it is possible that the undulations are the remnant interference present in samples which are 100 times wider than mesoscopic. Delahaye and Bournaud,⁷ however, were using samples made by Kawaji with very similar characteristics to ours. Although we have no explanation for their negative results, we note that our first measurements (points 1–5 of Fig. 16) showed no discrepancy to within 0.01 ppm, the precision quoted by Delahaye and Bournaud. It was only upon prolonged observation that the irregularities became apparent.

The basic theory of the "universal" conductance fluctuations (UCF) has been put forth by Al'tshuler and Aronov³⁴ and by Lee, Stone, and Fukuyama.^{35,36} It deals with samples with a uniform current flow at low magnetic fields and predicts a reduction in fluctuations as the sample dimensions exceed the inelastic diffusion length, $l_{\rm in}$. Timp et al.³⁷ have since considered suppression of the Aharonov-Bohm effect in the quantized Hall regime that results if the current is entirely carried by edge states. They show that the lack of backscattering of edge states pointed out by Büttiker¹⁸ leads to an exponential diminishing of the UCF amplitude as

$$\Delta \sigma / \sigma = \exp(-L^2 / 8r_c^2), \tag{4}$$

where the geometric length is compared with the cyclotron radius, r_c , instead of $l_{\rm in}$. Using numbers for our sample, this relation predicts a total suppression of the fluctuations for our samples. Presumably, if the current flow in our sample is neither perfectly guided along the edges, nor uniform throughout the sample, there can still exist a small, but measurable, fluctuation amplitude. Nevertheless, all explanations of the plateau undulations based upon the UCF phenomena predict deviations of ρ_{xx} to be similar in magnitude to those of ρ_{xy} , not 100 times smaller.

VII. CONCLUSIONS

In contrast to the use of the Josephson effect as a voltage standard, the reliable use of the quantum Hall effect as a resistance standard involves a much greater care in sample preparation and a deeper understanding of its underlying physics. Although the quantum Hall effect in some Si-MOSFET samples has been shown by Hartland *et al.*⁸ to yield the same resistance quantization as in GaAs/Al-Ga-As heterostructures to an accuracy of 0.0004 ppm, we have studied a Si-MOSFET sample which has a plateau unevenness two orders of magnitude larger. This is remarkable because our sample was otherwise ideal. It had an exceptionally low diagonal resistivity, less than 0.002 ppm of the Hall plateau resistivity.

Our sample also exhibited metastable plateaus up to 0.4 ppm *above* the nominal value which were sensitive to thunderstorm-induced electrical disturbances. These appear to be related to the offset plateaus observed by Kawaji *et al.*, 5,6,23 who was using nearly identical sam-

ples to ours.

Although a variety of phenomena were considered which might explain these observations, none is completely satisfactory. Additional quantitative calculations of fluctuation effects in wide samples and of currentsensitive edge state phenomena would be useful. The high-precision measurements required for this work are extremely time consuming. Numerous obvious extensions of the present experiments which can be envisioned must be postponed until more sensitive instrumentation is available.

Note added in proof. O. Heinonen has recently calculated effects caused by edge state-impurity interactions

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