Read, D.; Geiss, R.; Alers, G.
Title: Study of Fatigue Behavior of 300 nm Damascene Interconnect Using High Amplitude AC Tests
Journal: MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS; 2007; VOL 990
Page: 121-126
Publisher: Warrendale, Penn.; Materials Research Society; c2007

Study of Fatigue Behavior of 300 nm Damascene Interconnect Using High Amplitude AC Tests*

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ABSTRACT

The AC fatigue test technique, which uses cyclic joule heating to apply thermal cycles to thin-film structures, was applied to copper lines and vias in damascene dielectric structures on silicon substrates. Specimen chips with two different types of dielectric, oxide and low-k, were tested. The lines were 300 nm wide; various via widths were tested. At 100 Hz, cyclic temperature ranges from 400 to 900 ºC produced line lifetimes between 10 and 1 million seconds. Similar lifetimes were reached in the vias for temperature ranges between 100 and 500 ºC. When the data were plotted either as number of load reversals to failure or as lifetime against cyclic temperature range, the trends for the two different types of dielectric were indistinguishable. The temperature values at the one-reversal intercept for both types of dielectric were above 1000 ºC. The via data were more scattered, but trended toward a lower intercept temperature.

INTRODUCTION

Along with billions of transistors, the ultra large scale integration logic chips in the current generation contain billions of individual “interconnects”, which are copper conductors connecting different transistors and other components within a chip. The reliability of these interconnects is critical because a single failure can render the whole chip inoperative. Stresses in the interconnect system are created during manufacture by chemical-mechanical polishing and annealing cycles up to around 400 ºC, and during service by both on-off and idle-active thermal cycles of tens of degrees Celsius. Clearly, the idle-active cycle can occur many times per day. Efficient design implies minimization of the physical size of the whole interconnect structure, while maintaining electrical performance and reliability. The mechanical characteristics of the interconnect system define its reliability against stresses from all sources, most importantly, against thermomechanical stresses.

The AC fatigue test technique [1] uses cyclic Joule heating to apply thermal cycles to metal lines and vias in damascene dielectric structures on silicon substrates. Cyclic stresses from differential thermal expansion produce elastic and possibly plastic deformation in the metal line and its surrounding dielectric. The use of high-amplitude, low-frequency alternating current in tests of thin-film copper lines was explored by Mönig *et al.* [1]; they reported surface topography changes that appeared to be mechanical in origin. Tests of aluminum lines under by AC fatigue produced topographic damage in the form of regular undulations or wrinkles [2].

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Extensive transmission electron microscopy (TEM) and scanning electron microscopy (SEM) examination of these aluminum lines revealed that the AC stressing produced dislocations, grain growth, and grain rotation in various regions of the specimen [3,4]. Barbosa *et al.* plotted the behavior of aluminum lines under AC stress as S-N curves, familiar from metal fatigue [5]. They showed that their data could be fit by the Basquin law for fatigue in the appropriate range of cyclic temperature, and that the values of the exponent in the fit were within the same range as those for mechanical fatigue of bulk metals. The stress prefactor in the Basquin law is an estimator of the ultimate tensile strength in metals; they proposed this same relationship for the AC fatigue test. They were able to deduce a value of this stress prefactor that agreed with the ultimate tensile strength for their thin film as measured by the microtensile test [5].

In this paper we report on experiments carried out to explore the application of AC stressing to commercial-style interconnect structures, in particular, two-level copper damascene structures with 300 nm wide interconnect lines. Specimens with two different dielectric systems were available, oxide and a low-k carbon-doped oxide, which have different elastic moduli and hardnesses. Based on the assumption that high-amplitude AC can produce mechanical stresses sufficient to cause failure by fatigue, we hypothesized that the mechanical constraint imposed by the damascene structures could be different in the different dielectric systems, and could produce different S-N curves. So far this has turned out not to be the case. However, we argue that the present data are qualitatively consistent with previously reported calculations [6,7] and measurements [8,9] of stresses in damascene structures.

MATERIALS and TECHNIQUES

We tested two-level damascene copper structures from a commercial source, and also a set of physical vapor deposited (PVD) copper lines on the surface of a silicon wafer. Two types of damascene structures were tested, oxide, and carbon-doped oxide, designated low-k. The test chips contained straight, 300 nm wide lines of copper on metal level 1 (M1), and also Kelvin structures that allowed electrical tests of individual vias. For comparison, electrical tests were also carried out on PVD copper lines 10 μm wide.

In order to characterize the specimens mechanically, we used argon-ion etching to expose the various layers of the damascene structures on sample chips and tested them by nanoindentation [10]. The various layers are identified in Figure 1; the indentation data are shown in Table I. The values reported are averages for indentation depths between 100 and 200 nm. The tabulated values show that the properties of the two types of dielectrics are definitely different. The values listed in Table I must be considered approximate because of the thin layers and the etching procedure. The values for the oxide dielectric are approximately the same as values for bulk fused quartz obtained on the same instrument. The low-k dielectric, as expected, has a lower reduced modulus and hardness than the oxide dielectric. The increasing modulus and hardness of the low-k dielectric with depth in the structure were likely produced by repeated curing cycles as subsequent layers were added. Copper has a higher modulus and lower hardness than both types of dielectric. The cause of the low value of the reduced modulus for M2 of the low-k specimen is not known; this value is considered not reliable. In both specimen types, the base layer, D0, between M1 and the silicon wafer, is oxide.

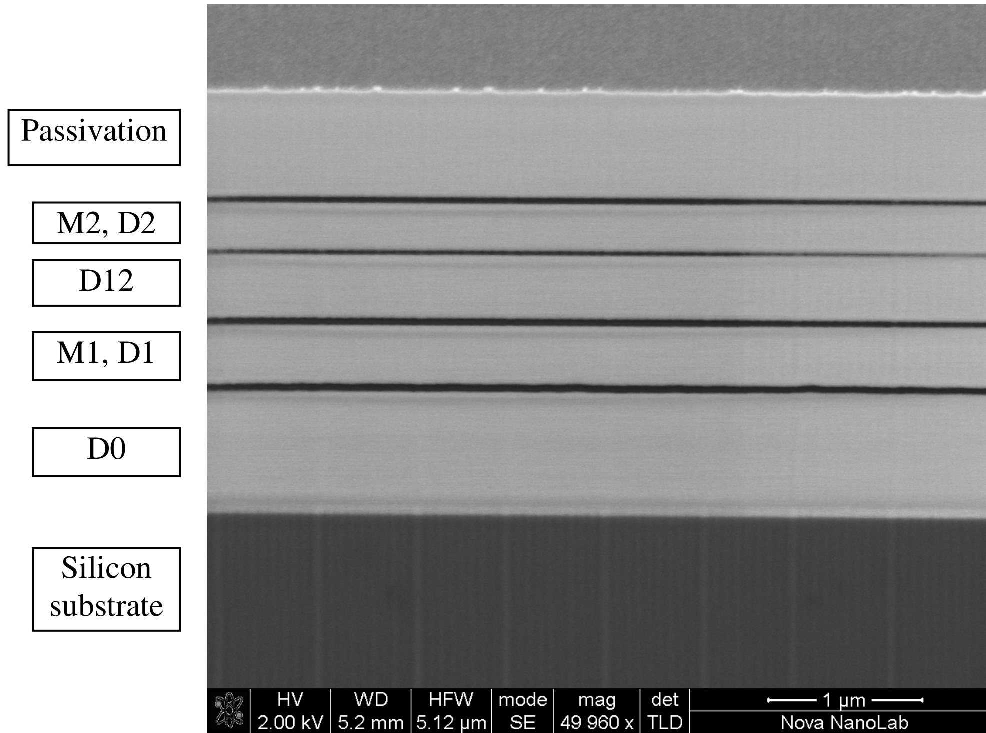

Figure 1. Sectional view of the dielectric layers in the two-level damascene structures tested, produced during focused-ion-beam (FIB) milling in a region without metal. In the layer designations, M denotes metal, and D, dielectric.

Table I. Reduced modulus and hardness values obtained by nanoindentation of layers of the damascene structures exposed by ion etching. The uncertainties give the standard deviation of the 20 or more individual measurements that were averaged to obtain each value.

	Damascene copper structures			
Dielectric	Oxide		Low-k	
Layer	Reduced modulus, GPa	Hardness, GPa	Reduced modulus, GPa	Hardness, GPa
Passivation	72±2	9.5±0.4	26±3.3	6.1±0.7
D2	78±2	9.8±0.3	15±1.1	2.2±0.1
M2	123±6	2.2±0.14	30±1.6	1.6±0.1
D12	76±2	9.4±0.3	23±2.7	2.6±0.1
D1	77±2	9.3±0.3	37±5	3.4±0.3
M1	114±8	2.3±0.15	100±4	1.9±0.1
D0	85±2	10.6±0.3	76±2	8.9±0.2
Silicon substrate	156±5	11.9±0.4	161±4	13.1±0.3
	PVD copper, unconstrained			
	Reduced modulus, GPa	Hardness, GPa		
Copper	144±8	2.0±0.15		

The AC tests were conducted under current control in a conventional wafer probe station. Pads on typical four-point structures were contacted by tungsten probes, so we conducted only one test at a time. The chuck was at room temperature for all the high-current tests. Current and voltage on the specimen were recorded under computer control approximately three times per second throughout the tests, which lasted from seconds to days. For comparison, DC tests were conducted on some lines.

As in a previous study [1], digital current and voltage waveform data were collected during the AC test and used to calculate the resistance. The variable electrical resistance of the lines under high-amplitude AC test was used to deduce the cyclic temperature for each test; in all cases, the temperature dropped back to very near room temperature as the current went through zero. The temperature coefficients of resistance (TCR) of our specimen materials were measured on "hot chuck" tests, where the specimen stage was heated slowly over a period of hours and the electrical resistance was measured as a function of temperature. For the lines, both damascene and PVD-on-wafer, the TCR was consistent with the values given by Schuster *et al.* [11]. However, for the vias the resistance changed much less with temperature, presumably because the via structures included a high-resistance, temperature-insensitive barrier layer.

RESULTS and DISCUSSION

The lifetime data for both sets of lines are plotted in Figure 2. The x-axis gives the lifetime in seconds; the y-axis gives the cyclic temperature change. The data sets were compared by fitting them to a logarithmic decrease of lifetime with increasing cyclic temperature. The intercepts agreed within 4 %, while the standard error of these fitting parameters was 5 %; the slopes agreed to within 15 %; both slopes had a standard error of about 10 %. Figure 2 also compares the data for lines in the oxide damascene structure with uncovered PVD lines 10 µm wide. The PVD lines fail at much lower cyclic temperatures. Figure 3 compares the vias and lines in the two types of damascene structures. The failure locus of the vias in the oxide dielectric cannot be distinguished from that of the vias in the low-k dielectric that have been tested so far.

The delta T-N curves for the lines in the damascene structures intersect the one-reversal ordinate at very high levels of cyclic temperature. When converted directly to strain and then stress by the simple thermomechanical formula, the stress values are around 2 GPa, which is very high compared to the expected ultimate tensile strength (UTS) of the copper, ~500 MPa. Consideration of variable mean stresses based on each individual cyclic temperature range, as done by Barbosa *et al.* [5], would not alter this result. The corresponding strain and stress values for the uncovered PVD lines are also large compared to expectations based on the UTS, but less so than the damascene lines. The UTS of the copper in these two structures should be roughly the same, as indicated by the hardness results from nanoindentation (Table I). This difference is qualitatively consistent with reports by Paik *et al.* [8] and Murray *et al*. [9] indicating that stresses in lines in damascene structures are lower than for lines on thin dielectric on silicon, because higher stresses would be required to produce failure in damascene structures. However, the AC tests of the damascene structures introduced very high maximum temperatures (Figure 2), leaving open the possibility that a thermally dominated mechanism is operating instead of or in addition to the mechanical fatigue mechanism reported previously [5].

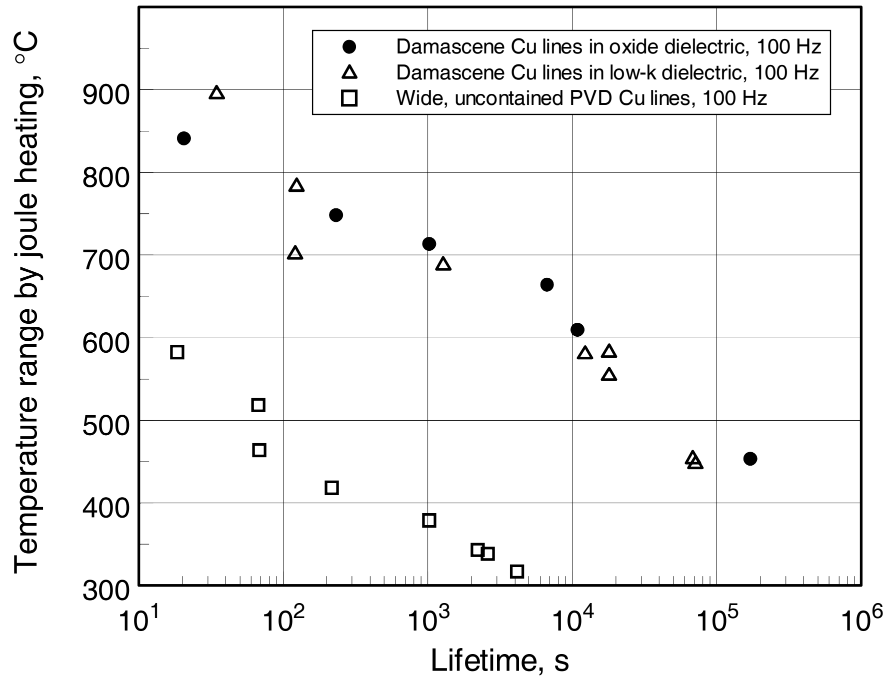

Figure 2. Time to failure under high amplitude AC for damascene lines compared to wide, uncovered PVD lines.

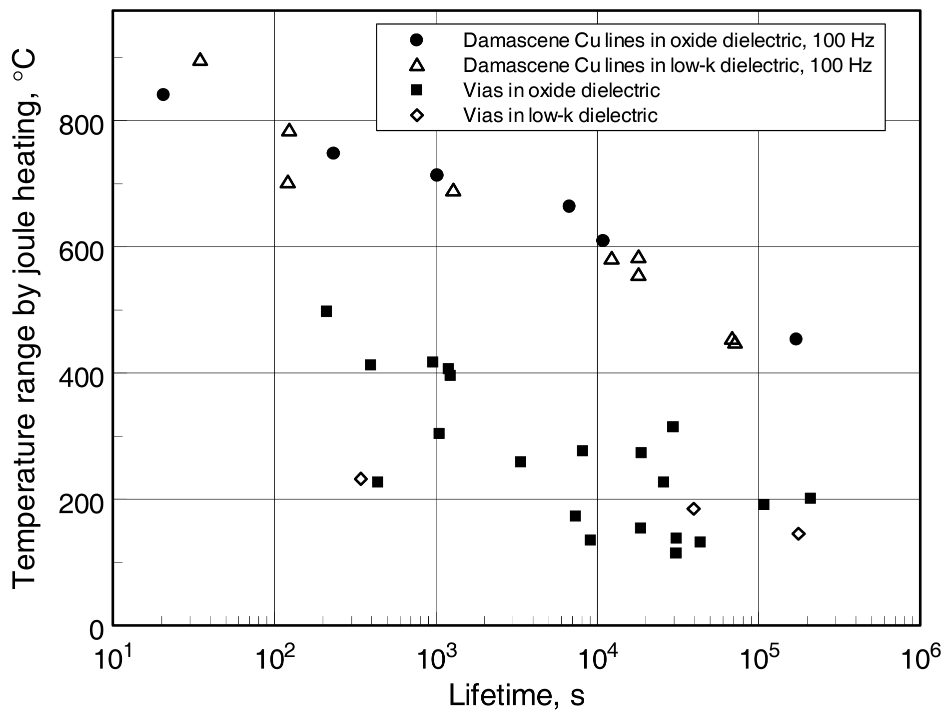

Figure 3. Comparison of line and via lifetimes under high amplitude AC in both types of specimens.

The difference in temperature range at a given lifetime between the damascene lines and vias is also large (Figure 3). This may be a consequence of the higher von Mises stresses in vias than in lines calculated by Paik *et al.* [8], or it may be an indication of other mechanical challenges that confront the via structure, with its built-in barrier layer.

ACKNOWLEDGEMENTS

Financial support for the NIST authors from the NIST Office of Microelectronics Programs is gratefully acknowledged.

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