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Microstructure Evolution during Electric Current Induced Thermomechanical Fatigue of Interconnects

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ABSTRACT

We demonstrate the evolution of microstructure and deformation associated with the use of electrical methods for evaluating mechanical reliability of patterned interconnects on rigid substrates. Thermomechanical fatigue in aluminum and copper interconnects was induced by means of low frequency (100 Hz), high density (> 10 MA/cm^2) alternating currents, which caused cyclic Joule heating and associated thermal expansion strains between the metal lines and oxidized silicon substrate. The failure mechanism involved formation of localized plasticity, which caused topography changes on the free surfaces of the metal, leading to open circuit eventually taking place by melting at a region of severely reduced cross-sectional area. Both aluminum and copper responded to power cycling by deforming in a manner highly dependent upon variations in grain size and orientation. Isolated patches of damage appeared early within individual grains or clusters of grains, as determined by a quasi *in situ* scanning electron microscopy and automated electron backscatter diffraction measurement. With increased cycling, the extent of damage became more severe and widespread. We document some examples of the types of damage that mechanically confined interconnects exhibited when subjected to thousands of thermal cycles, including growth and re-orientation of grains in a systematic manner. We observed in the case of Al-1Si certain grains increasing by nearly an order of magnitude in size, and reorienting by greater than 30°. The suitability of electrical methods for accelerated testing of mechanical reliability is also discussed.

INTRODUCTION

We describe the evolution of microstructure and deformation associated with thermo-mechanical fatigue of patterned interconnects induced by low frequency, high density alternating currents. This study is part of an ongoing program to develop electrical test methods for measuring mechanical response of thin films and interconnects on silicon substrates. The intent of pursuing such methods is to circumvent difficulties of implementing methods such as microtensile testing of free-standing films [1] or nanoindentation of films on substrates [2]. Although these methods are well developed, non-trivial preparation of specimens or interpretation of data can render them cumbersome for routine measurement of properties such as strength or fatigue lifetime. This is a particularly important issue for measurement of small structures such as sub-100 nm interconnects, from which microtensile specimens may be difficult to fabricate, or accurate positioning of an indentation tip may be difficult to achieve.

Reliability issues associated with thermomechanical fatigue center on failures that take place after accumulation of cyclic strain. Examples include resistivity increases due to the introduction of excessive lattice defects [3], brittle film cracking due to deformation of underlying metal films

[4], or open circuits due to metal deformation [5]. Test methods for assessing thermomechanical fatigue in an accelerated manner can be valuable in the design and performance prediction of new interconnect systems.

An electrical approach for testing thermomechanical response of interconnects on silicon-based substrates is well-suited for simulating thermal excursions that occur during operation of devices such as computer CPUs, which can reach temperatures approaching 90 °C, as shown in figure 1. In this example, temperature was measured directly on the case of the chip with a diode built in to a late-model commercial desktop computer. A 70 K temperature change from ambient leads to a thermal strain of approximately 0.1 % and corresponding thermal stresses of approximately 100 MPa for Al on Si and 125 MPa for Cu on Si. For metal films containing no significant residual stress, such thermal stresses result in compression-compression cycling. For films containing large residual tensile stress, such thermal stresses can result in either tension-tension or partially reversed cycling. AC electrical stressing can simulate thermal cycling if the current density is high enough to cause significant Joule heating and if the frequency is low enough to allow significant heat dissipation with each power cycle [6]. We present measurements of fatigue lifetimes in Al-1Si and Cu interconnects as well as observations of the evolution of deformation microstructures in Al-1Si interconnects, due to AC electrical stressing.

EXPERIMENTAL

AC tests were carried out on non-passivated, single-level structures composed of patterned and etched Al-1Si and Cu lines sputtered onto thermally oxidized silicon, using conventional processing parameters. We used a NIST test pattern originally designed for electromigration and thermal conductivity measurements. Tested lines were nominally 800 μm long, 1 to 3 μm wide, and 0.5 μm thick, with current pads and voltage taps at each end of a given line. Testing was conducted on a 4-point probe station using 100 Hz sinusoidal alternating currents with zero DC offset. Current was supplied with a current calibrator, which was driven by an arbitrary wave-

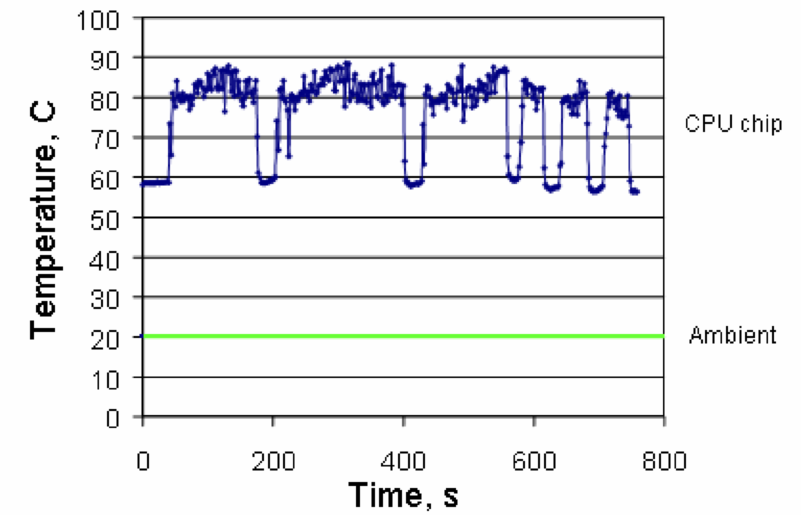

Figure 1. Computer processor temperature versus time during operation of a processor-intensive application, which was run and terminated six times.

form generator. Each test chip was held in place on a steel stage with a vacuum chuck during testing. Lifetime tests were conducted continuously until the test lines became electrically open. Current was measured with an uncertainty of 0.06 mA, and line cross-sections measured with an uncertainty of 0.05 μm^2, leading to an uncertainty in current density of 0.3 MA/cm^2. Current densities (rms) applied to individual lines ranged from 11 to 16 MA/cm^2. Lifetimes to open circuit were determined for all specimens, with an uncertainty of approximately 1 s.

Microstructure evolution during the course of one particular test on an Al-1Si specimen was monitored using field emission scanning electron microscopy (FE-SEM) and automated electron backscatter diffraction (EBSD). A current density of 12.2 MA/cm^2 was applied. The average specimen temperature, as monitored using a thermocouple attached directly to the die, indicated a rise of < 10 K during testing. However, the low frequency AC signals led to temperature cycling superimposed onto the average die temperature, with amplitude of approximately 100 K, at a frequency of 200 Hz [5], corresponding to the power cycling input into the line. FE-SEM and EBSD data were collected from the entire line prior to testing, establishing the as-deposited condition. The line was then subjected to testing for 10 s and removed from the probe station for another series of EBSD measurements. The line was subjected to another 10 s of testing, and so on. In this manner, we collected FE-SEM and EBSD data after the following accumulated times (in seconds): 0, 10, 20, 40, 80, 160, and 320, in a quasi *in situ* test. The specimen eventually failed at 697 s. EBSD measurements were made using an accelerating voltage of 15 kV and electron beam step increments of 200 nm. Scan times were typically less than 5 minutes for the collection of 1800 points with 8 x 8 binning. All EBSD orientation maps are shown in the as-collected state, with no software-imposed filtering or clean-up algorithms applied.

RESULTS

Figure 2 plots applied current density versus time to open circuit, including data from the quasi *in situ* test. The trend is typical of fatigue S-N data. Namely, lifetime increases for lower stress, *i.e.*, current density in this case. We note that despite the small number of data points for copper, a trend seems apparent: for a given target lifetime, copper can withstand higher current density than Al-1Si. More measurements for copper are underway.

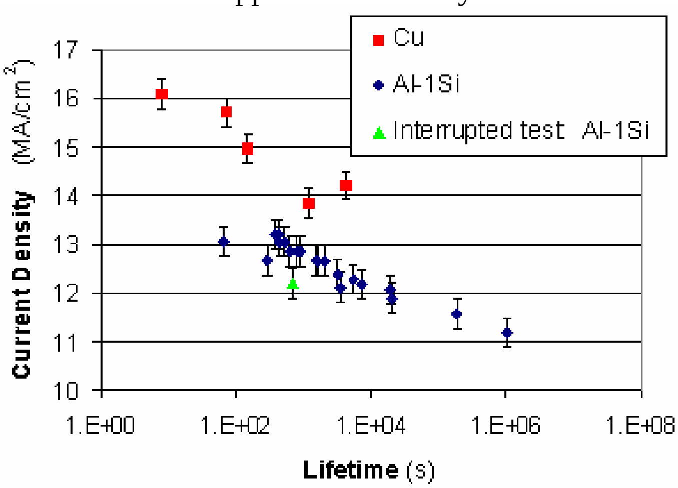

Figure 2. Applied current density versus time to open circuit for Cu and Al-1Si. Data point from quasi *in situ* test is shown in green. Vertical bars represent 0.3 MA/cm^2 uncertainty.

Figure 3 shows the evolution of microstructure with increasing accumulated stressing time for the Al-1Si line tested quasi *in situ*. The left series of SEM images shows the progression of surface damage with time, while the right series shows the corresponding grain structure progression, as revealed by automated EBSD mapping of surface normal orientations. All images were taken from the same area on this specimen. The color legend shown in the inverse pole figure (IPF) to the right of the images indicates that grain orientations started near (111), but some grains changed during testing, ending up near a (112) orientation. Generally, more heavily damaged grains tended to be among the larger grains at the start of a test, and they tended to show more changes in orientation during testing. Further, heavily deformed and re-oriented grains often showed significant grain growth, with grains A and B of figure 3 being good examples. EBSD maps also revealed that heavily deformed grains may initially have had a relatively large Schmid factor compared to the average value for a line, with the rough approximation of loading only along the longitudinal direction of the line. The actual stress state for this line geometry, however, is biaxial, with the stress component transverse to the line being non-negligible compared to that parallel to the line.

Figure 4 is an IPF showing crystallographic orientations associated with surface normal directions, both before and after AC stressing. Red points representing deformed regions indicate that some surface normals reoriented by more than 30°. Reoriented grains tended to cluster in orientation along a wide band extending from approximately (101) to (112).

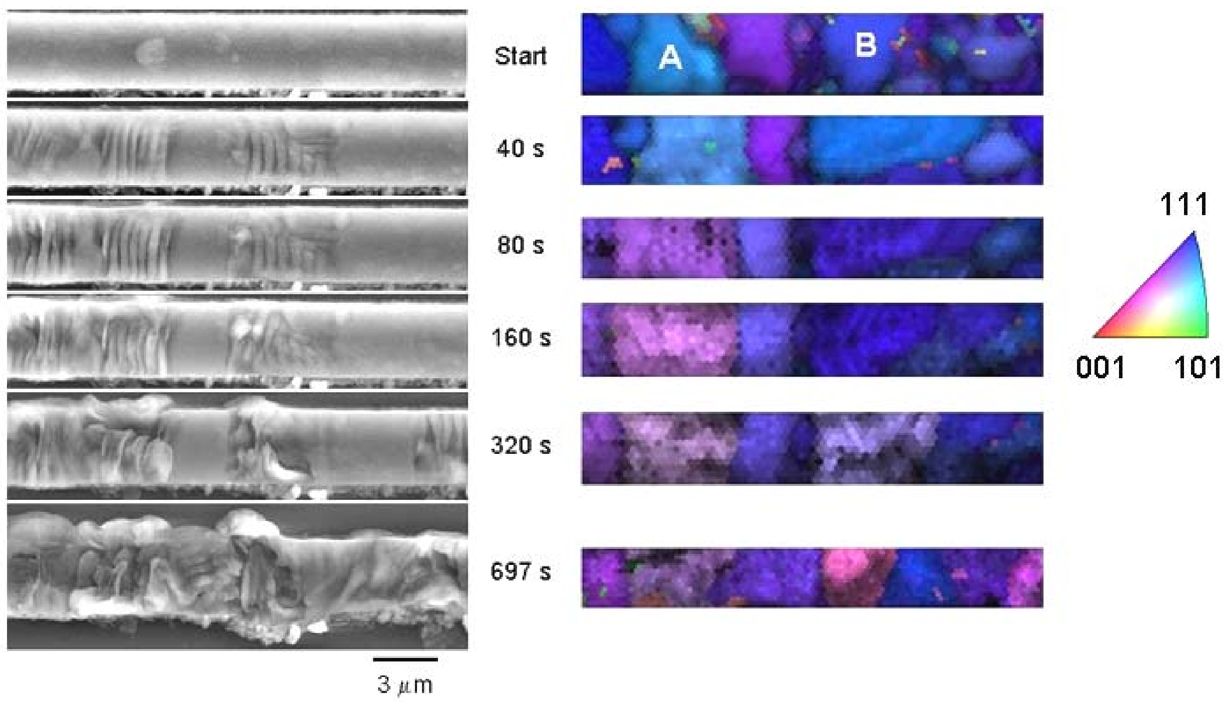

Figure 3. Microstructural evolution as a function of accumulated time of AC stressing. Left series made up of SEM images showing surface damage. Right series made up of EBSD maps corresponding to surface normal orientations, with color legend shown to far right. Grains A and B show both grain growth and reorientation.

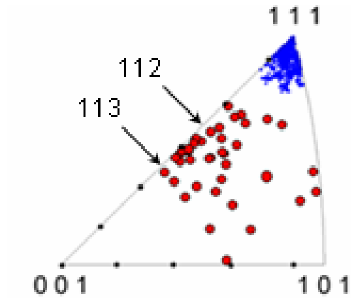

Figure 4. Inverse pole figure showing surface normal orientations before and after AC stressing. Blue dots represent orientations prior to stressing, and red dots represent orientations of severely deformed regions after stressing. Black dots along IPF edges indicate 10° increments.

DISCUSSION

Electrical Methods for Fatigue Testing and other Mechanical Properties

Thermomechanical fatigue is induced by low frequency, high current density AC stressing due to Joule heating. The power input into an interconnect during each power cycle is completely dissipated in the form of heat into the surrounding substrate and/or passivation (if present). This is because the thermal diffusivity of materials such as silicon or silicon dioxide is of the order of 10^{-4} m^2/s, allowing relatively large heat flow from the current-carrying interconnect into the surrounding materials during the period of one power cycle. The mismatch in thermal expansion coefficient between interconnect and substrate, coupled with the temperature difference within a power cycle, causes strain to be applied to the interconnect.

In terms of fatigue testing, the mechanical stress amplitude depends on the magnitude of the cyclic current density. Current densities in the range used here result in temperature changes of approximately 100 K, measured by means of time-resolved electrical resistance measurements [6]. Further experiments are underway to measure line temperatures using thermal scanned probe microscopy. The ratio of the minimum to the maximum mechanical stresses, *i.e.*, the fatigue R-value, can be varied by controlling the rms temperature of the test specimen through substrate heating or cooling. This would allow for tests encompassing tension-tension, compression-compression, or fully reversed tension-compression loading. Analyses of the temperature dependence of cyclic current flow and the frequency dependence of cyclic heat flow have also been completed in reference [6].

We are exploring how electrical testing can be used to measure other mechanical properties of thin films and interconnects. One such possibility is to estimate the ultimate tensile strength by determining the fatigue ductility coefficient through the Coffin-Manson relation for prediction of low cycle fatigue lifetime. That electrical approaches for extracting mechanical response are feasible is supported by comparing TEM observations on AC-tested interconnects with those from fracture tip regions of films deformed by microtensile testing [7]. For both cases, a higher density of prismatic dislocation loops was observed after testing, as compared to that seen in the as-deposited structures. A high density of dislocation segments was *not* seen in these specimens after testing, however. This suggests a high incidence of dislocation intersections occurring during both types of testing, with primarily glissile segments likely leaving the interconnect surfaces, or gliding to interfaces such as grain boundaries or the film/substrate interface. We are beginning a series of *in situ* TEM studies to confirm this hypothesis.

Thermomechanical Fatigue of Al-1Si Interconnects

Damage evolution in Al-1Si as documented by SEM and EBSD exhibited heterogeneous behavior typical of cyclic plastic deformation in polycrystalline face-centered cubic (fcc) metals. In particular, surface topography was observed to occur in only selected regions of stressed lines, and only certain grains showed growth and reorientation. Deformation taking place in only certain grains is consistent with variations in resolved shear stress and initial grain size, as suggested by our approximate Schmid factor and grain size observations. Reorientation is consistent with a recent analysis of slip asymmetry in cyclic deformation of fcc crystals [8], which showed that for the case of fully reversed loading, a single crystal reorients such that during the tensile half-cycle, the loading axis rotates towards the primary slip direction, [011], and during the compressive half-cycle, it rotates towards the normal to the primary slip plane, $(1\bar{1}1)$. The net result of this ratcheting action is an ultimate crystal orientation near (113). Some data points in figure 4 have reached (113), while others have not after 1.4 x 10^5 strain cycles.

We suggest that plasticity becomes especially pronounced in grains where a combination of the following factors can favor significant dislocation activity: (i) the resolved shear stress on preferred crystallographic slip systems exceeds the average such value for the entire polycrystalline aggregate; (ii) starting grain size is sufficiently large to exhibit low yield strengths; and (iii) dislocations may be easily nucleated, based on the availability of likely sources such as grain boundaries with highly random structure. This combination of factors, encompassing resolved stress, ease of slip, and likelihood of dislocation formation is being used to formulate a predictive model for failure initiation in AC-stressed lines. We are attempting to identify *a priori* which grains are the most susceptible to significant localized plasticity, and would therefore exhibit the greatest likelihood for reduced specimen cross-section. It is this population of grains that would be most likely to fail by open circuit.

ACKNOWLEDGMENTS

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REFERENCES

1. F. R. Brotzen, *Int. Mater. Rev.* **39**, 24 (1994).
2. W. D. Nix, *Mater. Sci. Eng.* **A234**, 37 (1997).
3. F. R. N. Nabarro, *Theory of Crystal Dislocations*, 2nd ed. (Dover Publications, New York, 1987) pp. 618-641.
4. M. Huang, Z. Suo, and Q. Ma, *J. Mech. Phys. Sol.* **50**, 1079 (2002).
5. R. R. Keller, R. Mönig, C. A. Volkert, E. Arzt, R. Schwaiger, and O. Kraft, in *6th International Workshop on Stress-Induced Phenomena in Metallization*, edited by S. P. Baker, M. A. Korhonen, E. Arzt, and P. Ho, (AIP Conference Proceedings **612**, American Institute of Physics, New York,2002) pp. 119-132.
6. R. Mönig, R. R. Keller, and C. A. Volkert, *Rev. Sci. Instrum.* **75**, 4997 (2004).
7. R.H. Geiss, R.R. Keller, D.T. Read and Y.-W. Cheng, this proceedings (2005).
8. Li, Li, Zhang, Wang, and Lu, *Phil. Mag.* **A82**, 3129 (2002).