A NEW FABRICATION PROCESS FOR PLANAR THIN-FILM MULTIJUNCTION THERMAL CONVERTERS

T. F. Wunsch*, J. R. Kinard**, R. P. Manginell*, O. M. Solomon*, and T. E. Lipe**

*Sandia National Laboratories
PO Box 5800
Albuquerque, NM 87185-0665

**National Institute of Standards and Technology
100 Bureau Drive
Gaithersburg, MD 20899-8111

Abstract

Advanced thin film processing and packaging technologies are employed in the fabrication of new planar thin-film multijunction thermal converters. The processing, packaging, and design features build on experience gained from prior NIST demonstrations of thin-film converters with optimizations for improved sensitivity, bandwidth, manufacturability, and reliability.

Introduction

Recent efforts at NIST and PTB have focused on developing novel designs of Multijunction Thermal Converters (MJTCs) in thin-film fabrication technologies [1,2]. The thin-film construction shows promise for producing a large number of high quality MJTCs at relatively low cost. The most significant advantage of the thin-film device is that the difficulties encountered in manual construction of conventional wire MJTCs are completely replaced by highly reproducible metal sputtering, photolithographic patterning and subsequent etching. Despite many advances, a number of difficulties exist in producing thin film thermal converters.

A thin film MJTC is comprised of a resistive heater and proximately placed thermocouples that sense any difference in temperature between dc and ac excitation. The heater and thermocouple hot junctions are constructed on a thin-film dielectric membrane that provides thermal isolation from the substrate. In this paper, new processing and vacuum packaging methods will be described. These methods alleviate some of the inherent difficulties in fabrication. Specifically, a description is given of 1) a low stress silicon nitride dielectric membrane, 2) a lift off technique for improved feature patterning, 3) a new Bosch etching process employed for back-etching of the membrane and definition of a silicon obelisk, and 4) an advanced vacuum packaging method.

Thermal Converter Fabrication

The heater structure is optimized through numerical thermal simulation and designed to provide a uniform temperature distribution across the central region where 100 thermocouple pairs are connected in series. The heater is of NiCrAlCu alloy† ($w_{Cr} = 0.2$, $w_{Al} = 0.025$, $w_{Cu} = 0.025$) for voltage converters. This alloy composition results in thermoelements with a very low temperature coefficient of resistance on the order of 10 $(\mu\Omega/\Omega)/°C$. Thermoelements with gold heaters are also constructed for use as current converters. The use of gold as the heater, bond-wire, and package lead completely eliminates any Peltier heating in the device. All devices fabricated use thermocouples of CuNi alloy ($w_{Ni} = 0.45$) for the negative leg and NiCr alloy ($w_{Cr} = 0.1$) for the positive leg. The Seebeck coefficient for a thermocouple pair is approximately 65 $\mu V/°C$. Gold bond pads are formed at the input/output of the heater and multijunction thermocouple.

The use of sputtered metals provides uniformity in composition of the deposited thin-film thermocouples and heater. Wet chemical etching steps are eliminated through the use of a photoresist lift-off. This technique, widely utilized for evaporated metals, results in well-defined features and a reduction in processing steps.

Backside Processing

Among the troublesome difficulties in fabrication is the production of the freestanding dielectric membrane. Silicon dioxide and silicon nitrides are known to produce high-stress thin films. The stress in these films is often enough to cause breakage on formation of the freestanding membrane by wet chemical back etching. Previous designs have used a "sandwich"

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†Alloy compositions are noted as follows: the primary alloy constituent is noted first and w_B is the mass fraction of the alloy constituent B.

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ide/nitride/oxide deposition to compensate for the ternal stress of the nitride dielectric [1,2]. This proach has been successful in improving yield. In this udy, we propose a simpler technique employing ommercially available silicon substrates with a 5000 Å w stress nitride film followed by a Bosch‡ etch lescribed below). The improved yield indicates that this ıethod has produced stronger freestanding membranes ıan the dielectric sandwich membrane technique.

Removal of silicon below the heater and thermocouple ıot junctions provides a thermally isolated membrane and is the key step in producing a thermal converter. Following patterning, a deep reactive ion etching process (DRIE) is employed. The patented DRIE process [3] utilizes an iterative inductively coupled plasma-based deposition/etch cycle in which a polymer etch inhibitor is conformally deposited over the wafer during the deposition cycle. The polymer deposits over the resist mask, the exposed silicon field, and along the sidewall of the feature to be etched. The polymer film is preferentially sputtered from the silicon trench perpendicular to the surface of the wafer. The polymer film on the sidewall is removed at a much slower rate, minimizing lateral etching of the silicon.

To form a silicon obelisk, a sacrificial dielectric layer is patterned beneath the heater. The relative etch ratio of the Bosch DRIE process for $Si:Si_3N_4$ allows control of the obelisk geometry and thermal time constant.

Vacuum Packaging

Under vacuum, thermal converters exhibit an increase in sensitivity and an increase in thermal time constant. An advanced vacuum packaging process is employed in sealing the fabricated devices in a leadless chip carrier (LCC) ceramic package under vacuum. The process utilizes a commercial high vacuum hermetic sealer and film getters composed of a NiCr ribbon covered with a porous mixture of Ti and ZrVFe alloy [4]. The getters are soldered to the package lids and allow the vacuum in the package to be maintained below levels where convective heat loss is significant.

Performance Characteristics

Several thermal converters have been compared against NIST working standards. The new process has produced devices with relatively low ac-dc differences and high sensitivities. As an example, a preliminary set of data taken at 3 V is shown in Figure 1 for a 980 Ω thermal voltage converter (TVC) along with a set of data taken at 50 mA for a 5 Ω thermal current converter (TCC). The short thermal time constants produce significant low frequency errors that are reduced in thermal converters with the obelisk.

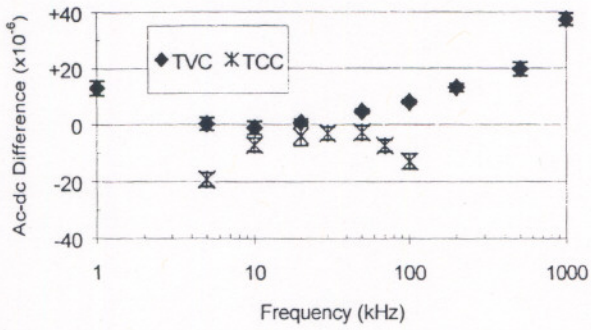

Figure 1. Preliminary ac-dc difference data for a thin-film TVC at 3 V and a thin-film TCC at 50 mA. Error bars are the k = 2 Type-A uncertainty of the comparison to NIST standards.

A variety of devices have been constructed and are currently under characterization. A more comprehensive evaluation of these devices will be provided.

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[3] Patent No. 5501893: Method of Anisotropically Etching Silicon, Inventors: Franz Laermer and Andrea Schilp of Robert Bosch GmbH, Issued March 26, 1996.

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‡ Identification of commercial equipment, instruments, and/or materials does not imply recommendation or endorsement by NIST or Sandia, nor does it imply that the material or equipment identified is necessarily the best available for the specified purpose.