AC Power Standard Using a Programmable Josephson Voltage Standard

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***Abstract*—This paper describes the implementation of a new quantum-based system for the generation of 120 V RMS, 5 A RMS, sinusoidal, active, and reactive power over the 50 to 400 Hz frequency range. The system accurately relates the spectral amplitudes and phases of the voltage and current waveforms of the generated power to a programmable Josephson voltage standard (PJVS) by using a novel differential sampling technique. The system also employs a new voltage amplifier that performs self-calibration and corrections of the gain and phase errors. Details of the system design, measurement techniques, and significant sources of error are presented.**

***Index Terms*—Analog–digital conversion, current measurement, digital–analog conversion, Josephson arrays, permuting capacitance, power measurement, quantization, signal synthesis, voltage measurement.**

I. Introduction

THE HIGHEST accuracy calibrations of standard wattmeters and watthour meters at power frequencies at the National Institute of Standards and Technology (NIST) are presently based upon the bridge technique [1]. The basic uncertainty of these measurements is within 15 μW/VA $(k = 1)$, and with considerable effort, we can achieve an uncertainty of 7 μW/VA $(k = 1)$. While these uncertainties remain more than adequate for the calibrations of the best revenue power and energy meters, several factors have recently made it necessary to develop a new standard for power generation. These factors include improved calibration efficiency and traceability to the SI units, reduced maintenance costs, and an increasing demand by meter and transformer manufacturers to provide calibration uncertainties that approach 1 μW/VA.

To achieve these goals, a quantum-based power generation system and differential sampling measurement techniques were developed [2]–[4]. The present system configuration is shown in Fig. 1, where a single piecewise-approximated programmable Josephson voltage standard (PJVS) waveform V_J is compared to two stable spectrally pure waveforms V_V and V_I, which are scaled versions of the voltage and current signals applied to the meter under test (MUT). The resulting differential waveforms are measured with two commercially available sampling digital voltmeters (DVMs) by selectively ignoring the values in the acquired data sets that correspond to the time periods in which the PJVS signal is changing state [3]. Realizing the potential accuracy of this sampling approach requires a high-performance signal generator; a new multichannel generator was developed featuring low amplitude and phase noise, low distortion, and 24 bit amplitude/phase resolution. In addition, it was necessary to develop a new voltage amplifier to accurately scale one of the PJVS-derived signals to 120 V RMS. An accurate temperature-controlled current shunt [5] with a three-stage active voltage transformer [6] was also developed to measure the applied current in the presence of large common-mode signals. The residual uncertainty of the system at 60 Hz is less than 2 μW/VA $(k = 1)$.

The system will be used to provide calibrations of the standard power and energy meters at 120 V RMS and 5 A RMS over the 50 to 400 Hz frequency range as well as serve as the basis for international comparisons of power measurements between NIST and other national metrology institutes.

II. Measurement System

Descriptions of the key system components are given hereinafter along with their significant sources of error.

A. Sampling DVMs

The system employs two DVMs that operate in their dc-voltage (DCV) sampling mode on their lowest (100 mV) input range. An isolated digital receiver circuit was added to the analog-to-digital converter (ADC) board of each DVM to allow the ADC reference oscillators to phase lock with an external 20 MHz reference that is supplied by the multichannel signal generator. Included in Fig. 1 are examples of the scaled voltage V_V, scaled current V_I, and multimode PJVS V_J signals that illustrate how only 1/2 of the differential DVM measurements are actually used (the bold intervals of the V_J signal). The remaining 1/2 of the samples contain the unwanted PJVS transitions and settling artifacts (greatly exaggerated in Fig. 1) and are discarded. For illustration purposes, the V_J signal shown in Fig. 1 contains 4 steps/cycle/waveform, but in general, it has at least 64. The sampling DVM is thereby used as a phase-locked, differential-mode, time-multiplexed, and time-selective null detector, where the effects of its ADC linearity errors, input circuitry bandwidth, and integration-time filtering are minimized.

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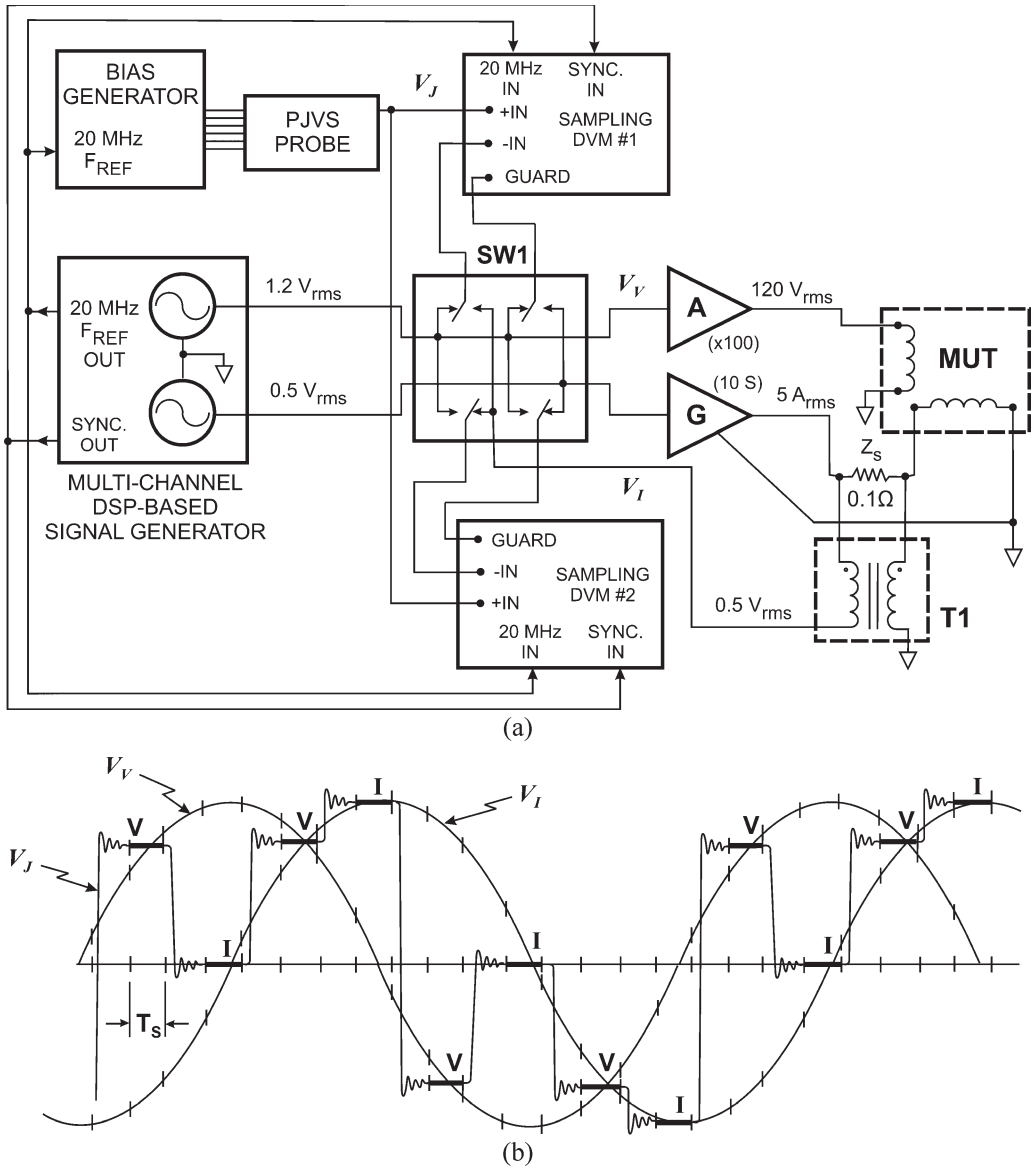

Fig. 1. Quantum-based power generation system. (a) Simplified diagram, including sampling DVMs operating in the differential voltage sampling mode. (b) How a single PJVS waveform V_J is used to provide reference levels for the differential sampling of the two scaled voltages V_V and V_I. The bold intervals of V_J represent the sampling intervals of interest; the remaining sampling intervals are ignored.

The reduced sets of sampled differential data are then processed by first adding the corresponding V_J values to the differential data, thereby reconstructing the sampled values of the original waveforms, and then applying a modified three-parameter sine fit algorithm [7] (amplitude, phase, and dc offset for each frequency component of the waveform) that includes additional degrees of freedom to estimate the mains-frequency power-line interference, yielding accurate frequency-domain representations of the sinusoidal V_V and V_I waveforms. Both channels of the signal generator are then adjusted with a 24 bit precision in amplitude and phase to minimize the difference (in terms of the amplitudes and phases of the fundamental and first ten harmonics) between the desired and measured V_V and V_I signals, which results in the accurately known amplitudes and relative phases of the V_V and V_I generated waveforms. In general, the signal generator harmonics are negligible for sinusoidal power applications but are included in this system for applications that require voltage and current signals with known harmonic content.

This measurement technique relies on the common-mode rejection performance of the DVM at the nominal acquisition configuration (sample rate, integration time, and input range setting) for each frequency. The common-mode rejection was tested by connecting the signal generator to both inputs of the DVM and has been determined to be less than one part in 10^7 at 60 Hz, less than four parts in 10^7 at 300 Hz, and less than two parts in 10^6 at 400 Hz, where a reduced number of V_J samples/period require that the ADC no longer operate in its lowest input range to avoid the ADC input overload. The ADC integration-time independence of the technique has also been verified at 50 Hz by using a stable thermal voltmeter, which detected no amplitude variations in the V_V waveform within the measurement noise of approximately one part in 10^7 when the ADC integration time was varied over the range from

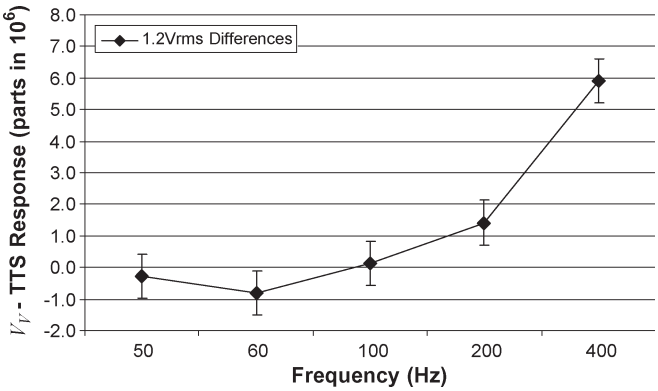

Fig. 2. Measured differences between the 1.2 V RMS PJVSderived V_V signal and a calibrated TTS.

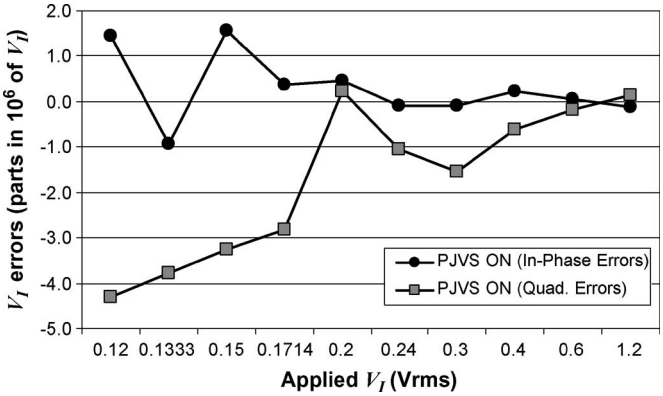

Fig. 3. PJVS-derived V_V/V_I ratio accuracy tests measured using a permuting capacitance divider. The V_V signal was set to 1.2 V RMS (DVM range = 100 mV).

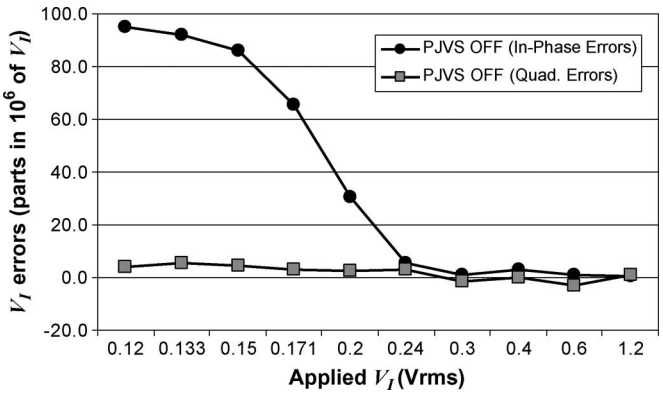

Fig. 4. Non–PJVS-derived V_V/V_I ratio accuracy tests measured using a permuting capacitance divider. The V_V signal was set to 1.2 V RMS (DVM range = 10 V).

4.47 to 22.3 μs. Similar results for the larger changes in ADC integration times are given in [3].

The initial investigations of the time-multiplexed acquisition approach indicated that the value of each sample was dependent upon whether the ADC was overloaded on the previous sample. A modified approach that organizes the V_J signal data record into bursts of several cycles of V_V data, followed by several cycles of V_I, was, therefore, devised. It was empirically determined that if the samples from the first 15 ms of each burst are discarded, then the overload dependency between samples becomes an insignificant source of error for this application. For additional details of this technique, see [3].

A check of the generated 1.2 V RMS V_V signal was performed by comparing it against a calibrated thermal transfer standard (TTS). The results of this test are given in Fig. 2, with the error bars representing the ac voltage measurement uncertainty $(k = 1)$ of the TTS. The results indicate that, within the uncertainty of the measurements, the PJVS-derived V_V signal is within one part in 10^6 $(k = 1)$ of the nominal over the 50 to 100 Hz frequency range. As with the common-mode rejection test previously described, the 400 Hz data point in Fig. 2 was measured by using a PJVS-derived V_V signal with the sampling DVM on the 1 V range instead of the usual 100 mV range due to ADC input overloading at the 400 Hz slew rate.

An analysis of the PJVS-derived V_V/V_I ratio accuracy was performed by connecting the V_V and V_I signals to a permuting capacitance divider. For more details about the permuting capacitance divider, see Section II-C. For these measurements, the V_V signal was set to 1.2 V RMS, and the V_I signal was set to 180° out of phase with V_V and varied from 0.12 V RMS to 1.2 V RMS. A permuting capacitance divider was then used to measure the in-phase and quadrature errors of the PJVS-derived V_V/V_I ratio. In addition, the same tests were performed with the PJVS system turned off $(V_J = 0)$ to determine the ratio accuracy of the DVMs when in normal (nondifferential) sampling mode. The results of these tests are shown in Figs. 3 and 4 for the PJVS on and PJVS off cases, respectively. The results suggest that the differential sampling approach yields accurate results even for large (10/1) signal ratios. It should, therefore, be feasible to use the quantum-based power system to generate voltages and currents over a wide dynamic range relative to 120 V RMS and 5 A RMS.

B. Multichannel DSP-Based Signal Generator

The accuracy of the sampling approach depends on the assumption that the sinusoidal signals to be measured have an amplitude and phase precision of better than one part in 10^6, high initial spectral purity, and low amplitude and phase noise over a wide bandwidth to avoid aliasing errors. A new multichannel DSP-based signal generator was developed to meet these demands and features sigma–delta digital-to-analog converters (DACs) with 24 bit amplitude and phase resolution, low distortion, real-time computation of up to 20 harmonics of waveform data/channel, and both optical and digital inputs and outputs for system timing. The signal generator receives a 10 MHz reference clock from an external frequency source and then generates all the necessary timing signals for the remaining instruments in the system. One drawback of the sigma–delta DACs is that they generally have relatively large gain–temperature coefficients as compared to the R-2R ladder or CMOS DACs. After a 1 h warm-up period, the gain drift of the generator is random and dominated by the random fluctuations of temperature in and around the sigma–delta DAC integrated circuit (IC). The gain drift is continuously cancelled in software but leads to higher standard deviations in the measurement data that must be averaged out.

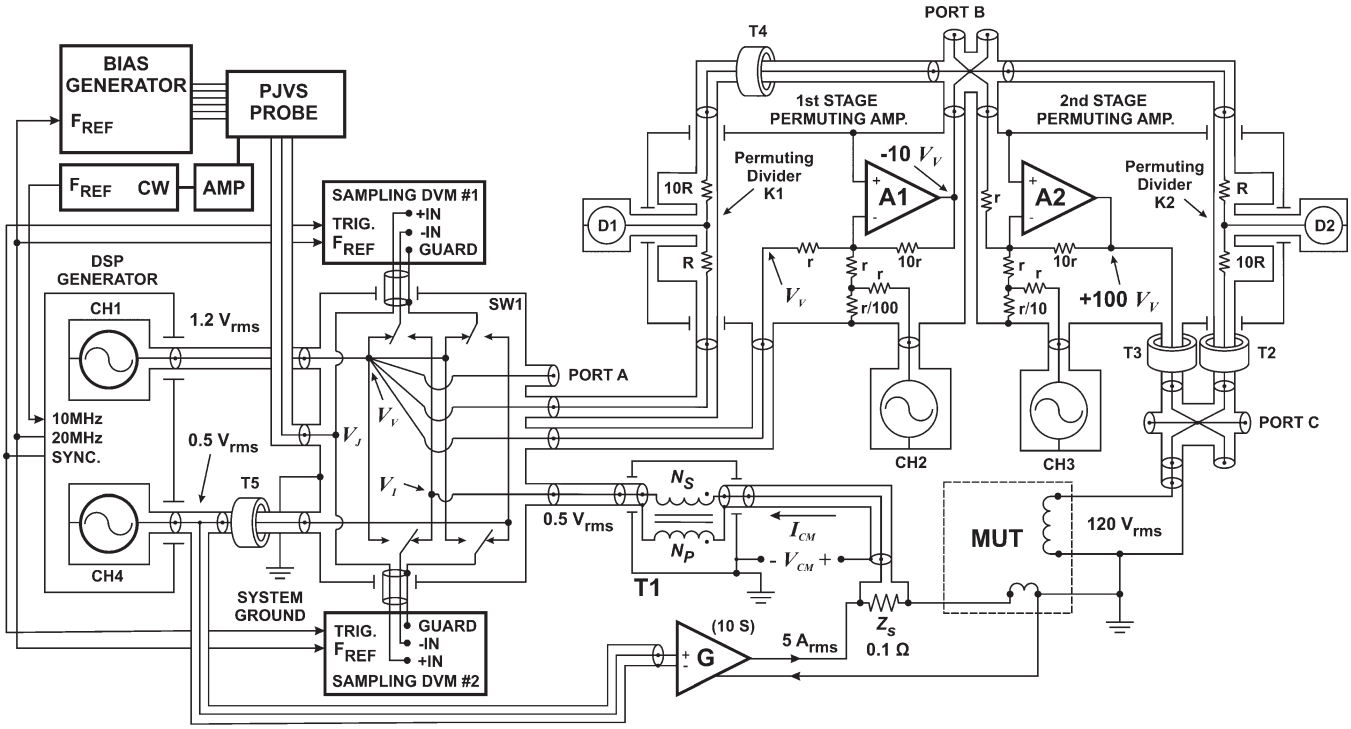

Fig. 5. Detailed diagram of the quantum-based power generation system detailing the permuting amplifier design and component interconnection requirements.

C. Voltage Amplifier

The voltage amplifier A in Fig. 1 consists of two $-10:1$ inverting amplifier stages, where the input and output of each stage are connected to a corresponding permuting divider, i.e., an 11-element relay-switched array of 1 MΩ thin-film resistors with low temperature and voltage coefficients.

A more detailed diagram of the quantum-based system is given in Fig. 5, which illustrates the hardware details and interconnection requirements for the various amplifier components. The 11 resistors in each permuting divider, which are labeled K1 and K2, respectively, in Fig. 5, have a low thermal resistance path to their brass enclosure and are connected to a common "star" or null point. The resistors are nominally arranged so that one of the resistors is connected to the amplifier output and the remaining ten are connected in parallel to the amplifier input, creating a resistive divider with a nominally zero potential output tap. For each amplifier stage, the null voltages are measured by using two additional sampling DVMs (shown in Fig. 5 as D1 and D2, respectively) for each of the 11 possible series/parallel resistance permutations. It can be shown that when the vector sum of each set of 11 null voltages is equal to zero, then each amplifier stage has an inverting gain of exactly $-10:1$, which yields a composite gain of exactly $100:1$. For more details on this technique for defining the voltage ratio, see [8] and [9].

Each amplifier stage incorporates a separate summing input that is connected to an additional channel of the multichannel signal generator (shown in Fig. 5 as CH2 and CH3, respectively). These signals bring the fundamental and the first ten harmonics of the vector sums to zero, thereby reducing the amplifier's gain errors, phase errors, and distortion. The gain and phase errors of each of the K1 and K2 dividers of the amplifier have been determined over the 50 to 400 Hz frequency range

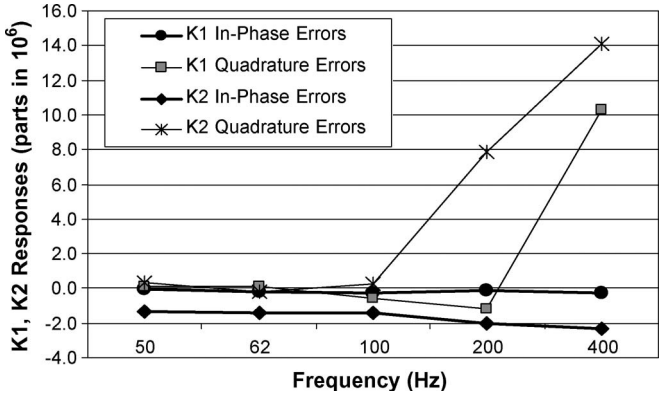

Fig. 6. K1 and K2 permuting divider responses as measured against a permuting capacitance reference divider.

by comparing each stage to a permuting capacitance divider consisting of 11 relay-switched fused-silica capacitance standards all with nominal values of 99.99995 ± 0.00002 pF. The voltage coefficient of the fused-silica permuting capacitance divider has been determined to be less than two parts in 10^8 from 10 V RMS to 200 V RMS at 1592 Hz by comparing it to a temperature-controlled reference capacitive divider consisting of 11 nitrogen-dielectric capacitors with known low loss. To test the first-stage (K1) divider, the permuting capacitance divider was connected at the PORT A and B terminals of Fig. 5. To test the second-stage (K2) divider, the permuting capacitance divider was connected at the PORT B and C terminals of Fig. 5. The results of these tests on the K1 and K2 dividers are shown in Fig. 6. The errors are expressed in parts in 10^6 of the nominal full-scale ratio (FSR) $(k_{\mathrm{nom}} = 10.0)$ so that for each stage of the amplifier an error in k of one part in 10^6 would represent an uncorrected amplifier gain of 10.00001.

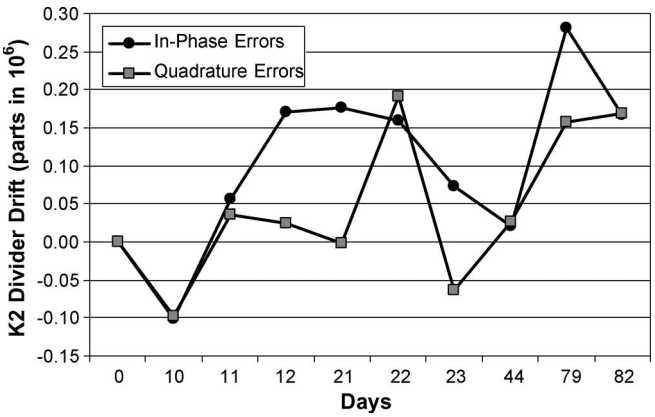

Fig. 7. Stability analysis of the K2 divider errors versus a permuting capacitance divider.

It is evident from Fig. 6 that the K1 and K2 permuting dividers exhibit different in-phase error responses that can be attributed to their relative voltage operating points. The K2 in-phase errors include appreciable components due to the voltage and power coefficients of the permuting divider resistors. The K1 and K2 dividers exhibit relatively large and different quadrature error responses due to the fact that they are operated under nonideal (biased) null conditions, as discussed below.

It is crucial to understand that the stated K1 and K2 divider errors do not represent the errors of the voltage amplifier. For each amplifier stage, the permuting capacitance calibration procedure determines both the K1 or K2 divider errors and the required null bias voltage that, when added to the K1 or K2 vector sum null, results in the cancellation of the amplifier errors and thus brings the permuting capacitance divider to a vector sum null. This is a consequence of the fact that the permuting capacitance divider is only accurate when operated at a vector sum null, so the K1 and K2 dividers are always operating under nonideal (biased) null conditions, which shows up at higher frequencies as rather large apparent phase errors in Fig. 6. The addition of the calculated null bias injections reduces the effect of the K1 and K2 divider errors on the corresponding amplifier stage by about a factor of 20, as determined by the residual permuting capacitance imbalance signal after a calibration sequence. The software maintains a database of the required null bias voltages for each amplifier stage at each operating frequency.

A stability analysis of the calculated K2 divider errors was performed over a three-month period to determine the suggested calibration intervals for the permuting amplifier against a permuting capacitance divider. The results of this analysis are given in Fig. 7 and indicate that the K2 divider changed less than four parts in 10^7 over the duration of the test. This would suggest a calibration interval of about 9–12 months to ensure that the voltage amplifier errors remain below one part in 10^6.

Additional tests were performed on the voltage amplifier to determine its sensitivity to various loads. The results of these tests indicated that for severe loads (several wattmeters connected simultaneously, for instance), the amplifier gain could shift as much as 7 μrad in phase at 60 Hz. This phase shift was caused by ground loops and is reduced to less than 1 μrad by the use of passive current equalizers T2, T3, T4, and T5, as shown in Fig. 5.

It is estimated from the measurement results that the type B uncertainty [10] in the gain of the first-stage amplifier k_1 is less than four parts in 10^7 at 60 Hz. The type A uncertainty in k_1 of six parts in 10^7 at 60 Hz is due to the combination of the divider K1 drift and the measurement uncertainty in the D1 null readings. The type B uncertainty of the second-stage gain k_2 is estimated to be less than five parts in 10^7 at 60 Hz. The type A uncertainty in k_2 of less than eight parts in 10^7 is due to the divider K2 drift and the residual loading errors. Combining these uncertainties, the results indicate that for a perfect 1.2 V RMS V_V input signal at 60 Hz, the 120 V RMS output of the amplifier is in error less than 1.2 parts in 10^6 $(k = 1)$. The key features of this amplifier are that it has an effective zero output impedance, and it provides an accurate 100 : 1 gain down to dc, thereby providing "quantum-based" dc voltages to 120 V.

D. Channel-Reversing Switch

Instead of using a single sampling DVM and a switch to alternately sample the V_V and V_I signals, a dual-channel switch (SW1 in Fig. 1) with dual DVMs was deemed necessary to avoid possible changes in either V_V or V_I when one was deselected. The chosen switch arrangement also ensures that both signals are sampled on similar cycle segments of the power-line interference. The switch crosstalk is below one part in 10^7 at 1.2 V RMS, 60 Hz.

E. Transconductance Amplifier

A new transconductance amplifier G in Figs. 1 and 5 was developed for this system; it features a 10 A/V transconductance gain, low noise, low distortion, low gain and offset drift with temperature, high output impedance, and fully differential high-input impedance $(> 500\ \text{k}\Omega)$ input circuitry to minimize the ground-loop-induced errors. A full description of this amplifier is to be presented in a future publication.

F. Current-to-Voltage Transducer

The 5 A RMS applied current is converted to 0.5 V RMS by using a temperature-controlled current shunt [5] (Z_S in Fig. 5) with a three-stage active voltage transformer [6] (T1 in Fig. 5) to reject the common-mode voltages present at the shunt output (V_{CM} in Fig. 5), which results in a ground-referenced signal V_I. The errors of the current transducer can be separated into the errors due to the shunt Z_S and to the voltage transformer T1. The ratio of T1, i.e., $N_S/N_P = 1$, is tested *in situ* by connecting the marked terminal of T1's secondary winding N_S to the marked terminal of the primary winding N_P, thus shorting both inputs to the low terminal of Z_S, whereas Z_S is under full rated current, and a MUT, or some other suitable impedance, is present to generate an adequate common-mode voltage V_{CM} across T1's primary and secondary windings. The residual voltage present at T1's output terminal (V_I in Fig. 5) is a measure of T1's ratio error. The measured ratio errors of T1 over the 50 to 400 Hz frequency range are given in Table I.

TABLE I
TRANSFORMER T1 RATIO ERRORS

F (Hz)	In-Phase (μV/V)	Quadrature (μV/V)
50	+0.09	+0.12
62	+0.09	+0.13
70	+0.11	+0.14
80	+0.12	+0.13
90	+0.13	+0.15
100	+0.14	+0.16
200	+0.18	+0.23
400	+0.25	+0.38

The results in Table I indicate that for $V_{\rm CM} < 1$ V RMS ($V_{\rm CM}$ is usually below 0.3 V RMS), the ratio errors of T1 contribute less than three parts in 10^7 to the total current transducer error.

The leakage resistance and inductance of T1's N_P and N_S windings and the capacitance between N_P and N_S act as a distributed RLC filter, which causes errors in the ground-referenced shunt output voltage V_I that must be measured and corrected. These errors are measured *in situ* by disconnecting T1's input from the shunt output and temporarily connecting T1's input to PORT A of SW1 in Fig. 5. The V_V signal is set to 0.5 V RMS, and the resulting measured V_I/V_V signal ratio represents the transfer function of the RLC filter. These errors are compensated for in software with residual uncertainties of less than three parts in 10^7 at 60 Hz.

Due to its three-stage design that minimizes the magnetizing current in the primary winding [6], the high input impedance of T1 minimizes any leakage current from the applied current path to ground (I_{CM} in Fig. 5). The input impedance of T1 was measured *in situ* by inserting a current comparator [11] with coaxial ratio windings in series with the shunt output and T1's input. First, a phase-sensitive detector was used to measure the current comparator's output voltage with T1's N_S winding disconnected from the V_I node in SW1 (see Fig. 5), which only leaves T1's magnetizing current flowing in the current comparator's remaining winding. Using the current comparator's known 100 μV/μA sensitivity and the measured $V_{\rm CM}$, the input impedance of T1 was measured to be 3.4 MΩ (780 pF) at 60 Hz. Finally, T1's N_S winding was connected to the V_I node in SW1, allowing the current to flow in the current comparator's other ratio winding. Any difference between the two measured currents represents the input current of the DVM and, therefore, the DVM's input impedance when driven in the differential mode. The difference current indicates a differential-mode DVM input impedance of approximately 87 MΩ at 60 Hz, which is an insignificant load on the shunt. The capacitance between T1's N_P and N_S windings was measured to be approximately 11.5 nF at 60 Hz. This represents an impedance that is in parallel with the shunt impedance Z_S and causes a 0.45 μrad phase error in the shunt at 60 Hz, increasing to 2.9 μrad at 400 Hz. This shunt loading is compensated for in software when calculating the shunt's ac impedance from the correction equations in [5].

The shunt's ac–dc resistance change over the dc to the 400 Hz frequency range is less than 0.04 $\mu\Omega/\Omega$ with an uncertainty of 0.05 $\mu\Omega/\Omega$ $(k = 1)$. The uncertainty of the determination of the shunt's time constant is 0.16 ns $(k = 1)$, which results in a 60 Hz phase uncertainty of less than 0.06 μrad $(k = 1)$. The temperature control circuitry of the shunt limits the changes of its dc resistance to less than 1.1 $\mu\Omega/\Omega$ for the applied currents from 0.3 to 10 A. In addition, the uncertainty in the dc measurement at rated currents of the shunt, traceable to the quantum Hall, is 0.25 $\mu\Omega/\Omega$ $(k = 1)$. The shunt has been calibrated at regular intervals over the last four years and has drifted less than 1 $\mu\Omega/\Omega$.

TABLE II
UNCERTAINTY COMPONENTS (PARTS IN 10^6)

Parameter	Type B In-Phase	Type B Quadrature	Type A
V_V	$\alpha_1 = 0.4$	$\beta_1 = 0.6$	0.1
V_I	$\alpha_2 = 0.5$	$\beta_2 = 0.8$	0.1
k_1	$\alpha_3 = 0.4$	$\beta_3 = 0.4$	0.6
k_2	$\alpha_4 = 0.5$	$\beta_4 = 0.5$	0.8
Z_S	$\alpha_5 = 0.5$	$\beta_5 = 0.2$	0.3
T1 (N_S/N_P, RLC)	$\alpha_6 = 0.2$	$\beta_6 = 0.4$	0.2

The errors associated with the shunt previously discussed are all compensated for in software so that the uncertainties in the errors of the current-to-voltage transducer are dominated by the shunt's dc resistance drift rate and the uncertainty of its dc calibration. At 60 Hz, the residual magnitude and phase errors of the current-to-voltage transducer output voltage at full-scale 5 A RMS input current are estimated to be less than 0.5 μV/V $(k = 1)$ for a dc resistance calibration interval of one year and a $V_{\rm CM}$ of less than 0.5 V RMS.

III. ERROR ANALYSIS

The uncertainty in the power applied to a MUT depends on the type A and B uncertainties of the applied voltage V_V, the gain of each stage of the voltage amplifier $k1$ and $k2$, the sensed current transducer voltage V_I, the ratio of T1 (N_S/N_P), and the impedance of the shunt Z_S. Estimates of the type A and B uncertainties of these parameters at 120 V RMS, 5 A RMS, 60 Hz are given in Table II. Provided that all the type B quadrature uncertainties are small, an expression for the active power P applied to a MUT is given by

$$\begin{aligned} P \approx\ & [V_V(1 \pm \alpha_1)k_1(1 \pm \alpha_3)k_2(1 \pm \alpha_4) \\ & \ldots V_I(1 \pm \alpha_2)(N_S/N_P)(1 \pm \alpha_6)/Z_S(1 \pm \alpha_5)] \\ & \ldots \cos(\theta \pm \beta_1 \pm \beta_2 \pm \beta_3 \pm \beta_4 \pm \beta_5 \pm \beta_6). \end{aligned} \quad (1)$$

The maximum type B uncertainty in P at any power factor U_M may be expressed as

$$\begin{aligned} U_M = \pm\, & [(\alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 + \alpha_5 + \alpha_6)\cos\theta \\ & \cdots + (\beta_1 + \beta_2 + \beta_3 + \beta_4 + \beta_5 + \beta_6)\sin\theta]. \end{aligned} \quad (2)$$

It is unlikely that the total uncertainty U_P will exceed the root-sum-squared (rss) value of the components in U_M and the type A components in Table II. Substituting from Table II, we have

$$U_P = [1.11\cos^2\theta + 1.61\sin^2\theta + 1.15]^{1/2}. \quad (3)$$

The U_P uncertainty $(k = 1)$ at 120 V RMS, 5 A RMS, 60 Hz for various phase angles is given in Table III.

TABLE III
TOTAL ACTIVE POWER UNCERTAINTIES (PARTS IN 10^6)

0°	30°	60°	90°
1.5	1.5	1.6	1.7

IV. CONCLUSION

A quantum-based system for the generation of ac power has been described. Uncertainties approaching 1 μW/VA $(k = 1)$ have been achieved. The largest contributions to the uncertainty of the applied power are due to the residual type A uncertainties in the determinations of the amplifier gain. The type A estimates stated here are the result of only a very few statistical samples. Additional tests are underway to more accurately determine these quantities.

An additional check of the new system was performed by comparing it to the power bridge described in [1]. First, the various components of the power bridge were calibrated to determine the updated correction coefficients. The quantum-based power generation system was used to generate the voltage and current signals with known amplitude and phase relationships that were then applied to the power bridge. The difference between the active power defined by the quantum-based power generation system and the active power necessary to balance the power bridge was measured to be less than 2 μW/VA at unity and zero power factors, 120 V RMS, 5 A RMS, 60 Hz. Additional tests between the two systems are underway at various operating voltages, currents, and power factors.

Further work in this area that is intended to provide a more complete support for the present NIST power calibration services includes the development of a second-generation permuting impedance voltage amplifier with 600 V RMS output capabilities.

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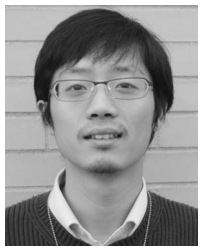

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Dr. Dresselhaus received a U.S. Department of Commerce Gold Medal for Distinguished Achievement and the 2006 IEEE Council on Superconductivity Van Duzer Prize.