# MODELING AND TEST POINT SELECTION FOR DATA CONVERTER TESTING

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## Abstract

Methods for generating efficient testing strategies for data converters are presented. Linear modeling techniques based on circuit analysis and empirical test data are included, as well as algorithms for selecting optimal test points. Using these tools, converter errors can be accurately estimated for all code states from a relatively small number of measurements.

## 1. Introduction

Because of the large number of discrete states possible, the testing of data converters can pose serious problems. This is particularly true for higher resolution devices for which precision analog measurements are required. As with large digital circuits, the time requirements for exhaustive testing can be prohibitively expensive, suggesting the need for more efficient testing strategies. This paper presents techniques and analytic tools with which efficient testing strategies can be developed. These methods address techniques for developing accurate error models, for selecting optimal test points, and for estimating the coefficients of the model from the limited measurement data.

## 2. Approach

### Modeling

In order to deduce the overall performance of a device from limited test data, an accurate error model is required; otherwise, completely exhaustive testing is needed.

For mathematical tractability, only linear error models are considered. The converter's errors for all p code states are then represented in matrix form as

$$\mathbf{m} = \mathbf{A} \times \boldsymbol{\epsilon}, \qquad (1)$$

where $\mathbf{A}$ is the error model of dimension p x m, $\boldsymbol{\epsilon}$ is the vector of model component errors (m x 1), and m is the number of components or model coefficients.

Several techniques have been explored for generating the model $\mathbf{A}$. In some cases, where sufficient design information is available, the model is a circuit component sensitivity matrix computed using network analysis techniques. In the more general case where detailed design information is lacking or is too complex, the model can be developed from a combination of implicit (a priori) models, and from empirical data. For example, it is well known that the individual bit errors are predominant in many converter types, and the errors are fully represented using the Rademacher subset of Walsh functions as a model basis [1]. Therefore, the Rademacher functions are prime candidates for k of the m column vectors of $\mathbf{A}$, for a k-bit converter.

This analysis is illustrated in figure 1. Here, typical measurement results are presented for a 12-bit DAC. The top plot is of measured linearity errors versus codeword in ascending order. The middle plot shows the linearity errors which can be accounted for by individual bit errors, and represents a global least squares fit of bit errors to linearity error data. The plot

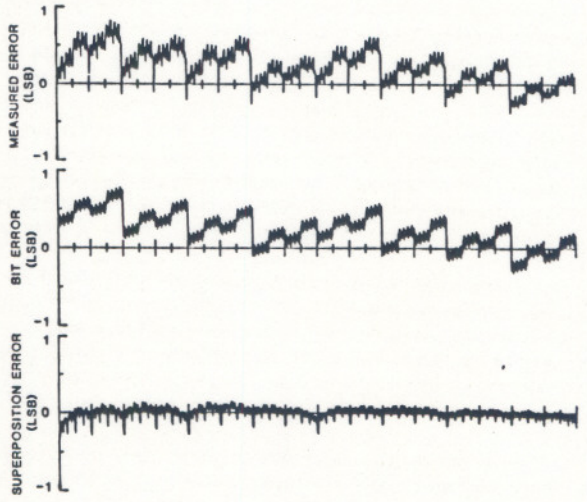


Fig. 1 Typical measurement results for a 12-bit DAC, showing measured linearity errors (top), errors attributable to the individual bits (middle), and superposition errors (bottom).



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was obtained by performing a Walsh transform of the measured errors, and then performing an inverse transform on only the Rademacher subset of Walsh functions, i.e., those functions which have the same sequency as the individual bits. The bottom plot gives the superposition errors which are, by definition, those errors which cannot be represented as simple sums of bit errors. This plot was obtained by subtracting the middle plot from the top plot. (Alternatively, it can be obtained by performing an inverse transform of all the non-Rademacher Walsh functions).

As seems evident from the bottom plot, superposition errors, which can arise from any number of different causes, are more difficult to model efficiently. However, lacking any additional a priori information, these errors can be modeled empirically through extensive (or all codes) tests of representative devices. From such measurement data, superposition models can be developed and expressed in terms of a complete but arbitrary basis, or alternatively, in terms of a natural basis, in which the error signature itself becomes a column vector of $\mathbf{A}$. For many converters, a truncated Walsh basis has been shown to be a suitable choice of the former type [2, 3]. The ultimate choice depends on the unit-to-unit repeatability of the superposition error signatures, the degree of noise present, and considerations of efficiency versus robustness. In the EXPERIMENTAL RESULTS section below, examples are given using models derived from circuit analysis as well as both empirical data approaches.

After the model has been developed, it is refined to eliminate possible dependencies among its components, i.e., the columns of $\mathbf{A}$. Independence among the components is assured by applying a QR Decomposition method [4] to $\mathbf{A}$.

## Test Point Selection

Having developed an efficient model (one requiring relatively few coefficients to completely express the expected behavior), the next step is to select an optimal set of test points which can be used to estimate the model's coefficients, $\epsilon$. Assuming a linear model, only m linearly independent test points are required to estimate the m model coefficients. The key is to find, out of the entire set of p code states, m test points which are both linearly independent and robust, to minimize the errors due to noise. Matrix decomposition techniques, specifically the QR Decomposition (QRD) algorithm, are well suited for this task.

Test points are selected by performing a QRD on the transpose of the model matrix $\mathbf{A}$. With this approach, $\mathbf{A}^T$ is reduced to the product of two matrices, one orthogonal ( $\mathbf{Q}$ ) and one right triangular ( $\mathbf{R}$ ). The decomposition process selects and orders the columns of $\mathbf{Q}$ following a modified Gram-Schmidt orthogonalization, first choosing the column of largest norm, orthogonalizing all remaining columns to it, next choosing the column of largest norm of these remaining, and so on, until the norms of all remaining columns are less than a preset bound. The code states corresponding to those columns of significant norm are the selected test points. The ordering, therefore, selects the test points which are maximally independent and thus robust.

Measurements are made at the test points selected by this process. To further minimize errors due to measurement noise, or to provide checks for model errors, additional points beyond the minimum required by the rank of the model are usually added.

## Coefficient Estimation

The coefficients of (1), i.e., the component errors $\epsilon$, are found by reapplying the QRD algorithm. In this case, the decomposition is performed on a truncated, reordered matrix, $\mathbf{A}'$, whose rows correspond to the chosen test codes. Equation (1) then becomes

$$\mu' = \mathbf{A}' \times \epsilon, \qquad (2)$$

where $\mu'$ is the vector of errors measured at selected test codes, and $\epsilon$ is the vector of independent component errors as before. A least squares estimate for vector $\epsilon$ is easily obtained by using one more QRD.

Finally, having determined $\epsilon$, the performance of the converter can be estimated at all test codes simply by solving for $\mu$ in (1).

After an adequate model and test sequence have been developed for a particular converter type, the same limited test sequence can be used for all subsequent converters of the same type, dramatically reducing testing time on the production line, or in incoming inspection.

# 3. Experimental Results

## Sensitivity Matrix Model

As an example of an explicit, sensitivity-based model, the 10-bit R-2R ladder network of figure 2 has been studied. Note that, in addition to the ideal ladder components, various residual error resistances have been added, such as nonzero ground and virtual ground bus resistance, and finite switch resistance. (Since the resistance in one switch position can be lumped with the 2R branch resistance, the resistance of only one position need be modeled explicitly). To generate sensitivity matrices for such networks, a general switched resistance network simulation program was written, based on nodal analysis techniques. The program accepts any arbitrary network of m resistors and k binary switches, and can permute the switches through all $2^k$ possible switch position combinations. Using the adjoint network method [5], the sensitivity of the transfer characteristic (i.e., output current divided by input voltage) to each component is calculated,

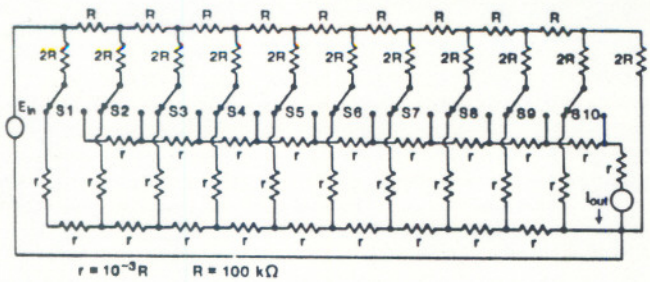


Fig. 2 Model for 10-bit R-2R ladder network DAC, with error resistances included (designated by r). Nominal values are shown.

forming one row of the sensitivity matrix **A**. The matrix is completed by repeating this process for each combination of switch positions or code states.

Once the sensitivity matrix is generated, a QRD is performed to select an independent set of components, thereby reducing the column order to rank. For the example of figure 2, the QRD reduced the 50 resistors to 37 independent components. The second QRD, used for test point selection, reduced the row order to rank, thus selecting the 37 test codes needed to solve for the 37 independent components.

Testing strategies derived from this model were tried experimentally on two D/A converters, one custom built to permit selection and manipulation of the various ladder and error resistances, and a commercially available IC multiplying DAC which was expected to have the same network topology. The custom built DAC has 10-bit resolution, and 16 locations at which known error resistances can be inserted. The commerical DAC has 12-bit resolution and was chosen because it exhibits significant superposition errors.

Linearity error measurements were made on both converters using the NBS data converter test set [1]. Full sets of measurements were made at the 1024 codes corresponding to all combinations of the top 10 bits, in accordance with the 10-bit model. The data corresponding to the 37 selected test codes was then used to predict the response at all 1024 codes, by first solving (2) for the component values, and then solving (1) for $\mu$. Test results, comparing the measured and predicted errors, are given in figures 3 and 4 respectively, for the two converters.

In figure 3, the top plot presents the errors for all code states predicted from the data taken at the 37 selected test codes, and the bottom plot gives the errors in the prediction, i.e., the difference between the predicted errors and the measured errors for all codes. Despite the large superposition error content of the test converter, the errors were predicted quite accurately. The residual pattern in the bottom plot is due to a small offset voltage in an output amplifier used with the DAC. Since this effect was not included

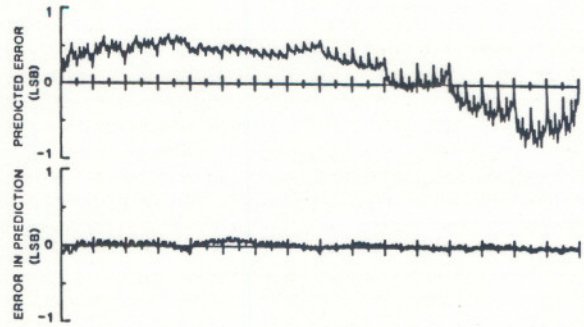


Fig. 3 Test results for custom built 10-bit DAC with selected errors, using explicit network model. Top plot gives predicted errors based on 37 measurements, and bottom plot gives errors in the prediction.

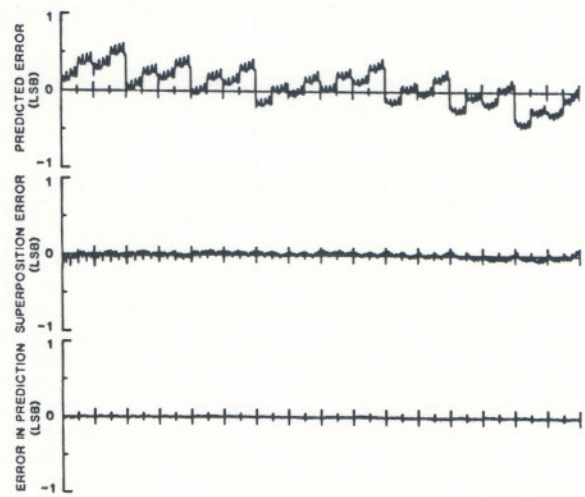


Fig. 4 Test results for commercial 12-bit DAC, using explicit network model, showing predicted errors based on 37 measurements (top), the calculated superposition errors of the converter (middle), and the errors in the prediction (bottom).

in the model, the results show up as small prediction errors. Therefore, the errors could be even further reduced by including the effects of offset voltage in the original model.

Figure 4 gives similar results for the commercial DAC. In this figure the top plot is the predicted error as before. To emphasize that the method is capable of predicting real superposition errors in commercial products, the middle plot gives the superposition error content of the converter as calculated from the full data set. The bottom plot gives the errors in the prediction, as before. The maximum error in the prediction is no greater than 5 % of the peak error.

## Truncated Walsh Model

The Walsh functions have been shown to constitute an efficient basis for many converter types, meaning that relatively few Walsh coefficients are needed to describe the errors of a given converter with reasonable accuracy. If it can further be shown that the same small subset of Walsh functions is complete for a whole class of converters, then they could form the basis for a useful model. This premise, of course, must be demonstrated empirically.

A truncated Walsh model was generated for the 12-bit converter discussed in the previous section. This model was developed by performing all codes tests on representative designs, and then performing full Walsh transforms on the data. The resulting Walsh coefficients were sorted by magnitude, and the Walsh functions having coefficients greater than a preselected bound were kept for the model. Since the Walsh functions are an orthogonal set, the selected model components need not be reduced to assure independence.

Test point selection, coefficient estimation, and calculation of the full error characterisitic were all performed as before, using the empirical truncated Walsh matrix for **A** . Having developed the model from a few representative devices, it was then applied to efficiently test other devices of the same general type. Typical test results are given in figure 5. For these results, 49 Walsh functions were selected for the model, requiring 49 test codes. As before, the two plots give the predicted errors (top) and the errors in the prediction (bottom). Despite the number of measurements involved, the errors have not been predicted as accurately as in the previous case where an actual network model was used. The poorer results indicate that a Walsh basis, at least in this case, is not particularly efficient. In addition, the accuracy is further reduced because the Walsh coefficients are not globally estimated as is customary, but instead are estimated on the basis of a single measurement per coefficient.

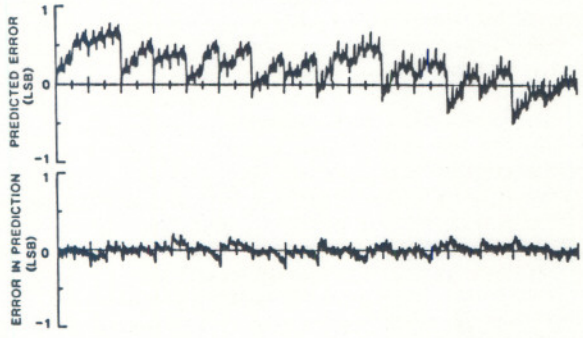


Fig. 5 Test results for commercial 12-bit DAC, using empirical 49 coefficient Walsh model. Top plot gives predicted errors based on 49 measurements, and bottom plot gives errors in the prediction.

## Natural Empirical Model

The superposition errors of the commercial 12-bit DAC (not including the output amplifier) arise almost entirely from residual resistance in the ground or virtual ground buses. It is reasonable to expect the pattern of these errors to be constant among units of the same design since they are determined by connection topology and line width. Their magnitude might vary from one production run to another, however, due to variations in thickness of metalization of the buses. In situations of this type, a testing strategy sensitive to such specific error patterns could be quite efficient. Taking another example, simple ladder network DACs of this type are quite susceptible to superposition error arising from offset voltage in the output amplifier which converts current to voltage. The resulting error signature has a fixed shape but an amplitude proportional to the actual offset voltage.

A strategy for the 12-bit DAC, including the output amplfier, has been developed and tested using this approach. It takes both of these effects, ground bus resistance and offset voltage,

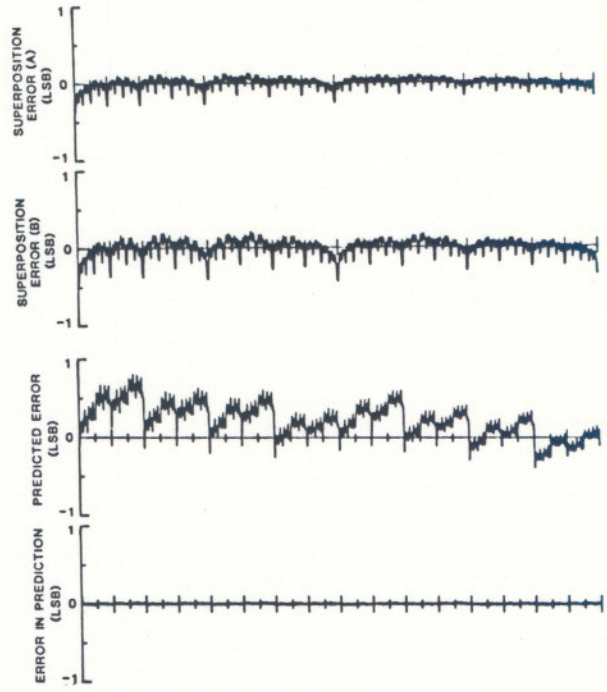


Fig. 6 Test results for commercial 12-bit DAC, using a 13 coefficient, empirical model based on 11 Rademacher functions and two sets of superposition errors. The top two plots show the superposition errors of the two other DACs from which the model was derived. The third plot gives the predicted errors for a third DAC, based on 13 measurements, and the bottom plot gives the errors in the prediction.

into account. The model was generated by using a combination of Rademacher Walsh functions to represent the bit errors, and the superposition errors were simply represented by two vectors of superposition errors calculated from the data of 1024-code tests of two representative devices. (Two devices were chosen exhibiting different amounts of superposition errors to provide enough information to separate the two error components). The 11 Rademacher functions and the two superposition error vectors then comprised the (13) columns of $A$. Test points were selected by QRD as before, and measurements were made at the selected test codes on a number of devices. Typical test results are given in figure 6. The top plots show the superposition errors of the two DACs from which the model was derived, the middle plot shows the predicted linearity errors for a third device, based on only 13 measurements, and the bottom plot gives the errors in the prediction, i.e., the difference between the predicted errors and the actual measurement data. With only 13 measurements, the errors have been predicted with a maximum uncertainty no greater than 2.5% of the peak error, despite the fact that the superposition errors in the unit tested differed from those upon which the model was based.

## 4. Conclusion

Based on the results in figures 3-6, it can be seen that careful modeling and test point selection techniques can result in accurate, efficient calibration strategies for D/A converters. In cases where it is feasible to develop a comprehensive model based on the component sensitivity matrix, this is probably the best approach since the model is then founded on engineering knowledge, and all major error conditions will in principle be embodied in the model. On the other hand, in cases where this is impossible, the empirical modeling approach using the error signatures themselves can still provide excellent results. In using the empirical approach, it should be borne in mind that, to be successful, the model must incorporate all significant error modes. Therefore, care must be taken to develop a truly representative model. Fortunately, as the results of figure 6 indicate, this is not necessarily difficult. In fact, in the authors' experience, it is quite common for superposition errors to have a characteristic shape which, although dependent on the peculiarities of the device's design and topological layout, varies only in magnitude from unit to unit.

In the examples included in this paper, the model components were estimated from the minimum number of test codes possible. In actual production testing, it would be good practice to include additional test points beyond the minimum. This would provide redundancy to reduce the random measurement errors, and would provide a means for detecting significant model errors which then show up as significant patterns in the residuals of the least squares parameter estimation.

While the present results have been limited to D/A converters, it seems quite reasonable to expect the same techniques to be applicable to A/D converters as well. In fact, the basic approach has much broader applications than just data converters. For example, the same techniques have been used to efficiently estimate the transfer functions of linear, time invariant networks such as amplifiers, attenuators and filters [6]. In this work, a sensitivity matrix model, together with the QRD test point selection techniques are again used; however, the test points are discrete test frequencies rather than switch codes.

## 5. Acknowledgements

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