Amorphous Nb-Si Barrier Junctions for Voltage Standard and Digital Applications

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Abstract—Amorphous Nb-Si has been previously demonstrated as a Josephson junction barrier material for Nb-based superconducting voltage standard circuits, including both dc programmable and ac Josephson voltage standards operating at frequencies up to 20 GHz. This material was chosen so that the junctions could be fabricated in vertical stacks, increasing the number of junctions in an array, which in turn increases the output voltage of the circuits. This barrier material may also be used to create higher-speed junctions, because the same factors that lead to improved stacks also lead to more reproducible junctions with thin, insulating barriers. Recently, a collaboration between the Physikalisch-Technische Bundesanstalt (PTB) and the National Institute of Standards and Technology (NIST) produced 1 V and 10 V programmable Josephson voltage standard chips operating at 75 GHz that use these junctions. In this paper, we demonstrate junctions with characteristic frequencies approaching 500 GHz and observed Josephson phase locking at frequencies of 400 GHz and 800 GHz. These junctions are promising for applications in high-speed superconducting digital electronics.

Index Terms—Josephson junctions, Josephson voltage standard, SNS junction.

I. INTRODUCTION

JOSEPHSON junctions using amorphous Nb_xSi_{1-x} barriers have been fabricated at NIST for voltage standard applications. These junctions were chosen because they have excellent run-to-run reproducibility, wafer-scale uniformity, and well controlled processing. A particularly important property they possess is the similar etching rates between Nb electrodes and the barrier, which allows for uniform multi-junction stack fabrication. The system also has a wide range of tunability of electrical parameters through control of both the barrier composition and thickness. With a sufficiently low Nb concentration such that the barrier is on the insulating side of the metal-insulator transition, junctions with values for the critical current density $J_c \sim 0.1 \, \mathrm{mA}/\mu\mathrm{m}^2$ and small hysteresis have been achieved; these junctions can have characteristic voltages $V_c = I_c R_n = (h/2e)f_c$ near 1 mV (where I_c is the critical current, R_n is the normal-state resistance, f_c is the characteristic frequency of the junction, and the ratio of Planck's constant to twice the electron charge is approximately 2.07 $\mu\mathrm{V}/\mathrm{GHz}$) [1]. This paper discusses the possibility of implementing this barrier and the corresponding Nb-based junction technology for high-speed superconducting digital electronics applications.

Superconductive digital electronics promises substantial improvements over conventional semiconductor electronics, including fast operating times with picosecond switching times, very low power consumption, and transmission lines of low loss and low dispersion for high-speed signals. Junctions for superconductive digital electronics have used predominantly oxide-barrier junctions [2]. These junctions are of high quality and may be fabricated uniformly on a wafer scale.

$Nb/AlO_x/Nb$ junctions are presently the preferred technology for superconducting integrated circuits [3], [4], but they are inherently hysteretic and require shunting resistors to bring them to the critically damped regime. These shunting resistors increase the complexity of the fabrication process and circuit layout, they reduce the circuit density, and introduce parasitic inductances. It has been observed that as the number of Josephson junctions in a circuit increases, the speed decreases significantly. This drop is not explained by the design of the circuits, but can be caused, in part, by random variations of the junction parameters, in particular I_c [4]. Ref. [5] indicates that variations in I_c of their junctions are likely caused by random variations in J_c and not by variations in junction sizes. This problem, most probably, will be more significant in junctions with higher J_c in which the oxide barriers are thinner [6]. These problems will likely hamper the implementation of shunted AlO_x-barrier junctions for high-speed circuit applications with densities approaching that of Si-based processor chips.

Self-shunted $Nb/AlO_x/Nb$ junctions of deep-submicron dimensions and oxide barriers of 1–2 monolayers thick have been developed and demonstrated with large critical-current densities, $J_c \sim 2 \, \mathrm{mA}/\mu\mathrm{m}^2$ [7]. These junctions can have reduced hysteresis, because their very thin barriers simultaneously increase both J_c and the subgap-leakage current. Such nonhysteretic junctions with high V_c are advantageous, because the fabrication is simpler and the parasitic inductances are eliminated. However, the ability to reproducibly yield high-quality, uniform junctions has not yet been achieved. It is also important to point out that these junctions need to be sub-micrometer sized due to their high J_c, another factor that complicates their implementation in circuits and affects uniformity. Frequency dividers using these junctions have been made that operated up to 520 GHz [8], but high I_c and high bias currents were a limitation.

Another method for obtaining intrinsically shunted junctions involves the use of high-temperature superconductors (HTS). Because they have large superconducting gap energies and thus potentially higher speed performance, HTS have been proposed and extensively investigated as candidates for high-speed mixer and digital superconducting electronics [9], [10]. However, even

for the lowest-speed junctions that operated far below the Nb gap frequencies, uniform and reproducible HTS junctions are difficult to fabricate. This has prevented their use in applications that require large numbers of junctions, such as those required for high-speed digital circuits.

Another technique to achieve nonhysteretic, high-V_c Josephson junctions is to use a barrier near the metal-insulator transition. The high V_c and relatively lower J_cs allow junctions that do not require submicrometer dimensions for practical critical currents less than 1 mA. However, previous efforts investigating junctions with non-silicide-based barrier materials suffered from complicated processing and poor reproducibility [11]–[13].

Unlike oxide barriers for which the thickness is only a few atomic layers, junctions with a-Si (amorphous silicon) and $a - \mathrm{Nb_xSi_{1-x}}$ barriers use significantly thicker barriers, thus offering the potential for better reproducibility of the junction electrical properties. Smith *et al.* [14] demonstrated stable fabrication of Nb-based Josephson junctions with a-Si-barriers. NIST has been fabricating uniform and reproducible $\mathrm{Nb/Nb_xSi_{1-x}/Nb}$ for use in vertically stacked junction arrays and has demonstrated SI'S junctions, where I' indicates a barrier in the regime between metal and insulator [1], [15]. In this paper, we describe results of our research focused on improving the quality of $\mathrm{Nb/a\text{-}Nb_xSi_{1-x}/Nb}$ Josephson junctions for voltage standards as well as research on junctions with lower Nb concentration and high values of V_c for operation at 75 GHz and higher speeds that are applicable to high-speed superconductive electronics.

II. FABRICATION

An automated, multi-target sputtering system was used to deposit Nb/Nb-Si/Nb trilayers similar to the process described in [16], [17]. The barriers were cosputtered by simultaneously using both Nb and Si targets, while the base and counter electrodes were deposited using only the Nb target. Three-inch diameter Si wafers with 150 nm of thermal $\mathrm{SiO_2}$ were used as substrates. By changing the sputter power of the Nb gun during the barrier deposition, the composition can be arbitrarily changed from pure Nb to pure Si. A superconducting transition temperature was found for films with x >∼ 15%, which limits the range of interest for this work to 0 < x < 15% [16]. During deposition, the substrate was backside-cooled by flowing $\mathrm{N_2}$ gas through the substrate platen. The substrate platen was rotated during deposition to improve uniformity across the wafer. The thicknesses of base and top Nb electrodes are 400 and 200 nm, respectively. As the base electrode thickness increases, the roughness due to columnar growth also increases. At a thickness of 400 nm, the estimated roughness is ∼5 nm, which is of the same order as the typical silicide barrier thicknesses [18]. In order to partially planarize the base electrode, an rf Argon plasma was used to slightly etch the surface before barrier deposition. We expect that the protruding columnar grains focus the local electric field, yielding a higher etch rate for the protrusions. An rf power of 100 W at 13.56 MHz was applied with a resulting dc bias in the range of 300 V. The Nb etch rate was measured at 2 nm/min for large structures, and an etch time of 6 min was used so that the total etch was several times larger than
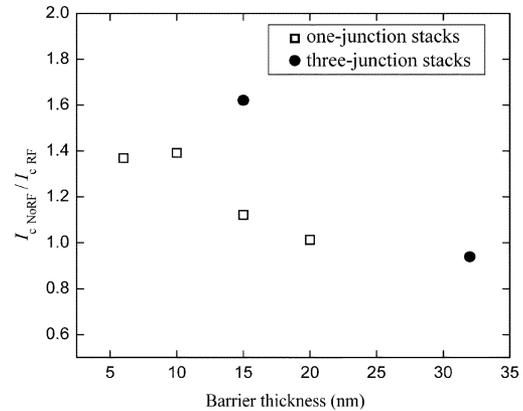

Fig. 1. Ratio of critical currents for untreated and RF-treated base and middle electrodes for 400 single-stack junction and triple-junction stacks arrays. The RF treatment for reducing the roughness of the electrodes has the greatest effect for thin barriers and three-junction stacks.

the expected surface roughness. This treatment gave a smoother surface on which to grow the barrier (as observed from TEM images) and thus gives more uniform junctions, especially when stacks are fabricated [19], [20].

III. PROPERTIES OF Nb-Si JOSEPHSON JUNCTIONS

The biggest challenge in producing high-speed junctions using an a-NbSi barrier is fabricating uniform, reproducible films for multilayer devices. The thin barriers demanded by this junction regime are particularly sensitive to roughness of the base electrode. Because this roughness will be translated throughout any multi-layer structure, it is important to grow the barrier on as smooth a surface as possible.

To address the roughness, we apply a RF plasma treatment to the base and middle electrodes of the stacks. Current-voltage curves (IVCs) of junctions with no rf plasma etching of the base electrode show a higher I_c as well as larger hysteresis compared to the plasma-etched junction. This result is due most likely to the fact that a rough surface with protrusions has regions of reduced barrier thickness, which dominate the critical current; smoother interfaces give a lower critical current for the same barrier thickness. It is expected that for thicker barriers (greater than the surface roughness) this effect will be reduced. On the other hand, it is expected also that in the case of stacks, irregularities will accumulate as the stack is grown taller, resulting in an enhanced difference between I_c for treated and untreated stacks.

Fig. 1 shows the ratio of critical currents for series-connected arrays with and without RF treatment. For single-junction-stack arrays with thin barriers (6 and 10 nm) the ratio is similar, around 1.4, but for thicker 20 nm barriers the effect is minimal. For stacked junctions the effect is more pronounced but also diminishes as the thickness increases. The RF treatment has a clear effect on the properties of junctions, especially in the case of thin barriers and taller stacks, which enable better junction uniformity. This treatment has now been incorporated in the NIST standard procedure of fabrication for Nb-Si barrier junctions for voltage standard applications. This may allow us to obtain taller stacks with margins suitable for voltage standard applications.
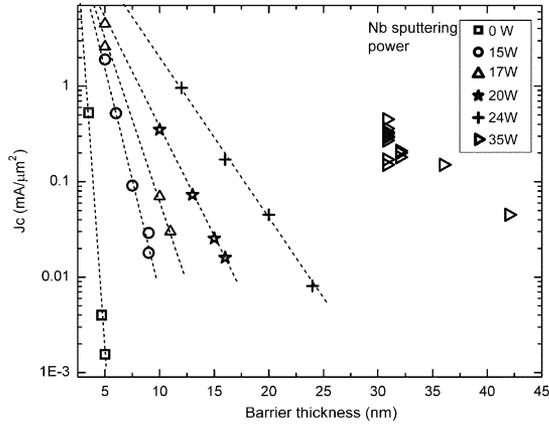
Fig. 2. Dependence of J_c on barrier thickness and composition for $Nb/Nb_xSi_{1-x}/Nb$ Josephson junctions. The composition is determined by the Nb sputtering power. The Si sputtering power is fixed at 200 W for all junctions. For a fixed composition, J_c depends exponentially on the barrier thickness. Dotted lines are an aid to the eye.

One big advantage of Nb-Si junctions is their ability to be tuned appropriately for a variety of different applications. For NIST Josephson voltage standards, the junctions have a characteristic frequency close to their typical 20 GHz operation frequency, which implies that $V_c \sim 40\,\mu V$. On the other hand, if we want to use these Nb-Si junctions at a higher frequency, such as 75 GHz, this requires $V_c \sim 150\,\mu V$. Because the critical current depends exponentially on the barrier thickness, while the normal resistance of the junction is linearly dependent, simply decreasing the barrier thickness will not yield useful devices—the current density will be too large for high-speed junctions. Instead, we want to increase the resistance of a junction by making the barrier more resistive. This is done by reducing the fraction of Nb in the barrier material. Simultaneously, the barrier thickness must be reduced, because a more resistive barrier will give a lower value for the critical current. By changing the composition and the thickness of the barrier, we can obtain the desired values of R_n and I_c so that the junctions can be tuned to the different frequencies and current densities required for each application.

Fig. 2 shows the dependence of J_c on thickness and composition. The plot shows the wide range of values for J_c which can be obtained by changing composition and thickness of the barrier. For a fixed value of J_c, usually determined by the desired junction size and a chosen design value of I_c, we can obtain different values of R_n (and thus V_c).

Recent results from these Nb-Si barrier junctions include 1 V and 10 V Josephson voltage standard chips operating at 75 GHz produced in a collaboration between PTB and NIST [21]. Because these voltage standard circuits have demonstrated operating margins and contain tens of thousands of junctions, their successful operation demonstrates the reproducibility and uniformity of these junctions.

IV. JUNCTION RESPONSE TO 400 GHz RADIATION

In an effort to demonstrate even higher frequency Nb-Si junctions with reasonable values of I_c, the insulating part of phase space in Fig. 2 was investigated in which the barrier has a low content of niobium; thus, it needs to be thin. Junctions were made with lateral dimensions of $2.5\,\mu m \times 2.5\,\mu m$ and embedded in double-dipole antennae in order to couple radiation from a laser to investigate their behavior under 400 GHz radiation. It is important to emphasize the fact that these junctions were fabricated with conventional lithography because sub-micrometer sized junctions are not necessary to maintain a value of I_c at a practical level (near 1 mA).

The electrical properties of the junction studied are as follows: 4.6 nm barrier thickness; barrier deposition sputtering gun powers of 8 W for Nb and 200 W for Si; $I_c = 0.764\,mA$; $J_c = 12.2\,kA/cm^2$; $R_n = 0.91\,\Omega$; $I_c R_n = 695\,\mu V$. The 1 cm $\times$ 1 cm chip containing the junctions was placed in a cryostat with a Mylar window, which allowed the radiation to enter. A silicon lens was attached to the back of the chip in order to focus the radiation onto the device under test.

The terahertz radiation was supplied by a CO_2-pumped formic acid (HCOOH) FIR laser [22], which radiated at 403 GHz. The output power of the FIR laser was measured to be 0.7 mW with a calorimeter at the output aperture. We were unable to continuously monitor the absolute power while measuring the Shapiro steps. Instead, we deflected the beam as often as necessary to a pyroelectric detector of small area (1 mm dia.) by use of a flip mirror to periodically monitor relative changes in power. At regular intervals between our Shapiro step measurements, the formic acid pressure was adjusted to maintain a signal level on the pyroelectric detector that was close to the value obtained when the 0.7 mW absolute power was measured. At 38 cm along the optical path from the FIR laser aperture, a 50.8 mm effective-focal-length parabolic mirror was placed to focus the beam onto the Josephson device assembly inside the dewar. The Josephson device assembly was located 8 mm behind the theoretical Gaussian beam waist, which was as close as possible before the dewar enclosure bumped into the focusing optics. Despite this complication, this configuration was chosen because it provided better coupling than one with a parabolic lens of longer (154 mm) focal length.

A set of polarizers before the cryostat allowed us to vary the power incident on the junction. Fig. 3 shows a pair of IV curves, with and without radiation coupled to the junction. The frequency, f, of the radiation was 403.7 GHz. Phase locking of the junction is clearly observed at f and 2f, giving rise to constant-voltage steps at 0.83 mV (n = 1) and 1.67 mV (n = 2), respectively. There is also a very small step at 2.5 mV, which is beyond the superconductor gap, as can be seen from the curve; this corresponds to locking at 1210 GHz. The vertical dotted lines show the theoretical values for n = 1, 2, 3 order constant-voltage steps. There is also a very small step at a value of V corresponding to n = 5/2, i.e., V = 2.087 mV, which appears to be due to subharmonic locking of the junction. Such subharmonic locking is possible in junctions with values of the McCumber parameter $\beta_C > 1$, that is, for junctions with relatively high capacitances. The McCumber parameter is given by $\beta_C = 2eI_c R_n^2 C/\hbar$, where C is the capacitance of the junction. The presence of hysteresis in the dc IVC indicates a value of β_C greater than unity for this junction. This is due to the reduced Nb content in the barrier. However, Fig. 3 shows that the IVC for the frequency-locked case is not hysteretic. Bias-induced heating is
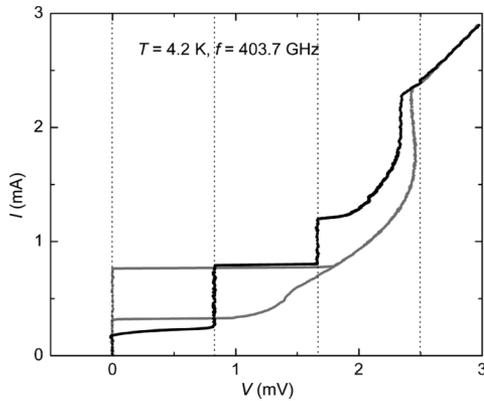
Fig. 3. IV curves of a $2.5 \times 2.5~\mu$m junction with (black trace) and without (grey trace) 403.7 GHz radiation applied. Vertical dotted lines mark the locations of $nf(h/2e)$ for $n = 0, 1, 2, 3$. At exactly half way between the second and third steps there is a small step that can be attributed to subharmonic locking of the junction ($n = 5/2$).
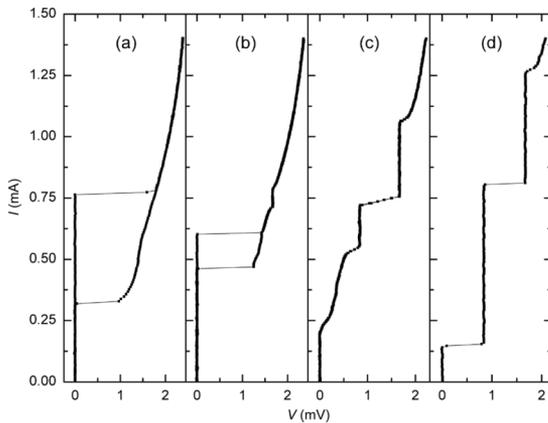

Fig. 4. A set of IVCs for different power transmitted into the cryostat. Curve (a) corresponds to zero power; consecutive curves correspond to increased power up to the maximum current range for the $n = 1$ Shapiro step (at 0.8 mV) as shown for curve (d).

evident from the backward bending of the IVC near the gap and from its reduced value. We can also see a small mismatch in the value of the gap voltages, being slightly lower for the irradiated case. This is likely caused by heating of the junction by the incident FIR radiation. One possible reason for this was the poor thermal contact between the sample and the cold plate of the cryostat to allow for coupling of the radiation.

By crossing the polarizers, the power dependence was investigated by observing the amplitude of the constant-voltage steps as the power coupled to the junction was varied. Fig. 4 shows that the amplitude of the steps increases with increasing applied power. The final curve (d) shows that the current range of the first and second steps increase with increasing power, while that of the zero step decreases, as expected. A detailed analysis of steps sizes and power dependence has not yet been performed.

V. CONCLUSION

Recent fabrication developments have improved the quality of a-NbSi-barrier Josephson junctions for NIST voltage standard circuits. By modifying growth parameters of the barrier, we

obtained a large range of junction electrical properties; in particular, we obtained high-speed junctions suitable for 75 GHz voltage standard systems. We also fabricated Josephson junctions with characteristic frequencies of a few hundred gigahertz that successfully locked to 400 GHz radiation. Even though the presence of Shapiro steps under 400 GHz radiation is not a proof that digital circuits made with such junctions can be clocked at this frequency, the large current range of these steps and the fact that they are close to the characteristic frequency of the junction suggest that a-NbSi-barrier junctions should be considered for high-speed digital circuits.

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