A Low-Noise Latching Comparator Probe for Waveform Sampling Applications

David I. Bergman, *Member, IEEE*, and Bryan C. Waltrip, *Member, IEEE*

***Abstract*—A new latching comparator probe is described. The probe is being developed as part of an effort to augment voltage measurement capability in the 10 Hz to 1 MHz frequency range. The probe offers an input voltage range of $\pm$10 V, input impedance of 1 MΩ and root mean square noise referred to the input as low as 55 μV. The probe's 3-dB bandwidth is approximately 20 MHz. Total harmonic distortion is as low as $-$93 dB at 50 kHz. Gain flatness is within $\pm$10 μV/V from 100 Hz to 100 kHz. Improved step settling performance is achieved using a technique that minimizes circuit thermal errors. The probe's input range can be extended with a frequency-compensated 1-MΩ input impedance attenuator allowing measurement of pulses in the microsecond regime up to 100 V. The attenuator can be compensated further with a digital filtering algorithm to achieve gain accuracy better than 100 μV/V.**

***Index Terms*—Comparator, frequency compensation, signal sampling, successive approximation, voltage measurement.**

I. INTRODUCTION

A low-noise latching comparator probe is being developed at the National Institute of Standards and Technology (NIST) to augment existing measurement capability for repetitive signals ranging in frequency from 10 Hz to 1 MHz. The probe is designed to work in conjunction with a wideband sampling voltmeter mainframe also developed at NIST. The voltmeter was designed to make wideband root mean square (rms) voltage measurements with accuracy comparable to that of instruments employing thermal converter technology, but requiring less measurement time and minimal operator intervention [1]. As a sampling and digitizing instrument, the voltmeter is also capable of measuring waveform parameters other than rms such as harmonic distortion, phase, and step settling response. Developed along with the voltmeter mainframe was a front-end sampling probe built around an NIST-designed application specific integrated circuit (ASIC) latching comparator [2]. Although the ASIC probe's performance is impressive for measurements in the RF range, its intrinsic rms noise ($\sim$ 400 μV), input impedance (50 Ω), and input voltage range ($\pm$2 V) are not well suited to lower frequency measurement applications such as distorted power, impedance, or pulses of microsecond or greater duration. The new probe will complement the ASIC probe and extend the sampling voltmeter's capability to include lower frequency, higher accuracy measurement applications. The new probe trades high bandwidth for much lower noise while offering very high input impedance, a wider input voltage range, comparable gain flatness over the 10 Hz to 100 kHz frequency range and better static linearity. These performance characteristics are needed to support an NIST Special Test measurement service for pulse settling [3] and other NIST measurement areas including power, ac rms voltage, and impedance.

Design goals of the probe included an input voltage range of $-$ 10 to + 10 V, rms noise less than or equal to 40 μV, input impedance greater than or equal to 1 MΩ, gain flatness less than or equal to 10 μV/V from 10 Hz to 100 kHz, step settling time of 200 ns to achieve a settling error of 10 μV/V and static linearity error of less than 20 μV/V of full scale over an input voltage range of $-$ 10 to + 10 V. An additional design goal was that the probe be able to accommodate a high input impedance (1 MΩ) voltage attenuator for measuring signals up to 100 V. Since a comparator capable of delivering this performance was not available, an effort was undertaken to develop one.

This paper describes the development effort and presents a few selected test results. Probe performance so far meets nearly all target goals and full compliance is expected from followup versions of the probe in the near future.

II. PROBE DESCRIPTION

As shown in Fig. 1, the latching comparator probe forms the comparator portion of a successive approximation type analog-to-digital converter (ADC) operating in equivalent time and at the same time performs the sampling function. A single conversion is obtained through a series of successive approximations, each occurring on a different period of the waveform being digitized. As each conversion is completed, the timebase delay is increased by one sample period allowing the next point on the waveform to be sampled. As implemented, the sampling mainframe's digitizing resolution is 16 bits.

The probe is comprised of a latching comparator and companion circuitry to interface the comparator to the sampling mainframe. Fig. 2 shows the measurement setup. The digital-to-analog converter (DAC) reference, strobe logic, and comparator decision output signals are sent and received differentially through individually shielded twisted pair cables that together comprise the probe umbilical harness. The probe is housed in a hand-sized metal enclosure. The probe input connector is type N. The umbilical connector is a standard 25-pin D connector.

Fig. 3 shows a simplified schematic of the latching comparator part of the probe. A latching comparator has two modes of operation—tracking and latching. In the tracking mode, the comparator tracks the input difference while the latch is disabled. In latching

Manuscript received June 15, 2002; revised January 13, 2003.

The authors are with the Electricity Division, Electronics and Electrical Engineering Laboratory, Technology Administration, National Institute of Standards and Technology, U.S. Department of Commerce, Gaithersburg, MD 20899 USA.

Digital Object Identifier 10.1109/TIM.2003.815982

U.S. Government work not protected by U.S. copyright.

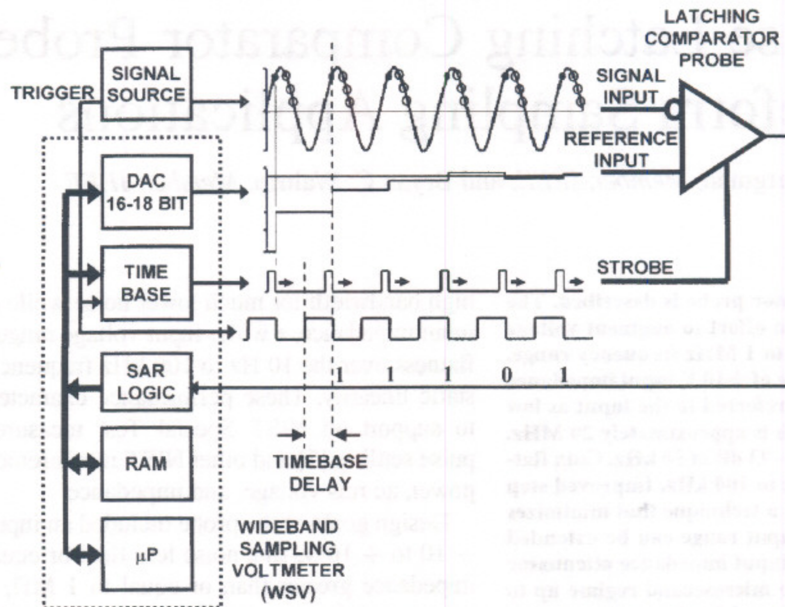

Fig. 1. Equivalent time successive approximation using a latching comparator.

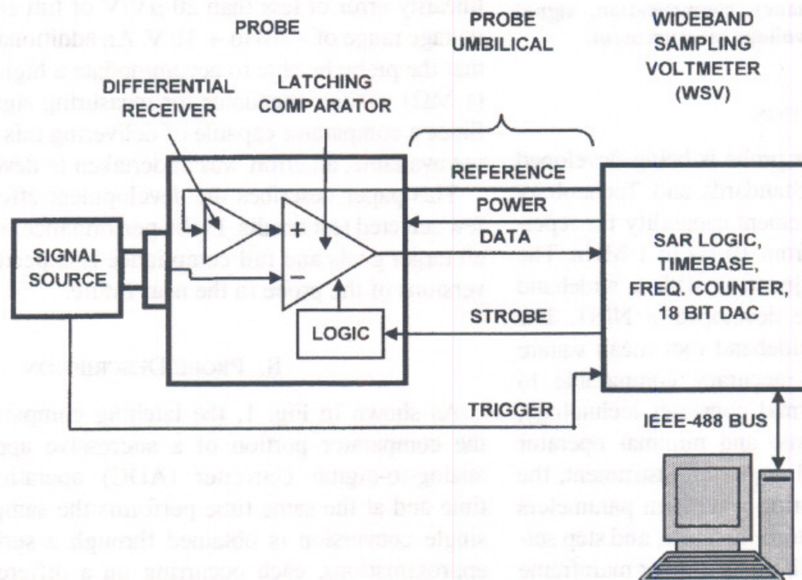

Fig. 2. Measurement setup of the probe, signal source, sampling voltmeter mainframe, and computer for data collection and control.

mode, the input amplifier (and subsequent tracking stages if present) is disabled and the latch enabled causing the output of the input amplifier at the latching instant to be regeneratively amplified by positive feedback producing logic levels at the output [4]. Sampling occurs within the comparator's latch rather than prior to preamplification. Comparators of this type have found widespread application in high speed, fully parallel ADCs [5], [6]. The latching comparator's simplicity, ease of construction, high performance, and flexibility to accommodate a refinement designed to minimize signal induced thermal errors made it the architecture of choice for this application.

III. Design Considerations

Several considerations guided the design approach. Because many factors can affect settling time including capacitor dielectric absorption, slew rate, saturation recovery, and thermal transients, to name a few, settling time usually is not specified in terms of settling error less than 100 μV/V of full scale [7]. For the latching comparator described in this paper, the dominant source of settling error and corresponding gain flatness error below 100 μV/V is thermal error arising from unequal self heating of the transistors comprising the differential pairs, particularly in the input stage. To meet the gain flatness and settling time requirements, minimizing signal induced thermal errors is a necessity. Therefore, a decision was made to use an approach similar to the enabling technique described in [2]. While a variety of commercial voltage comparator devices is available, a latching comparator that could accommodate a signal range of $\pm$ 10 V could not be found and there did not appear to be a straightforward way to address thermal errors present in an off-the-shelf device. If a custom design approach was to

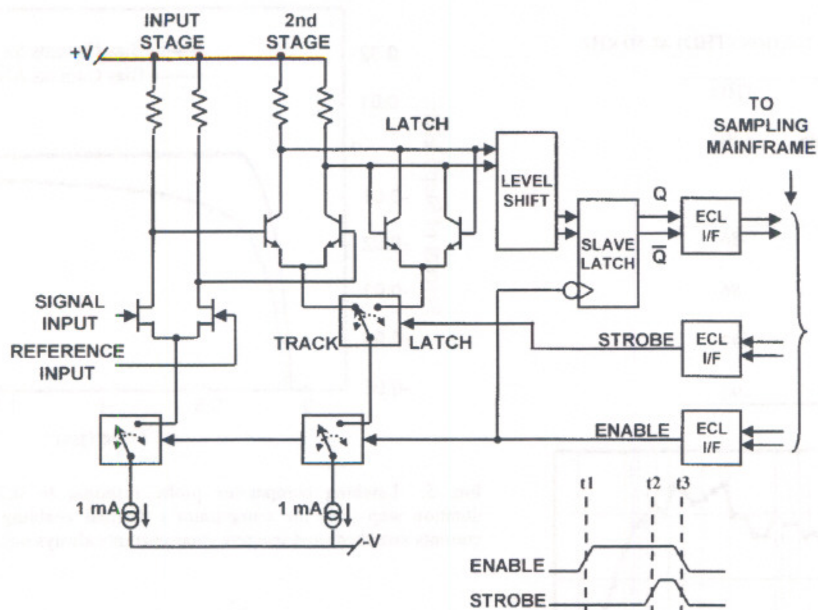

Fig. 3. Simplified schematic drawing of the latching comparator circuitry.

be taken, then compatibility with the voltmeter mainframe required that the probe have some form of differencing or comparison input to be able to compare the input signal with the mainframe's digital-to-analog converter (DAC) reference. Here, the high input impedance and low-noise requirements ruled out a resistive divider or bridge approach, and, for similar reasons, an operational amplifier based architecture was ruled out as well. The chosen approach would require the use of devices capable of sustaining signal levels between − 10 and + 10 V and even greater power supply voltages. From these considerations, a design approach was chosen similar to that taken with the ASIC comparator but using carefully selected discrete devices on a carefully laid out printed circuit board.

IV. Test Results

Selected test results are presented. Descriptions of the various test methods and sine fitting algorithm used may be found in [8] and [9].

A. Noise

Probe noise was determined by applying to the probe input a low-frequency (100 Hz) sine wave having a small, peak amplitude (~ 10 mV). To minimize the effects that noise and distortion components from the source would have on the test result, the signal was significantly attenuated before being applied to the probe. The frequency of 100 Hz was chosen so that signal distortion caused by the probe itself would be negligible. A 1000 point data record was collected at a sample rate of 20 μs per sample. The record was then fitted to a sine wave using a four-parameter least squares sine fit method. Probe noise was determined from the variance of the residuals of the sine fit. The contribution to the computed value from quantization noise was removed by subtracting $Q^2/12$ from the computed variance where Q is the code bin size. The assumption that quantization noise power is approximated by $Q^2/12$ is justified on the grounds that the signal traverses enough code bins to produce a nearly uniform distribution. Table I lists the noise standard deviation values for four full scale range settings of the probe. The probe's full scale range is set by the attenuation factor in the probe's differential receiver amplifier applied to the mainframe DAC reference signal. Signal-to-noise ratio or related parameters such as effective bits are omitted from this discussion because only the performance of the probe itself is being reported and not the overall performance of the sampling comparator system of which the probe is a part.

TABLE I
Measured RMS Noise

Full Scale Range (V)	Random and Quantization Noise (μV)	Random Noise Only (μV)
±10	137	105
±5	86	74
±2	60	58
±1	55	54

B. Total Harmonic Distortion (THD)

The probe's total harmonic distortion was measured with a 50 kHz sinusoidal signal. To minimize the effect that distortion components from the source would have on the test result, the source was filtered to ensure that the amplitudes of all harmonics of the signal frequency were at least 120 dB below the signal amplitude. Table II lists the results over four different full scale ranges. The test frequency of 50 kHz was chosen for a practical reason; it was the lowest cutoff frequency offered among the available collection of low distortion filters.

TABLE II
MEASURED TOTAL HARMONIC DISTORTION (THD) AT 50 kHz

FS Range (V)	Peak Amplitude (V)	THD (dB)
±10	4	-86
±5	4	-86
±2	1.5	-93
±1	0.7	-90

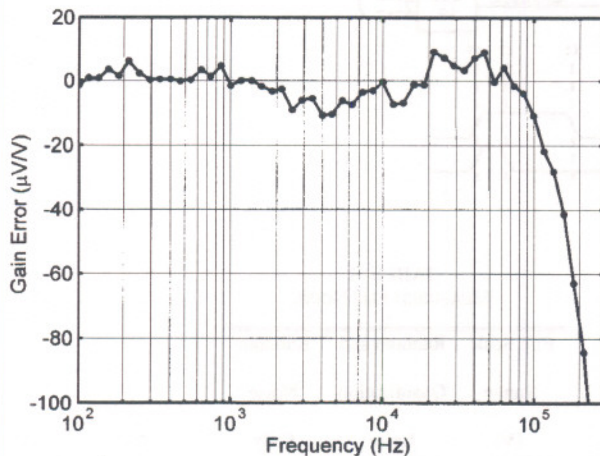

Fig. 4. Gain error of the probe relative to the value at 1 kHz. The peak signal amplitude was 4.5 V.

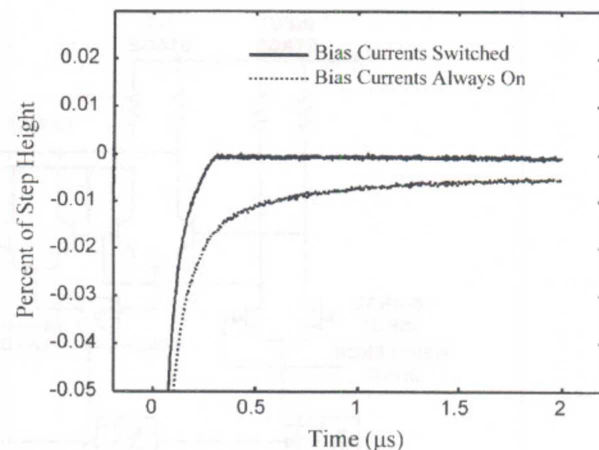

Fig. 5. Latching comparator probe response to 0.5-V, 15-ps transition duration step with the comparator's thermal enabling feature active (bias currents switched) and inactive (bias currents always on).

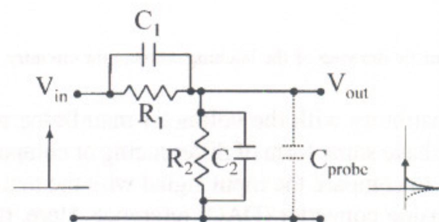

Fig. 6. Commonly used frequency compensated attenuator.

C. Gain Flatness Versus Frequency

The 3-dB bandwidth of the probe is approximately 20 MHz. This result can be obtained either by a swept sine measurement or from the probe's transition duration in response to a step input. One of the principal applications of the probe is to measure ac rms accurately. To characterize the probe for this purpose, its frequency response was measured between 100 Hz and 100 kHz using a swept sine test method against a commercial ac/dc thermal transfer standard with direct traceability to NIST thermal voltage converter (TVC) standards. The measurement was made by connecting a sinusoidal source to the inputs of both the probe and the transfer standard using a coaxial tee connection. To minimize timing jitter, the signal itself was used to trigger the sampling mainframe through a tap at the measurement plane with a second tee. The peak signal amplitude was 4.5 V measured on the probe's ± 10-V scale. Fig. 4 plots the result of this measurement. Because it is not relevant to the computation of rms, the phase response of the probe has not yet been characterized. However, phase response is a parameter of interest and will be the subject of a future investigation.

D. Settling Time

The step settling response of the probe was measured with a reference step generator designed to output a nearly ideal step-like waveform. Fig. 5 shows the response of the probe to a 0.5 V step whose 10% to 90% transition duration is approximately 15 ps. In the figure, the 50% point of the step's rising transition occurs at time 0 μs. The curve labeled "bias currents switched" shows the step settling response with the probe configured so that the tracking stages' bias currents are held off until 300 ns prior to strobing using an enabling technique described in [2]. The curve labeled "Bias currents always on" shows the step settling response with the probe configured so that the tracking stages' bias currents are held constant as would be the case in a typical amplifier or comparator circuit. The improvement in settling response due to enabling is evident. Further study examining the effects of different enabling times is ongoing. Enabling can also improve gain flatness in the frequency domain. Determining the probe's frequency response from step response data allows the probe to be calibrated independent of thermal converters and is the subject of ongoing work at NIST [10], [11].

E. High Voltage Pulse Response

The probe may be used to measure signals with amplitudes up to several hundred volts at frequencies from dc to 20 MHz if a suitable voltage attenuator is present at the signal input. To minimize loading of the source and power dissipation in the attenuator and associated thermal errors, the attenuator should use relatively high resistance values. However, unless compensated, a high output resistance from the attenuator will form a low-pass filter with the input capacitance of the latching comparator reducing the probe's bandwidth. To maintain bandwidth, a conventional frequency compensation scheme may be used as shown in Fig. 6. When $R_1C_1 = R_2(C_2 \| C_{probe})$, the input to

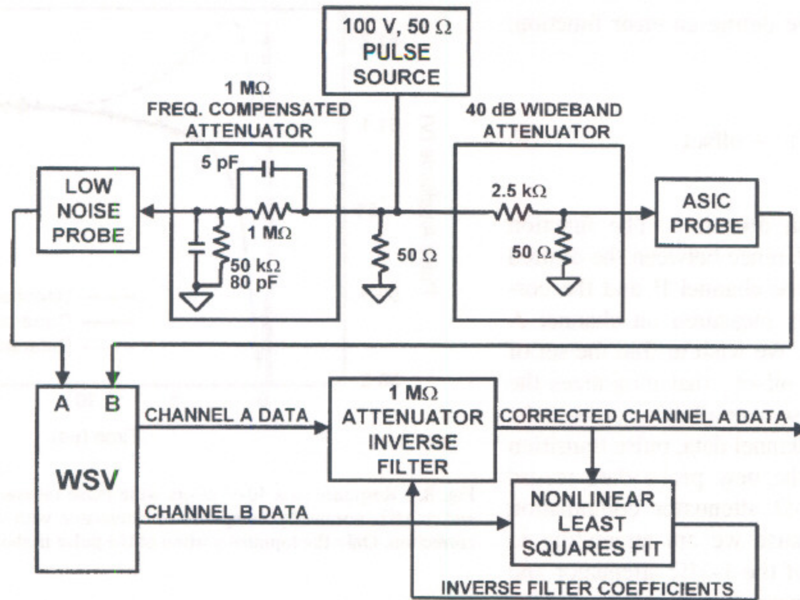

Fig. 7. Measurement setup for determining optimal filter coefficients to numerically correct for mismatch in the high side and low side impedances of the 1 MΩ attenuator.

output transfer function of the network is purely real. In practice, it is difficult to match the attenuator impedances (including the probe input capacitance) to better than about 1%. For applications requiring uncertainties better than 1%, the attenuator's frequency response may be compensated further using a digital filter on the sampled data. The digital filter compensates for mismatch between the high side and low side impedances of the attenuator by providing a transfer function that is the inverse of the attenuator's transfer function.

The digital filter is derived as follows. The transfer function of the frequency compensated attenuator may be written as

$$H(s) = \frac{a_0 s + a_1}{b_0 s + b_1} \quad (1)$$

where $a_0 = R_1R_2C_1$, $a_1 = R_2$, $b_0 = R_1R_2(C_1 + C_2)$ and $b_1 = R_1 + R_2$.

The inverse Fourier transform of this expression gives the impulse response $h(t)$ of the filter

$$h(t) = \frac{a_0}{b_0}\delta(t) + \left(\frac{a_1}{b_0} - \frac{a_0}{b_0}\frac{b_1}{b_0}\right) e^{-b_1/b_0 t} u(t) \quad (2)$$

where $\delta(t)$ is the unit impulse function and $u(t)$ is the unit step function. Since (1) is the transfer function of the attenuator RC network, then, by inspection, the inverse filter is seen to be of precisely identical form but with the a and b coefficients exchanged. Performing this exchange in the time domain produces an expression for the impulse response of the inverse filter. The discrete-time inverse filter's impulse response may be written as

$$h^i(kT) = \frac{b_0}{a_0}\delta(kT) + T\left(\frac{b_1}{a_0} - \frac{b_0}{a_0}\frac{a_1}{a_0}\right) e^{-a_1/a_0 kT} u(kT) \quad (3)$$

where kT are discrete sample times occurring at integer multiples of the sample period T.

This expression can be simplified as

$$h^i(kT) = w_1\delta(kT) + w_2T(w_0 - w_1)e^{-w_2kT}u(kT) \quad (4)$$

where $w_0 = (R_1 + R_2)/R_2$, $w_1 = (C_1 + C_2)/C_1$ and $w_2 = 1/(R_1C_1)$ are the three governing parameters of the attenuator response. Numerical compensation of the attenuator is achieved by computing $h^i(kT)$ for a given sample rate and record size and then convolving probe data with this impulse response. Alternatively, the inverse filter can be implemented with an equivalent two-step process. The exponential component of (4) acts upon the data in a manner that can be represented by a first-order infinite impulse response (IIR) filter

$$y'_k = w_2T(w_0 - w_1)x_k + e^{-w_2T}y_{k-1} \quad (5a)$$

and the impulsive component of (4) is accounted for by adding to the intermediate result, y'_k, of (5a) the input data, x_k, appropriately weighted

$$y_k = y'_k + w_1x_k. \quad (5b)$$

Fig. 7 illustrates one method for obtaining the filter's coefficients. A 100-V pulse generator drives the 1-MΩ attenuator to be corrected connected to the probe on mainframe channel A. The generator also connects to a reference sampler consisting of a wideband ASIC probe and a wideband 50-Ω attenuator on channel B. The data collected through the low-noise probe channel are filtered by the attenuator inverse filter using initial estimates for the filter coefficients. A nonlinear least squares fitting algorithm fits the filtered data to the reference channel data iteratively until an appropriate stopping criterion is reached.

The procedure goes as follows. We define an error function, $\mathrm{err}(w_0, w_1, w_2, \mathrm{offset})$ as

$$\mathrm{err} = \mathrm{chB} - \mathrm{chA}^*\mathrm{h}^{\mathrm{i}} + \mathrm{offset} \tag{6}$$

where '*' denotes the convolution operation. The function $\mathrm{err}(w_0, w_1, w_2, \mathrm{offset})$ is the difference between the desired output as measured by the reference channel B and the corrected (inverse filtered) probe data measured on channel A with allowance made for an offset. We wish to find the set of parameters $\mathbf{x} = [w_0 \quad w_1 \quad w_2 \quad \mathrm{offset}]$ that minimizes the error function in a least squares sense over all data points in the record. Note that in the reference channel data, pulse transition times are much smaller than in the new probe data record because the ASIC probe and 50-Ω attenuator combination has much higher bandwidth. Because we are attempting to correct only the transfer function of the 1-MΩ attenuator and not the difference in bandwidth between the new probe and the ASIC probe, for pulse measurements, we exclude points in the vicinity of the transitions from the fit. Note also that because the transition frequency of the attenuator is much less than the bandwidth of the probe, the inverse filter is fitted entirely to the response of the attenuator and not to the response of the probe which is almost completely flat in the vicinity of the transition frequency. Since the function err is nonlinear in the parameters, we use Newton's method to search iteratively for the minimum error. Because the set of equations is overdetermined, the iterative Newton procedure has the form

$$\mathbf{x}_{i+1} = \mathbf{x}_i - \left(\mathbf{J}_i^T \mathbf{J}_i\right)^{-1} \mathbf{J}_i^T \mathbf{err}_i \tag{7}$$

where err is a vector of errors computed for every point included in the fitting process. $\mathbf{J}$ is a sensitivity matrix relating each parameter to the error and has the form

$$\mathbf{J} = \begin{bmatrix} | & | & | & | \\ \frac{\partial \mathbf{err}}{\partial w_0} & \frac{\partial \mathbf{err}}{\partial w_1} & \frac{\partial \mathbf{err}}{\partial w_2} & \frac{\partial \mathbf{err}}{\partial \mathrm{offset}} \\ | & | & | & | \end{bmatrix} \tag{8}$$

where each column contains the partial derivative of the error function with respect to a different parameter at each data point. The partial derivatives are determined numerically. For example, to determine the sensitivity of the error function to the w_0 parameter, we compute (9), at the bottom of the page, with a suitably small Δw_0. As already noted, once determined, the filter coefficients may be used to resample the filter impulse response for data collected at any sample rate.

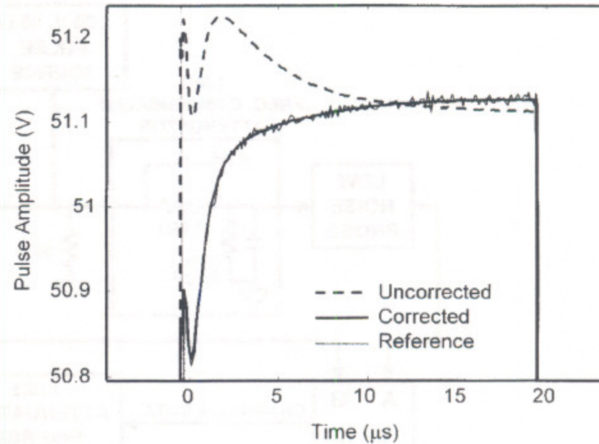

Fig. 8. Response to a 50-V 20-μs wide pulse measured with the new probe and 1 MΩ, nominally compensated attenuator with and without numerical correction. Only the topmost portion of the pulse is shown.

Fig. 8 demonstrates the ability of digital filtering to compensate for nonoptimal trimming of the attenuator's fixed components. The topmost portion of a 50-V 20-μs wide pulse measured with the probe and attenuator nominally compensated is shown. Also shown in the figure is the pulse after digital correction overlaid upon the pulse measured with the wideband ASIC probe as a reference. Agreement between the corrected waveform and the reference waveform is better than 100 μV/V. The new probe's lower noise is also clearly evident.

V. Conclusion

A latching comparator probe is being developed to support an NIST Special Test Measurement Service for repetitive pulse waveforms and to respond to external customers' needs for accurately measuring ac rms and pulse waveform parameters. The probe works in conjunction with an NIST developed wideband sampling voltmeter mainframe and is part of an ongoing effort to improve voltage measurement capability in the 10 Hz to 1 MHz frequency range. Several of the probe's performance parameters were discussed including intrinsic noise, total harmonic distortion, gain flatness versus frequency, and step settling time. Use of the probe with a high-input impedance, frequency compensated attenuator for measuring signals up to 100 V was also discussed. A digital filter algorithm for further compensating the attenuator to 100 μV/V gain accuracy was described.

Acknowledgment

The authors would like to thank M. Souders and O. Laug for their valuable advice, suggestions, and insight. The authors

$$\frac{\partial \mathbf{err}}{\partial w_0} = \frac{\mathbf{err}(w_0 + \Delta w_0, w_1, w_2, \mathrm{offset}) - \mathbf{err}(w_0, w_1, w_2, \mathrm{offset})}{\Delta w_0} \tag{9}$$

would also like to thank R. Palm for his contribution to the fabrication and assembly of the probe and supporting hardware.

REFERENCES

[1] T. M. Souders, B. C. Waltrip, and O. B. Laug, "A wideband sampling voltmeter," *IEEE Trans. Instrum. Meas.*, vol. 46, pp. 947–953, Aug. 1997.

[2] O. B. Laug, T. M. Souders, and D. R. Flach, "A custom integrated circuit comparator for high-performance sampling applications," *IEEE Trans. Instrum. Meas.*, vol. 41, pp. 850–855, Dec. 1992.

[3] *Calibration Services Users Guide*, NIST Special Publication SP250, 1998, pp. 189–193.

[4] R. Ockey and M. Syrzycki, "Optimization of a latched comparator for high-speed analog-to-Digital converters," in *IEEE Proc. Canadian Conf. Elect. Comput. Eng.*, 1999, pp. 403–408.

[5] P. J. Lim and B. A. Wooley, "An 8-bit 200-MHz BiCMOS comparator," *IEEE JSSC*, vol. 25, pp. 192–199, Feb. 1990.

[6] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997, pp. 328–330.

[7] H. K. Schoenwetter, "A sensitive analog comparator," *IEEE Trans. Instrum. Meas.*, vol. IM-31, pp. 266–269, Dec. 1982.

[8] *Standard for digitizing waveform recorders*, IEEE Std. 1057-1994, 1994.

[9] *Standard for terminology and test methods for analog-to-digital converters*, IEEE Std. 1241-2000, 2000.

[10] T. M. Souders and D. R. Flach, "Accurate frequency response determinations from discrete step response data," *IEEE Trans. Instrum. Meas*, vol. IM-36, pp. 433–439, June 1987.

[11] J. P. Deyst and T. M. Souders, "Bounds on frequency response estimates derived from uncertain step response data," *IEEE Trans. Instrum. Meas.*, vol. 45, pp. 378–383, Apr. 1996.

David I. Bergman (M'99) received the B.S.E.E. degree from the University of Maryland, College Park, and the M.S. degree in electrical engineering from the Johns Hopkins University, Baltimore, MD, in 1988 and 1994, respectively.

From 1988 to 1999, he was with the National Aeronautics and Space Administration designing mixed-signal electronic instrumentation for space-borne scientific instruments. Since 1999, he has been with the Electricity Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD, where he is currently working to develop precision sampling instrumentation and improved methods for testing complex electronic devices.

Bryan C. Waltrip (M'87) received the B.S. degree in electrical engineering and computer science from the University of Colorado, Boulder, and the M.S. degree in electrical engineering from the Johns Hopkins University, Baltimore, MD, in 1987 and 1998, respectively.

Since 1984, he has been an Electronics Engineer with the Electricity Division, National Institute of Standards and Technology, Gaithersburg, MD, where he is currently working on precision waveform synthesis and measurement standards in the dc to 1-GHz frequency range.