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Silicon nanowire NVM cell using high-k dielectric charge storage layer

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ABSTRACT

Si nanowire (SiNW) channel non-volatile memory (NVM) cells were fabricated by a "self-alignment" process. First, a layer of thermal SiO_2 was grown on a silicon wafer by dry oxidation, and the SiNWs were then grown by chemical vapor deposition in pre-defined locations. This was followed by depositing the gate dielectric, which almost surrounds the nanowire and consists of three stacked layers: SiO_2 blocking layer, HfO_2 charge-storing layer and a thin tunneling oxide layer. Source/drain and gate electrodes were formed by photolithography and lift-off, and the devices were electrically tested. As expected from this fabrication process and the enhanced electrostatic control of the "surrounding" gate, excellent cell characteristics were obtained.

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1. Introduction

There is a need for urgent progress in non-volatile memory (NVM) technology as is made abundantly clear in the latest (2007) IEEE International Electron Devices Meeting (IEDM) technical digest [1]. Among the many currently pursued approaches, a NVM cell architecture that shows great promise uses silicon nanowire channel and discrete trapped charge storage [2]. The cylindrical geometry of this cell allows excellent size scaling and fast program/erase (P/E) operation. Fig. 1a and b are two cross section schematics of such a cell, showing the nanowire channel, the tunnel oxide, the storage (trapping) layer, the blocking oxide and the gate electrode. The "natural" length λ for this geometry [2,3] has a logarithmic dependence on the gate equivalent oxide thickness to nanowire diameter ratio t_{EOT}/t_{Si}. This makes it possible to scale the channel length without the need to reduce the gate oxide thickness very much, thereby improving the retention time of the cell. A second consequence of the cylindrical geometry is the increased density of the (concentric) field lines on the nanowire surface, which lowers the cell program/erase voltage [2]. Finally, the cylindrical geometry leads to a reduction of the "effective" width of the tunneling barrier, resulting in fast cell operation [2]. In this paper a novel approach is described to fabricate silicon nanowire channel NVM cells, which leads to excellent cell characteristics. Section 2 presents the experimental details of the fabrication process; Section 3 presents and discusses the experimental measurements of the cell characteristics (write/erase and retention) and finally concluding remarks are made in Section 4.

2. Experimental/device fabrication

Compared to the nanowire obtained via lithography and etching, which are more controlled in terms of position, self-assembled nanowire has the following advantages: (i) thin channel (as small as 1 nm) which is impossible to achieve by lithography-defined etching, (ii) smooth surface, and (iii) self-assembling technique which will exponentially reduce the fabrication cost of nanoscale device. In this work, a "self-alignment" process was developed whereby silicon nanowires were grown via self-assembling from Au catalyst patterned on predefined locations by photolithography and lift off [4,5]. First, a 50 nm layer of SiO_2 was thermally grown on a heavily doped p-type silicon wafer by dry oxidation. A pattern of "open windows" (5 μm × 11 μm) was then defined by photolithography, a 1 nm thick Au film was deposited and the Au catalyst locations were defined on this oxide by the lift-off process. The wafers were then transferred into a low pressure chemical vapor deposition (LPCVD) furnace, where the SiNWs were grown on the Au catalyst with a SiH_4 stream at 440 °C for 2 h under a pressure of 500 mTorr by the vapor–liquid–solid (VLS) mechanism [6]. Following growth step, the SiNWs were oxidized at 700 °C for 30 min in O_2 with rapid thermal process (RTP) to form a 2 nm thick SiO_2 layer as the tunneling oxide. At this point a pattern of Al/Au Schottky contact source/drain electrodes were deposited and aligned with the Au catalyst pattern (hence "self-alignment" process): after opening suitable windows through the tunneling oxide by wet

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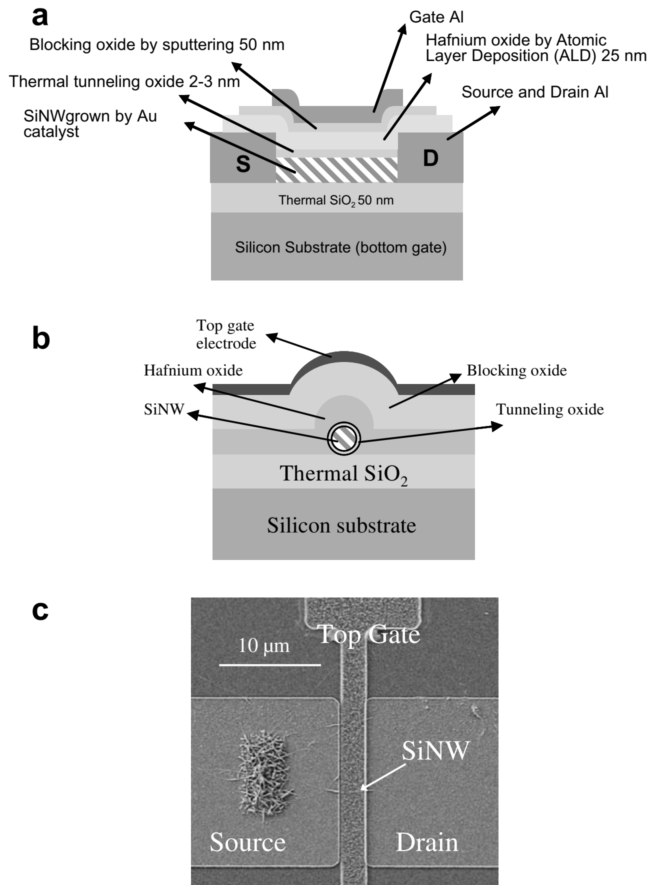

Fig. 1. Two cross-section views of the SiNW-based memory device are shown in (a) and (b). (c) SEM picture of a typical SiNW based memory cell with L_{gate} = 3 μm.

etching in 2% HF for 15 s, Al/Au (50/10 nm) source/drain electrodes were deposited by electron beam evaporation and lift-off. SiNWs grown by CVD show a certain degree of disorder. By optimizing the size and position of Au catalyst, device structure and nanowire length, about 85% of the pre-defined locations successfully form the SiNW memory device with one or more nanowires. A layer of 25 nm HfO_2 was then deposited by atomic layer deposition (ALD) with tetrakis hafnium (TEMAH) and H_2O steam at 250 °C, followed by deposition by sputtering of the blocking SiO_2 50 nm thick layer. The top gate electrode was finally formed by the same process as the source and drain. The finished devices were annealed in forming gas (5% H_2 in N_2) at 325 °C for 5 min by rapid thermal annealing (RTA). This final annealing step was found to significantly reduce the interface state density between the SiNWs and dielectric layers. The process flow is summarized in Fig. 2, and as seen in Fig. 1a and b the resulting "omega-shaped gate" and gate dielectric is surrounding the SiNW channel. Fig. 1c shows the scanning electron microscope (SEM) image for the top view of a typical SiNW based memory cell with 3 μm gate length.

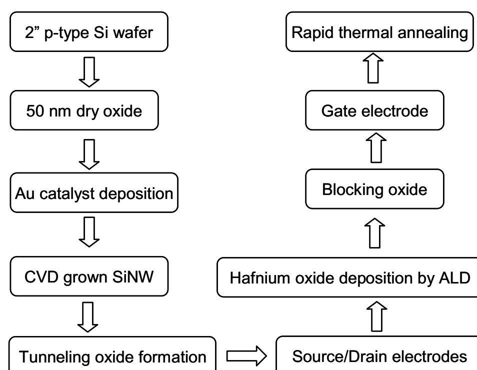

Fig. 2. Process flow for the SiNW based memory cells.

3. Results and discussion

The typical dimensions of the nanowires grown as described above were 20 nm diameter and 5–20 μm length. The memory cells had channel lengths in the 2–6 μm range and the experimental results shown here were taken from a 3 μm cell. The normal cell operation is with the substrate grounded and the top gate acting as the control gate; the characteristics can also be measured by grounding the front gate and using the substrate (bottom gate) as the control gate.

Fig. 3 shows the drain current versus drain/gate voltage characteristics for a range of drain, top gate (V_{TG}) and bottom gate (V_{BG}) voltages. The channel current under top gate control is much higher than under bottom gate control, since the top gate nearly surrounds the SiNW and thus exercises greater electrostatic channel control than the bottom gate. A large threshold voltage shift is obtained when V_{TG} or V_{BG} is swept from +10 V to −10 V. A memory window of 6 V and an ON/OFF current ratio of 10^7 is observed in the SiNW memory device with top gate control; both these values are smaller with bottom gate control, once again demonstrating the top gate stronger electrostatic control. At V_{TG}/V_{BG} = +10 V, the

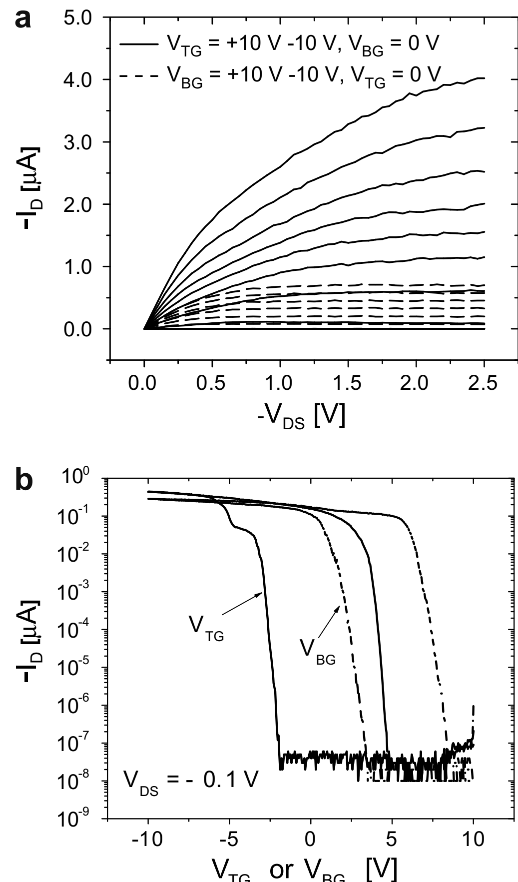

Fig. 3. Electrical characteristics of a typical SiNW memory cell under top gate (solid line) or bottom gate (dash line) control. (a) I_{DS} vs. V_{DS} at V_{TG}/V_{BG} = +10 V to −10 V in −1 V steps. (b) I_{DS} vs. V_{TG}/V_{BG} for V_{DS} = −0.1 V.

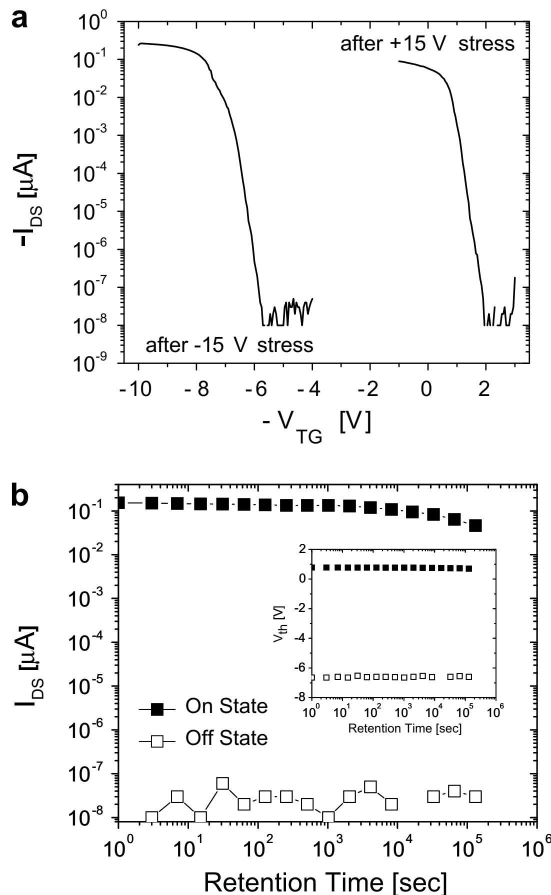

Fig. 4. (a) I_D–V_{TG} transfer curves of a typical cell at programmed and erased state (b) The monitored drain current vs. time at $V_{TG} = V_{BG} = 0$ V and $V_{DS} = -1$ V. The memory cell was initially programmed or erased at *V*g_write/*V*g_erase = +15 V/−15 V for 1 s. The extracted threshold voltage vs. retention is plotted in insert.

electrons in the channel tunnel through the thin tunneling oxide and are trapped in the HfO_2 charge storage layer where they induce a threshold voltage shift in the positive direction. Under negative gate bias $V_{TG}/V_{BG} = -10$ V, these electrons are de-trapped while holes are attracted and trapped in the HfO_2 layer shifting the threshold voltage in the negative direction. The status of the memory can be read by the presence or absence of current flowing between source and drain due to the two distinct threshold voltage values.

Retention time is a critical parameter for nonvolatile memory application, as the threshold voltage of programmed/erased memory may decrease/increase with time due to: (1) injection of carriers from silicon to the charge trapping layer and (2) loss of charge from trapping layer to silicon or gate electrode by tunneling. For modern nonvolatile memory, at least 10 years of retention time is required. Two I_D–V_{TG} transfer curves of a typical device at programmed and erased state are shown in Fig. 4a. The device was sequentially biased at $V_{TG} = +15$ V/−15 V with grounded bottom gate for 1 s and a memory window of 8 V was obtained. In each case the drain current at $V_{TG} = V_{BG} = 0$ V was monitored with time as shown in Fig. 4b, where it is shown that the ON current degraded by a factor of 10 in 10^5 s. The extracted threshold voltage vs. retention time is plotted as well. These rather poor retention characteristics are probably due to the grain boundaries of hafnium oxide which may introduce current leakage paths. For the erased device, the OFF current does not change significantly over the same time period (Fig. 4b). The reason for the excellent erase retention performance might be the favorable hafnium oxide/silicon valence band energy offset [7].

4. Conclusions

We have fabricated nonvolatile memory cells with CVD-grown silicon nanowire channel and hafnium oxide charge storage/trapping layer. The devices display p-type semiconductor transport characteristics. Because the gate and the HfO2 dielectric surround almost completely the nanowire ("omega gate") the cells exhibit excellent gate control, large memory window, and a higher ON/OFF current ratio. The retention capability of the programmed and erased cell is also discussed. We believe that this type of omega gate SiNW-based cell with high-*k* trapping layer is very promising for high density, low cost and high performance future nonvolatile memory technologies.

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