Negative-bias temperature instability induced electron trapping

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Despite four decades of research, the physics responsible for the negative-bias temperature instability (NBTI) in *p*-channel metal-oxide-silicon field-effect transistors is still unresolved. The current NBTI debate focuses on the dominance of either a hole trapping/detrapping mechanism or a hydrogen depassivation mechanism. In this study, we present NBTI-induced changes in the peak transconductance which indicate the presence of a third mechanism involving electron trapping/detrapping. The presence of this electron trapping/detrapping component adds further complexity to the very complicated NBTI phenomenon. © *2008 American Institute of Physics*.
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The negative-bias temperature instability (NBTI) is one of the most important reliability problems in advanced *p*-channel metal-oxide-silicon field-effect transistors (*p*MOSFETs).[1] It manifests as an increase in absolute threshold voltage (V_{th}) and degradations in drive current (I_D) and channel transconductance (G_M).[1] NBTI's exacerbation in highly scaled *p*MOSFETs with silicon oxynitride (SiON) gate dielectrics is one of the major reasons for its recent rise in importance.[2] Consequently, a considerable research effort has been devoted to determine the mechanism which governs this elusive phenomenon. However, 40 years of research[3] has still not led to a definitive understanding of NBTI.

Historically, the physics responsible for NBTI have been debated since the phenomenon was first reported.[3] Very early reports indicated that a portion of NBTI-induced degradation is recoverable.[4] This partially recoverable degradation is the key feature which distinguishes NBTI models. One faction of researchers believes that NBTI is dominated by the hydrogenic depassivation and repassivation of interface states (reaction-diffusion kinetics)[5] while another faction believes that NBTI is dominated by both the depassivation of interface states and a hole trapping/detrapping component. For many years, reaction-diffusion kinetics has been used to explain most NBTI observations. However, the recent development of fast measurement techniques has produced data which are more consistent with the hole trapping/detrapping mechanism.[6] An increasing number of recent fast NBTI measurements supports a hole trapping/detrapping mechanism.[7,8]

In this study, we extend our recent speculative reports[9,10] to include strong experimental evidence of yet another NBTI mechanism, namely, electron trapping and detrapping. This mechanism contributes to the transient behavior of NBTI, but with a more complex time dependence than hole trapping and detrapping. An increase in electron detrapping after harsher stressing conditions (where the interface state density is presumably higher) indicates that the trapped electrons are at energy levels which require an interface state mediated detrapping process.

Fully processed 2×0.06 μm^2 and 2×0.07 μm^2 (physical gate area) *p*MOSFETs with 1.6 nm SiON gate dielectrics were utilized in this study. Our measurements involve a fast-I_DV_G technique in which a voltage pulse is applied to the gate electrode while the drain current is monitored using a fast-amplifier circuit.[11,12] Both the gate pulse and drain current response are captured and stored on a digital oscilloscope such that the entire I_DV_G curve is captured at the rising and falling edges of each gate pulse. The gate pulse sequence utilized in this work is schematically illustrated in Fig. 1. The pulse train consists of a trapezoidal "stress" pulse and a triangular postrecovery "sense" pulse separated by a variable recovery time where the gate voltage is held at 0 V. This results in prestress (a), poststress (b), and postrecovery (c) fast-I_DV_G measurements. Peak-G_M values were extracted for each fast-I_DV_G measurement with the help of digital filtering. The details and performance of our fast-I_DV_G measurement methodology are described elsewhere.[10] For simplicity, the postrecovery G_M values were taken as the average of the falling and rising measurements of the sense pulse (c). The major contribution of this work stems from an examination of $\%G_M$ degradation values between the prestress and postrecovery measurements. A drain voltage of −50 mV is maintained at all times while the source and substrate remain grounded.

Figure 2 illustrates the $\%G_M$ degradation as a function of recovery time for devices subject to a NBTI stress of −2.5 V at 125 °C for 10 s. Each data point represents the average of 12 repeated measurements with a fresh device for each recovery time. It is important to note that the stress condition

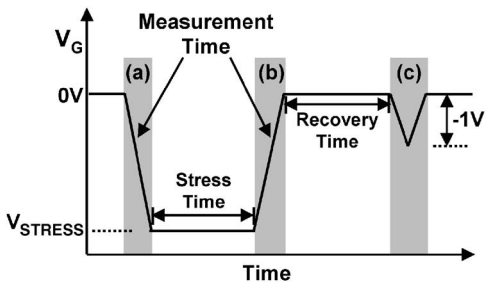

FIG. 1. Schematic of the gate voltage pulses during the NBTI stress and measurement sequences. The major contribution of this work stems from a comparison of the (a) prestress and (c) postrecovery extracted $\%G_M$ degradation values.

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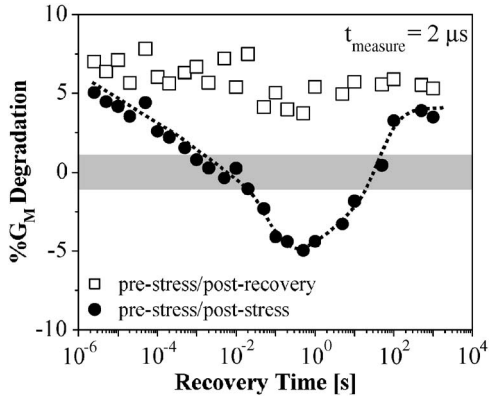

FIG. 2. Prestress/postrecovery $\%G_M$ degradation as a function of recovery time for 2×0.06 μm^2 *p*MOSFETs subject to a NBTI stress of −2.5 V at 125 °C for 10 s. The prestress/poststress $\%G_M$ degradation values are included for completeness. The box centered about 0% represents one standard deviation error bar. The lines are only a guide for the eyes.

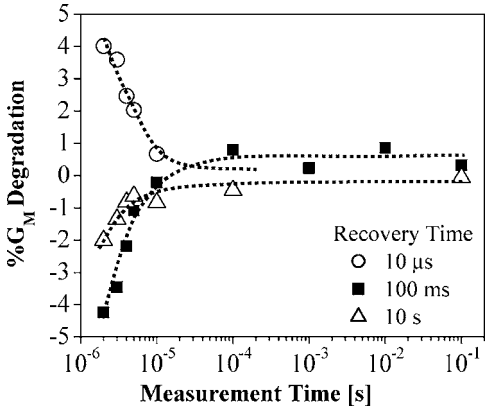

FIG. 3. Prestress/postrecovery $\%G_M$ degradation as a function of measurement (rise and fall) time for 2×0.07 μm^2 *p*MOSFETs subject to a NBTI stress of −2.5 V at 125 °C for 10 s. G_M degradation/improvement is only observable for measurement times <10 μs. The lines are only a guide for the eyes.

utilized in this study is rather common for NBTI studies of ultrathin gate dielectrics,[6] but represents electric fields which are traditionally categorized as high-field stressing. This high-field stress component is very likely present in most of the reported NBTI literature and will become unavoidable as device scaling continues. It is clear from Fig. 2 that $\%G_M$ is dependent on the recovery time. At very short recovery times (2 μs), $\%G_M$ exhibits degradation. As recovery time increases $\%G_M$ decreases and transitions to negative values. This corresponds to post-recovery peak-G_M values *better* than the prestress measurement. At longer recovery times, $\%G_M$ reaches a minimum (maximum improvement) and turns around toward the positive initial degradation values. The observed G_M improvement, albeit brief, is an unexpected result which forces the introduction of an electron trapping and detrapping component to NBTI. While our recent fast-I_DV_G reports detail V_{th} and G_M parametric variations as a function of both stress voltage[9] and stress time,[10] this recovery time study is the first to clearly demonstrate the presence of a NBTI-induced electron trapping/detrapping component.

The observed G_M degradation at short recovery times is consistent with the assumption that NBTI generates (1) traditional interface states which, in *p*MOS devices, are positively charged in inversion and (2) trapped holes in the bulk of the gate dielectric.[13] Both of these species contribute positive charge which increases the Coulombic scattering and degrades G_M. Both hole detrapping and interface state repassivation (as assumed in reaction-diffusion kinetics) can explain the reduction in $\%G_M$ degradation as the recovery time increases. However, neither mechanism is capable of improving G_M to values better than before stress. G_M improvement is only possible by realizing that there must be trapped electrons in the gate dielectric which can effectively counteract the positively charged interface states to reduce Coulombic scattering and improve G_M. Observation of G_M improvement due to electron trapping is rare, but not without precedent. For example, Charpenel *et al.*[14] observed G_M improvement after injecting electrons into the gate dielectric.

The complete $\%G_M$ behavior can be explained as follows. Stress traps both holes and electrons in the gate dielectric and generates positively charged (during measurement) interface states. At the conclusion of stress, the combination of trapped holes and interface states overwhelms the trapped electrons, and we observe a net increase in positive charge and Coulombic scattering, which is observed as G_M degradation. It is known that holes detrap faster than electrons.[15–17] Thus, as the recovery time increases and the hole concentration decreases, the net positive charge and Coulomb scattering also decrease.[18] This leads to a reduction in the G_M degradation. This process continues until the trapped holes are largely depleted, leaving only the trapped electrons in the bulk. The net positive charge is now at a minimum (and could even be negative). If the net positive charge is less than the amount before stress, G_M improvement will result, as the case in Fig. 2. At longer recovery times, the electrons eventually detrap, which diminishes the net negative charge in the dielectric and reduces the interface state compensation.[18] Only the positively charged interface states remain, and G_M returns to degradation.

Further evidence supporting our electron trapping hypothesis comes from the observation that G_M improvement is only observable using very fast measurement times. Figure 3 illustrates $\%G_M$ as a function of measurement time (rising or falling time of the gate pulse) for various recovery times. Depending on the recovery time, $\%G_M$ exhibits improvement or degradation. Clearly, this transient G_M behavior is only observable when the measurement time is less than 10 μs. This behavior is also consistent with electron trapping by realizing that the formation of an inversion layer of holes will neutralize any trapped electrons via tunneling. Since the gate dielectric is only 1.6 nm thick, the tunneling front rapidly reaches the trapped electrons.[16] Consequently, only fast measurements (faster than inversion layer formation and tunneling neutralization times) are capable of observing this electron trapping phenomenon. We recently reported this measurement time effect[10] and tentatively attributed the behavior to the presence of trapped electrons. An examination of our somewhat expanded G_M observations as a function of measurement time (Fig. 3) and our systematic examination of recovery time (Fig. 2) very strongly indicate the presence of an electron trapping/detrapping mechanism. This electron trapping/detrapping mechanism is hidden in typical NBTI V_{th} characterizations by the relatively large positive charge accumulation and depletion. The identification of the electron trapping/detrapping component was only possible due to our

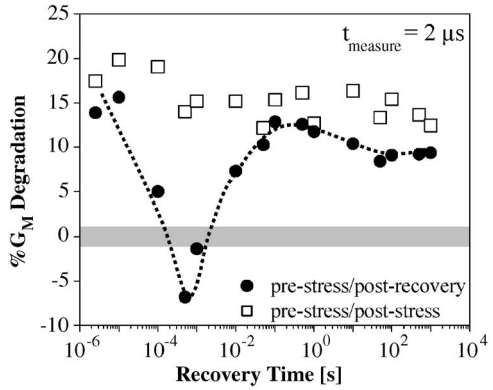

FIG. 4. Prestress/postrecovery $\%G_M$ degradation as a function of recovery time for $2\times0.07\ \mu m^2$ *p*MOSFETs subject to a NBTI stress of −2.7 V at 125 °C for 1000 s. The prestress/poststress $\%G_M$ degradation values are again included for completeness. The box centered about 0% represents one standard deviation error bar. The lines are only a guide for the eyes.

measurement technique, G_M extraction, and careful characterization of the recovery time period.

In an effort to further examine the electron trapping/detrapping phenomenon, the experiment was repeated using a harsher stress condition (−2.7 V at 125 °C for 1000 s). Figure 4 illustrates the $\%G_M$ degradation as a function of recovery time for this harsher stress condition. Since this harsher stress very likely introduces a permanent degradation, no averaging was used for these measurements. It is important to note that the G_M turnaround now occurs at a much shorter recovery time. This suggests that both holes and electrons detrap much faster. The perceived faster hole detrapping may be due to a much higher trapped hole concentration[19] or may simply be a consequence of faster electron detrapping which obscures the actual hole detrapping. It is even possible that the hole detrapping rate may not have changed. However, the faster electron detrapping is, without question, real. It is difficult to explain why a harsher stress would increase the electron detrapping rate if the electrons detrap to either the conduction or valence bands. (The harsher stress should have no effect.) This leads to the conclusion that the electron detrapping must be assisted by interface states and that the electrons must detrap to the substrate, not the gate electrode.[15] Within this framework, a harsher stress would presumably lead to a higher interface state density which allows for a faster electron detrapping rate.

In summary, a rare G_M improvement was observed for a brief duration after NBTI stress. Our results are consistent with an additional NBTI-induced electron trapping/detrapping component occurring in parallel with the well known hole trapping and interface state generation. Post-stress detrapping of both holes and electrons produces complex transistor parameter shifts. Qualitative analysis of the electron detrapping process suggests that the trapped electrons detrap to the substrate and require the help of interface states. The identification of this electron trapping/detrapping mechanism further refines the current understanding of NBTI.

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