High Temperature, High Power Module Design for Wide Bandgap Semiconductors: Packaging Architecture and Materials Considerations

Z. John Shen, Brian Grummel, Ryan McClure, Ali Gordon, and Allen Hefner*

College of Engineering and Computer Science, University of Central Florida
P.O. Box 162362, Orlando, FL 32816-2362, USA
Tel: 407-823-0379, Fax: 407-823-5835, E-mail: johnshen@mail.ucf.edu

*National Institute of Standards and Technology, Gaithersburg, Maryland, USA

Abstract

Wide bandgap power semiconductors such as SiC or GaN can safely operate at a junction temperature of 500°C. Such a high operating temperature range can substantially relax or completely eliminate the need for bulky and costly cooling components commonly used in silicon-based power electronic systems. However, a major limitation to fully realizing the potential of SiC and other wide band-gap semiconductor materials is the lack of qualified high-temperature packaging systems, particularly those with high-current and high-voltage capabilities required for power conversion applications. This paper proposes a new hybrid power module architecture that allows wide bandgap semiconductor power devices to operate at a junction temperature of 300°C. The concept is based on the use of double metal or DCB leadframes, direct leadframe-to-chip bonding, and high temperature encapsulation materials. The leadframes, serving as both the external leads and the internal interconnect to the semiconductor chips, need to provide excellent high temperature stability, adequate electrical and thermal conductivity, and a coefficient of thermal expansion (CTE) closely matching that of SiC or GaN. The SiC chips are sandwiched between and bonded to the top and bottom leadframes using a brazing or adhesion process. Extensive electrical, thermal, and mechanical modeling has been performed on this new concept. Several prototypes are fabricated and evaluated. Packaging architecture and materials considerations are discussed in detail.

Key words: *high temperature packaging, power module, wide bandgap semiconductors, power electronics.*

I. Introduction

Wide bandgap semiconductors such as silicon carbide (SiC) or gallium nitride (GaN) are widely considered as the power semiconductor of choice due to their wide energy band-gap, high breakdown field strength, high operating junction temperature, high carrier saturation drift velocity, and high thermal conductivity [1]-[4]. SiC or GaN devices offer great potential for use in high-temperature, high-power, high-frequency, and radiation-resistant military applications such as ultra-compact, ultra-light power conversion units in ground power sources, hybrid electric vehicles, and electric aircrafts and ships. SiC devices can also be used in a wide range of commercial applications including hybrid electric cars, power supplies, and electric utility power units.

The wide bandgap semiconductor power devices can safely operate at a junction temperature of up to 500°C to 600°C. Such a high operating temperature range can substantially relax or totally eliminate the need for bulky and costly thermal management components such as liquid cooling components, fans, and heat sinks that are commonly used in silicon-based power electronic systems, leading to a smaller, lighter, more efficient, and more reliable power converter design particularly suitable for military applications. The thermal management subsystems in many silicon-based power converters account for up to 30 percent to 40% of the total system cost. The cost benefit at the system level resulted from higher operating temperatures that can partially offset the high cost of today's SiC components, eventually leading to a lower total-system cost as SiC technology evolves. However, a major limitation to fully realizing the potential of SiC and other wide band-gap semiconductor materials is the lack of qualified high-temperature packaging systems, particularly those with high-current and high-voltage capabilities required for power conversion applications. The commercial SiC Schottky diodes currently available are only rated for an operating junction temperature up to 175° C due to the limitation of the conventional plastic packages used.

The primary issues to be considered in high-temperature electronic packaging are:

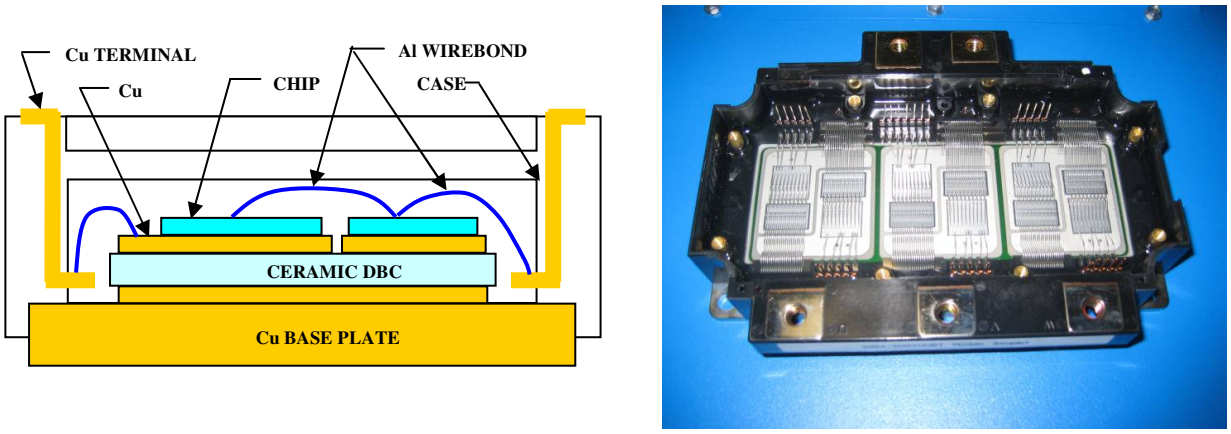


Fig. 1: Basic structure of hybrid power module using wirebond, DBC substrate and Cu base plate. A typical half-bridge Si-IGBT/SiC-Diode power module is also shown.

- Characterizing materials and their interactions at high temperatures
- Minimizing mechanical stresses caused by thermal expansion mismatches
- Providing a suitable path for heat dissipation
- Providing environmental protection
- Ease of system integration (from chip-level to board-level).

In addition, high current capability and low package interconnect impedance are critical factors in the design of hybrid power modules for power electronic systems. The overall objective of packaging is to distribute signal and power, dissipate heat, protect the devices enclosed inside, and ensure reliable operation of semiconductor devices. Considerable progress has been made in the field of high-temperature electronics and electronic packaging in the past two decades [8]-[10]. The high-reliability packaging schemes used today for military applications do offer considerable high temperature operation capability but fall short on power handling capability and other requirements.

A single metal package is usually made of gold-plated Kovar (an alloy of 53% iron, 29% nickel). The output leads are sealed into the Kovar package sidewalls or floor using glass-to-metal seals or ceramic feedthroughs. These metal packages are designed with welded metal lids. Gold (Au) wires are typically used to interconnect the semiconductor chip and the metal leads using a wirebonding technique. These metal packages have been evaluated to 400°C with satisfactory results [10]. However, these packages are limited to relatively low current applications due to the use of thin Au wires (typically 2-5 mils in diameter). Paralleling these packages for higher current capability may be feasible for low-frequency power converters, but does not provide a viable solution for high-density, high-performance power electronic systems due to the inevitable large parasitic impedance and physical dimensions associated.

Another widely used type of packaging that provides good high-temperature performance is the ceramic package. Ceramic packages are manufactured using a cofired tape process and have an advantage over metal packages because they can avoid the use of expensive fragile glass-to-metal seals [11]. The packages can be sealed either by soldering or welding. Temperature limitations for ceramic packages depend on the type of sealing method used. However, these ceramic packages are not suitable for high-current applications due to the high resistance of the refractory metal interconnects used inside the packages.

For conventional temperature high power electronic systems, multi-chip hybrid power modules are predominantly used. The hybrid modules distribute signal and power, dissipates heat, protects the devices enclosed, and serves as the basic power electronics building block (PEBB). The state-of-the-art power module technology, initially developed in mid-1980's, mainly relies on the use of aluminum wirebonds, direct-bond-copper (DBC) ceramic substrates, and copper base plates, as shown in Figure 1. The thin aluminum wirebonds suffer from high parasitic impedance, fatigue induced lift-off failures, and inability to remove heat. The DBC ceramic substrate (Al_2O_3 or more expensive AlN) provides electrical isolation but inadvertently increases the package thermal resistance. The thick Cu base plate serves as a heat spreader but considerably increases the weight, size, and thermal resistance of the power module. The easy oxidation of Cu, low melting temperatures of the Sn/Pb solder joints of chip-to-DBC and DBC-to-baseplate, and low glass transition temperature of the epoxy case all prevent the use of the

conventional power modules in high temperature applications.

Over the past few years, high-temperature power modules based on AlN ceramic substrates have been developed [13]-[15]. AlN ceramic has excellent high temperature stability, high thermal conductivity and a coefficient of thermal expansion (CTE) closely matching that of SiC materials. One of the proposed approaches was to use molded AlN package with nickel (Ni) conductor traces actively brazed to the AlN substrate [13]. Semiconductor chips are soldered directly to the Ni conductors and aluminum wirebonds connect the devices to interconnect circuitry on the AlN substrate. This approach is very similar to the conventional ceramic hybrid packaging technology. Another slightly different approach was to use a flat AlN substrate with patterned metal films, and a Kovar alloy case and Kovar feedthroughs brazed to the AlN substrate [15]. Yet another approach was to use direct die attaching and flip-chip techniques in addition to the use of AlN substrates [14]. This approach eliminates the need of wirebonds, which are known to be the weakest link at high temperatures. However, this approach does not offer high current handling capability due to the high resistance of the thick-film Au or Pt interconnection layer used.

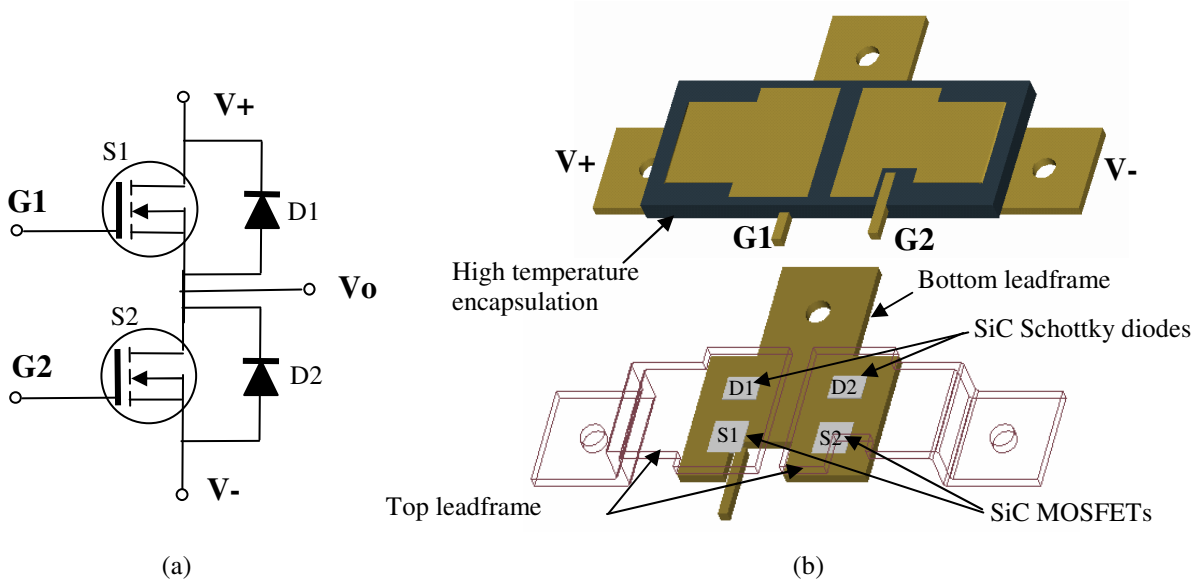
Those AlN-based high-temperature modules are essentially very costly duplicates of the existing conventional temperature hybrid module technology, which is, unfortunately, a 20-year old technology due for an overhaul itself. The biggest problem of a conventional power module is the complexity of its material system, which is comprised of multiple semiconductor chips, one or more ceramic substrates with patterned metal interconnect films, a metal baseplate, Al or Au wirebonds connecting the semiconductor chips to the substrate metal layer, soldering joints of semiconductor-to-substrate and substrate-to-baseplate, epoxy sidewall module case, external metal posts or feedthroughs, and silicon-gel potting material. Such a module construction method unnecessarily increases the module's weight, size, and junction-to-case thermal resistance. More critically, the complex material system creates many joints and interfaces between dissimilar materials, which tend to cause reliability concerns at high temperatures or under thermal cycling conditions. For example, it is well known that aluminum wirebonds tend to fail by creep deformation at high temperatures, and Sn/Pb solder joints suffer from voids or delamination under thermal cycling in the conventional power modules. While the reliability issue can be mitigated to a certain extent through the selection of new materials and processes (often with the penalty of a sharp increase in cost), as suggested by the aforementioned high temperature modules, it would be much more advantageous to have a simplified material system to begin with.

Furthermore, in the conventional hybrid power modules (and their high-temperature variants alike), heat is solely dissipated from the semiconductor chips downward to the ceramic substrate, metal baseplate, and eventually to the external thermal management components such as the heat sinks or liquid-cooling cold plates. Note that the top side of the power module does not contribute at all to removing heat from the semiconductor chips. While this may be tolerated in conventional temperature power converters equipped with sophisticated cooling subsystems, it is highly desirable to dissipate heat from both sides of the module in high temperature electronic systems, where we expect to employ very simple or no cooling design at all.

In short, the existing hybrid power module technology, limited by its material and construction complexity, does not provide a good platform for new high temperature module development. It is simply not enough just to substitute the materials in the conventional module architecture with newer and more costly high-temperature alternatives. More disruptive technological innovation in both module architecture and material selection is needed to provide smaller, lighter, cheaper, and more reliable modules for high temperature power electronics in both military and commercial applications.

II. New Power Module Concept

The objective of this paper is to introduce a hybrid power module packaging concept that allows 300°C operation to leverage recent advances in SiC and other wide band-gap semiconductor materials. We propose a new power module architecture based on the use of double metal leadframes, direct leadframe-to-chip bonding, and high temperature encapsulation. A half-bridge circuit, comprised of two active SiC switches and two anti-parallel SiC Schottky diodes, is used for the purpose of illustration in Fig. 2. The half-bridge circuit is the most basic building block in power electronics, which can be used in various combinations in electric vehicle motor drive inverters, power supply DC-DC converters, uninterruptible power supply DC/AC inverters, and many other applications. Nevertheless, the proposed module construction concept can be easily adapted to other circuit configurations such as three-phase inverters or even RF power circuits.



(a) (b)

Fig. 2: (a) A SiC half-bridge circuit. S1 and S2 are SiC power MOSFETs while D1 and D2 are SiC Schottky diodes. (b) The proposed concept of the new SiC half-bridge power module, which is comprised of four SiC chips bonded to a top and a bottom leadframe, and encapsulated with high-temperature injection-molded polymer or hydro-setting ceramics.

As shown in Fig. 2, two metal leadframes are used as both the external leads and the internal interconnect to the semiconductor chips enclosed in the power module. They may be formed with a metal stamping or machining process. Several metals or metal alloys were considered including molybdenum (Mo), Mo-Cu alloys, Mo-Cu laminates, copper-diamond or silver-diamond composites. As summarized in Table I, those materials provide excellent high temperature stability, adequate electrical and thermal conductivity, and a coefficient of thermal expansion (CTE) closely matching that of SiC and Si materials. The leadframes are plated with a thin nickel (Ni) metal layer and a thick Au layer to accommodate direct Au-Au bonding with SiC chips and enhance high-temperature stability. Alternatively, AlN-based DCB substrates can be used to serve as the top and/or bottom leadframes. The distinct advantage of using DCB ceramic substrates over metal leadframes is electrical isolation.

Table I: Leadframe Material Consideration

Material	Maximum Temperature °C	Electrical Resistivity μΩ-cm	Thermal Conductivity W/m-K	CTE ppm/k
Mo Cu: 0%	2615	5.1	139	5.1
MoCu Cu: 15%	1080	4.3	150	5.3
MoCu Cu: 30%	1020	3.7	190	7.5
MoCu Cu: 50%	1000	2.8	250	9.9
Copper-diamond	1020	9.1	470	6.7
Silver-diamond	990	8.5	550	5.8
AlN DBC	>1000	1.7 for Cu	180	4.5

Two methods are considered to attach the top and bottom sides of the SiC chip to leadframes: eutectic brazing and high temperature epoxy attachment. SiC devices with Ni as contact metal and thick Au film as cap metallization demonstrated stable operation at high temperatures [8]. In our proposed module design, a 3-4μm Au film will be formed on both the front and back sides of the SiC chips to accommodate direct Au-Au bonding with the Au-plated metal or DCB leadframes. The SiC chips are sandwiched between and bonded to the top and bottom leadframes using a brazing process. Au-Au bonding system is capable of reliable performance at 300°C or higher temperatures [8]. The bonding temperature essentially depends on the eutectic temperature of the alloy brazes or hard solders to be used. Several solder/braze materials are considered as summarized in Table II. For example, Au/Si and Au/In alloys exhibit an eutectic melting temperature of 363° C and 451° C respectively. The Au-based alloy "hard" solders or brazes have high strength and low elasticity but low fatigue resistance and little stress relief. Fortunately, this does not present a major challenge in our proposed module construction, since the leadframes have a CTE very close to that of SiC (4-5ppm/°C), and the leadframe/chip/leadframe sandwich structure should

Table II: Die Attachment Material Consideration

Material	Maximum Temperature °C	Electrical Resistivity μΩ-cm	Thermal Conductivity W/m-K	CTE ppm/k
AuGe 88/12	356	15.1	44	13
PbInAg 92.5/5/2.5	300	31	25	25
PbAgSn 97.5/1.5/1	309	27	30	30
PbSn 95/5	312	20	36	30
AuIn 81/19	487	20	28	14.7
Aremco Pyro-duct 597	927	200	9.1	17.3
Cotronics Duralco 124	343	200	7.2	n/a

Table III: Encapsulation Material Consideration

Material	Type	Maximum Temperature °C	Thermal Conductivity W/m-K	CTE ppm/k
Cotronics Durapot 863	Polymer	343	1.3	34
Ticona S135	LCP	350	n/a	n/a
Cermacast 575N	Hydro-set Al_2O_3 ceramic	1650	28	n/a
Cermacast 673N	Hydro-set SiC ceramic	1750	103	n/a

only experience a minimum amount of thermo-mechanical stress even at high temperatures. Alternatively, electrically conductive, silver or nickel filled, high temperature epoxy pastes, such as Aremco's Pyro-Duct™ 597 or Cotronics' Duralco™ 124 may be also used to bond the SiC chip to the leadframes. Those epoxy materials offer acceptable resistivity and can sustain high temperature operation.

It is critical to identify an encapsulation material that can sustain a temperature over 300°C yet with reasonable manufacturability. High temperature polymer such as Cotronics' Durapot 863 and hydro-set ceramic materials like Cermacast 673N are considered for this purpose, as listed in Table III.

III. Potential Benefits of the New Package

The proposed new hybrid power module concept has the following unique technical merits in comparison to the prior art in high temperature packaging solutions:

Simple material system and improved reliability – The new module essentially has only three basic elements: leadframes, SiC chips, and encapsulation, resulting in a much simpler material system than the prior-art hybrid power modules. The new module is completely free of unreliable wirebonds and soft solder joints. The nearly ideal direct Au-Au bonding between the CTE-matched SiC chips and Mo leadframes, when combined with the carefully selected low-stress, high-temperature, hermetic encapsulation material, should provide much improved long-term reliability for high-temperature applications.

High current and high power capability – The Mo or alloy leadframes serve as both the external leads and the internal interconnect to the SiC chips enclosed in the power module. Molybdenum has an electrical resistivity of 5.2μΩ-cm, slightly higher than Au (2.2μΩ-cm) or Cu (1.7μΩ-cm) but much lower than Kovar (49μΩ-cm) or Alloy 42 (70μΩ-cm). The Mo leadframes can be designed to have a thickness of 1-2 mm, roughly 2-25 times thicker than the direct bond or actively brazed Cu or Ni metallization on Al_2O_3 or AlN substrates (typically of 200-500 μm), and 40-120 times thicker than the co-fired Au or Pt metal films in LTCC substrates (typically less than 25 μm). The leadframes are also far more conductive than the 10-15 mil (in diameter) Al or 2-5 mil Au wirebonds commonly used in the prior-art power modules. As a result, the Mo or alloy leadframes provide low parasitic resistance and high current-carrying capability. We expect the new power module concept to offer a current rating up to several thousands of amperes.

Reduced package parasitic impedances – Eliminating Al or Au wirebonds in the new module will lead to a substantial reduction in both parasitic resistances and inductances, which usually cause voltage overshoots and excessive power losses in the operation of power modules.

Double-side cooling – The exposed parts of the leadframes also serve as heat spreaders or heat sinks in addition to their role of electrical leads, similar to the metal tab (the drain lead of a power MOSFET) of a conventional plastic package such as TO-220 or TO-247. Heat can be effectively removed from both sides of the SiC chips and transferred to the Mo leadframes and eventually to the ambient environment, resulting in lower operating junction temperatures. Double-side heat removal, when applied to wide band-gap semiconductors, can help completely eliminate the need for cooling subsystems and lead to substantial cost saving at the system level.

Ultra-thin form factor – The new module will have a typical thickness of 3-5 mm, which is roughly 5 times thinner than the prior-art power modules.

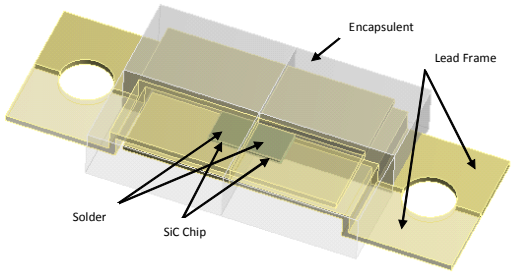


Fig. 3: Cut-away view of the single die diode module for FEA modeling and prototyping.

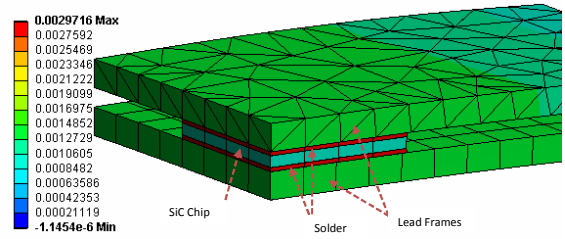


Fig. 4: Simulated thermal strain in the module. Note that the encapsulation is hidden in this view.

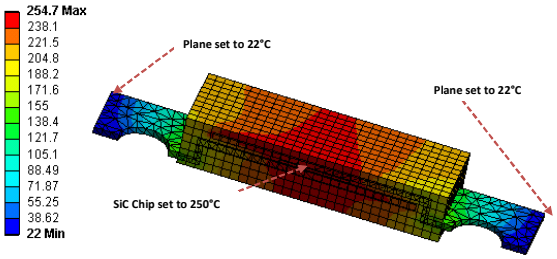


Fig. 4: Cut-away view and temperature distribution of the single die diode module for FEA modeling and prototyping.

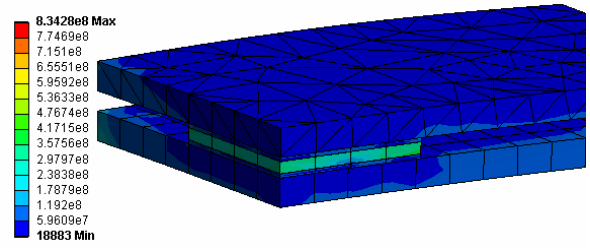


Fig. 5: Simulated equivalent stress (Von Mises) distribution in the module. Note that the encapsulation is hidden in this view.

IV. Modeling and Prototyping

The modeling and prototyping work was initially focused on a single chip SiC Scotty diode power module as shown in Fig. 3. Extensive finite element modeling (FEM) was carried out with ANSYS Multiphysics Software to determine the stress and strain distributions that arise due to thermal/mechanical property mismatch within the new package.

Fig. 4 shows a cut-away view and temperature distribution of the single die module. Boundary conditions at specific locations on the surface of and within the device were designed to simulate the anticipated service conditions. The initial thermal conditions implemented for this model were a constant temperature of 250°C on the SiC chip. The outside plane on each side of the lead frames is set to maintain a temperature of 22°C. The entire package is initially set at room temperature (22°C). The plating layers on each component were not modeled due to the negligible thermal expansion effect these plating layers would have on the base material. It is further assumed that thermal convection does not occur, having only purely conductive conditions present.

The thermal and mechanical stress was modeled in this module to identify potential location for failures which may originate in the solder joint due to high temperature combined with thermal mismatching of the adjoining materials. The maximum equivalent stress determined on the basis of distortion energy theory was found to be 110 MPa in the solder layer, and the maximum thermal strain was 0.297%, as shown in Figs. 4 and 5, respectively. Fig. 6 shows the modeled thermal strain in the whole package including the encapsulation and the full metal lead.

Using the results obtained from simulations, life prediction is determined for given service conditions. The fatigue analysis was performed using the Basquin's equation in conjunction with the Modified Goodman equation to determine the expected life given the present stress state. The thermal cycling was presumed to be completely tensile, from room temperature (zero stress state) to the SiC ramping to 250°C (max stress state). No dwell period was used. The fatigue analysis for these conditions resulted in a fatigue life of 55,875 cycles for the solder component of this package.

Fig. 7 shows a power module prototype with Mo leadframes and hydro-setting SiC ceramic encapsulation. A 2x2 mm2 SiC Schottky diode chip was used to make the prototype. Electrical characterization at high temperatures is underway.

V. Summary

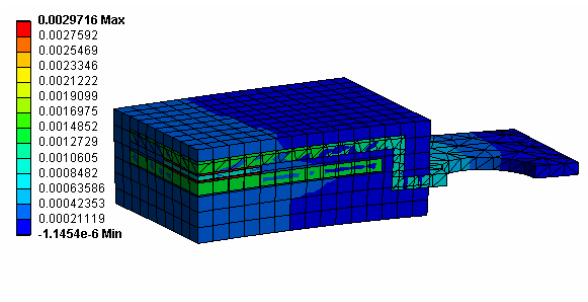


Fig. 6: Simulated thermal strain in the module including the encapsulation and external lead.

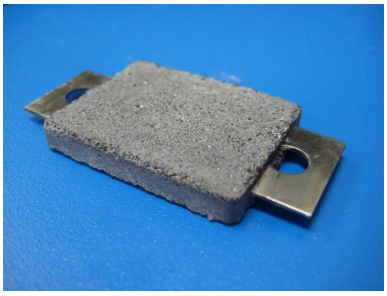


Fig. 7: A SiC diode power module prototype using Mo leadframes and SiC hydro-set ceramic encapsulation.

This paper proposes a new hybrid power module architecture that allows wide bandgap semiconductor power devices to operate at a junction temperature of 300°C. The concept is based on the use of double metal or DCB leadframes, direct leadframe-to-chip bonding, and high temperature encapsulation materials. The new power module concept has several advantages in comparison to the prior art high temperature packaging solutions including simplified material system and improved reliability, high current and high power capability, reduced package parasitic impedances, double side cooling, and ultra-thin form factor.

Acknowledgements

This work was supported in part by the U.S. National Science Foundation under Award ECS-0454835 and an EEEL grant from NIST. The authors wish to thank David Sheridan from SemiSouth for providing the SiC diode samples used in our prototypes.

References

1. S. E. Saddow and A. Agarwal, *Advances in Silicon Carbid Processing and Applications*, Artech House, 2004.
2. J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and Prospects for SiC Power MOSFETs", *IEEE Trans. Electron Devices*, Vol. 49, pp. 658-664, 2002.
3. J. B. Casady and R. W. Johnson, "Status of Silicon Carbide (SiC) as a Wide-Bandgap Semiconductor for High-Temperature Applications: A Review", *Solid-State Electronics*, Vol. 39, No. 10, pp.1409-1422, October, 1996.
4. R. C. Clarke and J. W. Palmour, "SiC Microwave Power Technologies", Proceedings *of IEEE*, Vol. 90, No. 6, pp. 987-992, June, 2002.
5. Cree Data Sheet, http://www.cree.com
6. S. Ryu, S. Krishnaswami, M. Das, B. Hull, J. Richmond, B. Heath, A. Agarwal, J. Palmour, and J. Scofield, "10.3 mΩ-cm^2, 2kV Power DMOSFETs in 4H-SiC", *Proc. ISPSD2005*, pp. 275-278, 2005.
7. "SiC defects slashed with new growth scheme", *Nature*, 26th August issue, page 1009.
8. R. Kirschman, *High Temperature Electronics*, IEEE Press, 1999.
9. F. P. McClusky, R. Grzybowski, and T. Podlesak, *High Temperature Electronics*, CRC Press, 1997.
10. National Research Council, *Materials for High Temperature Semiconductor Devices*, National Academy Press, 1995.
11. J. E. Sergent and C. A. Haper, *Hybrid Microelectronics Handbook*, McGraw-Hill, 1995.
12. Z. Lin and R.J. Yoon, "An AlN-based high temperature package for SiC devices: materials and processing", *Proceedings of International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces*, Page(s):156 – 159, March 16-18, 2005.
13. Ender Savrun, *Packaging Considerations for Very High Temperature Microsystems*, http://www.siennatech.com/Packaging%20Consi%C9icrosystems.pdf
14. T. O. Martin and T. R. Bloom, *High Temperature Aluminum Nitride Packaging*, http://www.ctscorp.com/techpapers/techpapers.htm