Thermal Network Component Models for 10 kV SiC Power Module Packages

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Abstract—**The DARPA WBGS-HPE program is developing 100 A, 10 kV SiC power modules to demonstrate the viability of a 2.75 MVA Solid State Power Substation that uses 10 kV, 20 kHz switching-capable devices. Thermal network component models for these modules are developed and are validated with temperature measurements obtained through various methods for a range of power dissipation levels. The models include the direct-bond-copper materials required to obtain 15 kV baseplate isolation and are parameterized in terms of the structural and material properties of the package to provide flexibility for different configurations. This enables the use of electro-thermal simulations to optimize SiC module parameters for specific system requirements.**

I. Introduction

Silicon carbide (SiC) material technology has advanced significantly in recent years, allowing the development of new high-voltage, high-frequency power semiconductor devices capable of 10 kV, 20 kHz switching [1]. The goal of the Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor – High Power Electronics (WBGS–HPE) Phase II program is to develop 100 A, 10 kV SiC power modules required to demonstrate a 2.75 MVA, 13.8 kV Solid State Power Substation (SSPS) in DARPA WBGS-HPE Phase III [2]. This paper develops and validates thermal network component models needed for the 100 A, 10 kV SiC module as well as other packages being developed by the HPE Phase II program. The module package model is combined with the electrical model for the 10 kV SiC semiconductor device models (MOSFET and JBS diode) developed in [3] to analyze the electro-thermal performance of the entire system and to aid in the selection of the final HPE Phase III module parameters.

An electro-thermal network simulation methodology was previously introduced using the Saber[2] simulator where the semiconductor models have a thermal terminal (in addition to the electrical terminals of conventional circuit simulation models) that is connected to a thermal network. This thermal network represents the semiconductor package and cooling system [4]. Many electro-thermal semiconductor models have been developed using this methodology including the IGBT electro-thermal model provided in Saber [5]. A thermal network component modeling methodology was also introduced in reference [6] that enables the development of compact (computationally efficient) thermal network component models for the semiconductor chip, package, and cooling system that are valid for the full range of applicable power dissipation functions. These methods have been applied in the past to model several different package and cooling system technologies [7, 8] and have been applied to simulate the electro-thermal performance of power converters [9, 10, 11].

II. Package Thermal Network Component Model Development

The models developed using the thermal network component method are parameterized in terms of the structural and material properties of the package and SiC devices within the package. This permits the manipulation of the model parameters to describe different module configurations which is particularly important in this work because the models are being used to aid in the optimization of the HPE Phase III module configuration. The models are developed by discretizing the heat diffusion equation using the effective heat flow area approach to represent the three dimensional symmetry conditions and using a quasi-logarithmic grid spacing to produce computationally efficient models that are valid for the full range of applicable power dissipation functions. Computationally efficient models are very important for this work because the models are being used to simulate the complex SSPS system with many SiC power devices and packages as described in [3].

The basic thermal stack structure of the packages analyzed for this work is presented in Fig. 1. The different materials that are used to achieve the 15 kV baseplate isolation required for the 10 kV devices are indicated. For simplicity, Fig. 1 shows a package with a single chip (e.g., a single JBS diode chip or single MOSFET chip). The voltage isolation stack consists of a direct-bond-copper (DBC) structure that is soldered to the chip and to the baseplate. The material properties and thickness of the layers within the voltage isolation stack, as well as the dimensions of the chip, represent the parameter set for the developed thermal network component model. The model uses these parameters to calculate the internal thermal resistances and thermal capacitances of the discretized heat diffusion equation. Fig. 2 shows an example of the location of some of the stack dimensional parameters that are needed by the model to compute its thermal characteristics.

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[1] NIST contribution; not subject to copyright. The devices discussed in this paper were produced by Cree Inc. under a DARPA HPE Phase II contract funded by Sharon Beerman-Curtin (DARPA) and monitored by Harry Dietrich (ONR).

[2] Saber software is a trademark of Synopsys Inc. This tool or any other commercial products that may be identified in this paper to adequately describe the performed experimental procedures or results do not necessarily imply any recommendation or endorsement by NIST.

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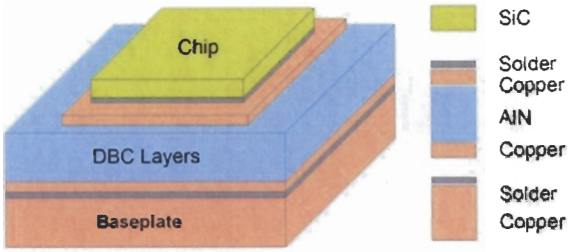

Figure 1. Description of the package layered material composition (dimensions not shown to scale; only for illustrative purposes).

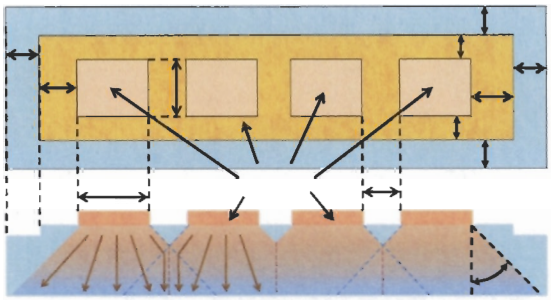

Figure 2. Description of some of the stack dimensions needed for the developed 10 kV module package thermal model. This would represent an example case having four chips. The arrows shown in the side view perspective indicate the heat flow path at the corners and also shows where the proximity of adjacent dice creates a reflective boundary condition for heat conduction.

The thermal network component model developed in this work makes use of multiple templates to represent the various structures within the package such as the chips, DBC stacks, and the baseplate. It can also be extended to incorporate templates for different heat sinks by interconnecting the needed templates. References [4-9] have already presented examples of how scripts are used to interconnect different thermal component model templates in order to represent a complete structure that may have single or multiple chips or DBC stacks.

Fig. 3 illustrates the effective heat flow area approach that is used to represent the three dimensional heat flow within the package DBC and baseplate layers [7]. Fig. 4(a) shows how each layer of the pyramidal-shaped lateral heat spreading profile of Fig. 3(a) is represented by a single thermal node or thermal element (for computational efficiency), where the three dimensional symmetry conditions are used to calculate the effective heat flow area for each node. These thermal nodes can be viewed as equivalent nodes of an electrical network, as shown in Fig. 4(b). The simulator solves the thermal and electrical network equations simultaneously.

Since the nodes vary in shape according to the given input dimensions and other parameters, it is easier to compute their surface area and volume if they are further decomposed into a group of common geometrical elements like the ones shown in Fig. 5. A single complete spherical cone is divided into four sections to represent the corners. A rectangular prism represents the volume directly beneath the semiconductor die. Semi-cylindrical portions extend form each side of the rectangular element except for the bottom node in the stack.

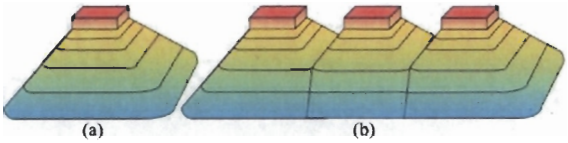

Figure 3. View of the pyramidal-shaped lateral heat spreading profile for (a) a single die and (b) multiple dice. Here (b) gives an idea of how the pyramidal profile will be overlapped on the sides by other components when more than one die is present. The amount of overlap will depend on the given die separation and the heat spreading angle.

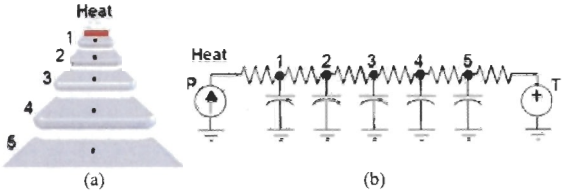

Figure 4. (a) Detailed view of the stack nodes and (b) thermal circuit representation for the same configuration. Heat generated from a power source (P) flows through the thermal circuit while the baseplate temperature (T) of the integrated fluid cooled heatsink.

The bottom node of the stack is assumed to be flat to represent the flat baseplate of the package, thus elements on the sides of the bottom node will be triangular in shape instead of being semi-cylindrical, and the corners will also be derived from a rectangular cone instead of from a spherical one.

The interaction of the heat flow between the multiple chips is illustrated in Fig. 2, where the downward arrows within the pyramidal volumes show the lateral heat flow interaction as the heat spreads to regions between chips [7]. This lateral interaction at the reflective boundary is managed by the model through the chip separation parameter that is given as input. The nodes beneath the dice on the ends of the series have a larger volume because they only encounter a reflective boundary of an adjacent die on one of their sides. (See the arrows pattern beneath the first of the four dice shown in Fig. 2.)

Fig. 6 shows the effect on the shape of the pyramidal elements due to the interaction of the reflective boundary condition between adjacent dice. As the die separation increases, the thermal conductance increases due to lateral heat spreading. For large die separations, the conductance does not continue to increase after the bottom node no longer has a reflective boundary due to interaction with any adjacent die.

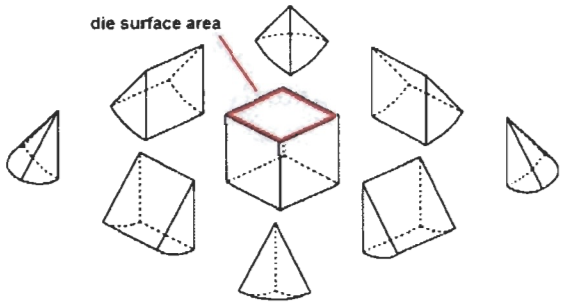

Figure 5. Geometrical decomposition of the thermal components used by the template to represent the pyramidal stack nodal structure shown in Fig. 3(a).

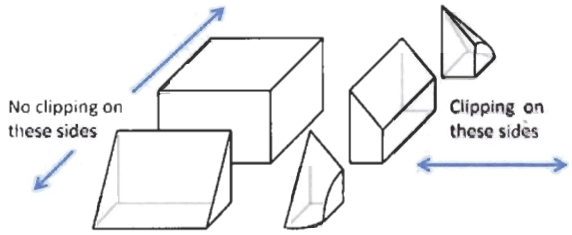

Figure 6. Partial view of the clipping due to the reflective boundary condition in Fig. 2 (bottom) and Fig. 3 (b). The pyramidal geometric decomposition for the single die case shown in Fig. 5 needs to be modified when the reflective boundary of an adjacent die is present during the multiple-chip case. The perspective shown in this diagram is from the point of view of only one corner for simplicity purposes.

This is depicted in the lateral view shown in Fig. 7 of the pyramidal structure as the separation increases. Fig. 8 is an example multi-chip module configuration for different die separations indicating the predicted thermal behavior of the module. In this example, the SiC active die area dimensions are 0.39 cm by 0.39 cm and a constant 100 W power pulse is applied to an arrangement of 10 devices in parallel. The baseplate bottom temperature is 25 °C in all the cases. For the case of no separation, the temperature rises over 17 °C, while the temperature only rises by 15 °C for cases with more than 3 mm spacing.

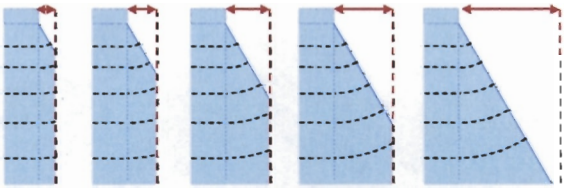

Figure 7. Die separation affects the volume of each node depending on both the distance between dice and the stack heat spreading angle. Once the separation goes beyond the stack base the reflective boundary ceases to affect the nodes beneath each die.

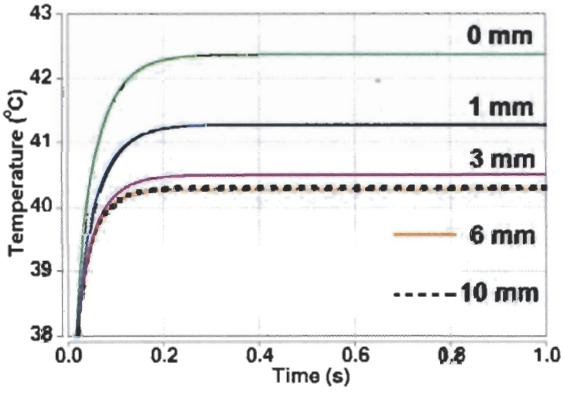

Figure 8. Simulation results for a 10-chip module when a 100 W constant power level is applied as the die separation is varied between 0 mm and 10 mm. In all cases the baseplate temperature is 25 °C and the heat spreading angle is 50°.

III. Power Device Package Measurements

The thermal network component models developed in this work are compared with experiments to ensure that they are applicable for the full range of power dissipation functions that can occur for the package or module being modeled. For low-speed power transients close to steady-state conditions, thermocouples and infrared thermal images of the chip surface are adequate. However, various methods are required to validate the different frequencies defining the transient thermal response.

For the intermediate frequencies representing 60 Hz or system start-up power cycles, high-speed temperature-sensitive parameter (TSP) measurements [12, 13] are employed as described next. The circuit and procedure required for the high speed TSP method described in reference [12] for the silicon IGBT has been adapted to characterize the thermal performance of SiC power MOSFETs in the work described in this paper. As an example, Fig. 9 shows a captured TSP voltage response for 100 W, 5 ms power pulses with a 50 ms period, and Fig. 10 shows the temperature profile obtained according to the respective calibration curves at this power level [12].

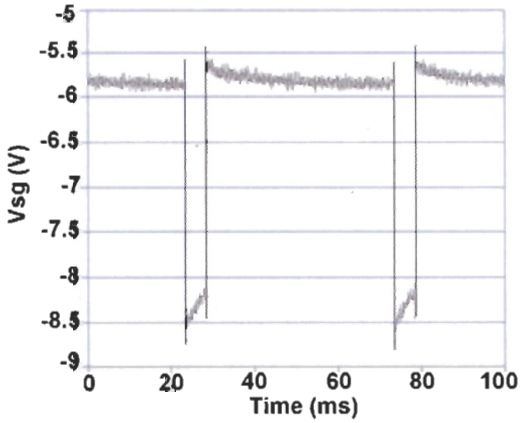

Figure 9. Measurement example for a temperature-sensitive parameter (Vsg) that is used to validate the thermal model of a SiC power MOSFET.

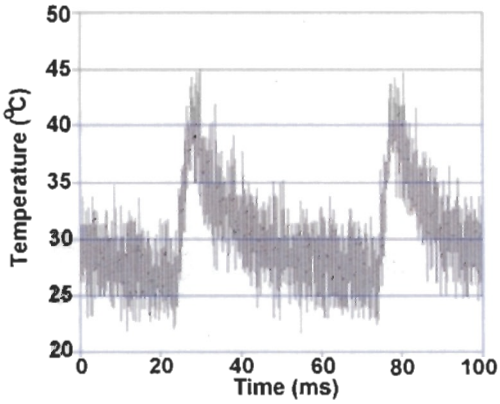

Figure 10. Equivalent temperature profile for the TSP measurement shown in Fig. 9.

Fig. 11 and Fig. 12 show comparisons of measured and simulated TSP junction temperature waveforms for different power levels and pulse widths. The lower 200 W test in Fig. 11 was performed with a baseplate temperature of 30 °C, while the upper 300 W test had a baseplate temperature of 75 °C. The simulation was able to predict the thermal behavior of the device under similar power level and room temperature conditions in both cases. Note that the thermal conductivities of the materials, especially the SiC, are temperature dependent and are influenced by the temperature offset. The 100 W test measurements depicted in Fig. 12 is the same TSP measurement shown previously in Fig. 10, but they were averaged to reduce the waveform noise for the comparison. Both the heating and cooling portions of the transient response were compared in this case. This simulation also predicts the measured behavior with acceptable concordance.

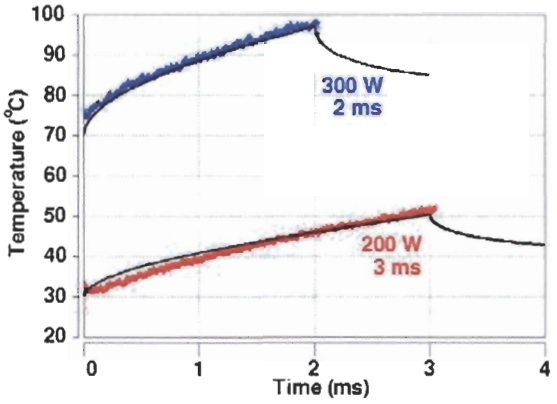

Figure 11. Measured (jagged lines) versus simulated (solid smooth lines) results for various power levels. Power level magnitude and pulse width duration are identified. In these cases the emphasis is focused only on the heating period of the response.

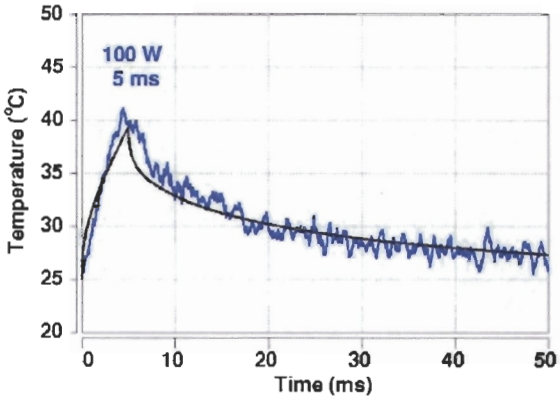

Figure 12. Measurement (jagged line) and simulation (solid line) comparing the temperature profile of the device junction once the heat generated by the applied pulse begins to dissipate through the stack.

High-speed thermal imaging is required for the nearly-adiabatic chip heating that occurs during high-frequency switching events or fault conditions [14]. Fig. 13 shows a picture of a SiC MOSFET used for the infrared-thermal measurements below. Since the device is made of different materials and each material has a different emissivity, a thin carbon-black layer is applied to the surface. Fig. 14 shows one of the 200 captured image frames from a validation experiment where a power pulse of 180 W was applied during 1 ms. The series of images are used to show how the heat changed with time as it was distributed through the SiC MOSFET surface before, during, and after the power pulse was applied. The surface temperature shown in Fig. 14 has a detected maximum of 89.2 °C. That behavior is the typical heat distribution observed in other similar devices analyzed using the same method. The low temperatures in the lower portion of the image are mainly from the wirebonds that show a different emissivity during the capture. They also tend to block or interfere with the surface measurements from the areas located below them.

The image in Fig. 14 was generated by acquiring 32 x 32 sampling locations, each 70 µm apart, vertically and horizontally. In each one of those locations a transient temperature waveform was captured by the high-speed infrared camera, and they were all combined into a series of time-consecutive X-Y arrays to generate the 200 individual images that the test captured.

The transient waveform corresponding to the hotspot location shown in Fig. 14 (oval shape close to the center of the image) is presented in Fig. 15. At the same time, the thermal transient waveforms for the array locations surrounding the hotspot are plotted together to generate an "envelope" of temperature measurements in the region of the hotspot.

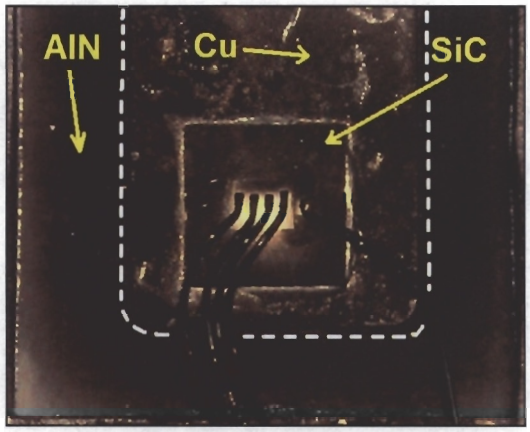

Figure 13. Picture of the actual MOSFET used for the infrared measurements used for validation purposes. Four drain wirebonds and one gate wirebond are shown in the lower half of the image. Stack materials are identified. The device was covered with a thin layer of carbon to improve the emissivity measurements acquired by the infrared camera during the measurements.

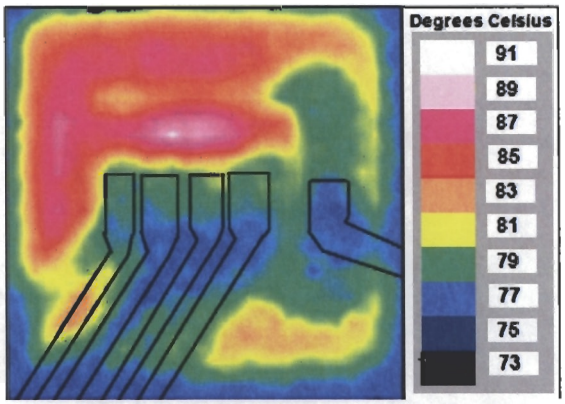

Figure 14. Infrared surface temperature mapping for a SiC MOSFET used for the thermal model validation. A hotspot close to the drain wirebond contacts was detected with a maximum temperature of 89.2 °C. Notice that a lower temperature between 85 °C and 87 °C is more evenly distributed around the hotspot and the upper left corner of the captured image. The depicted wirebonds location (black lines) is approximate and given only as a reference to be compared with Fig. 13.

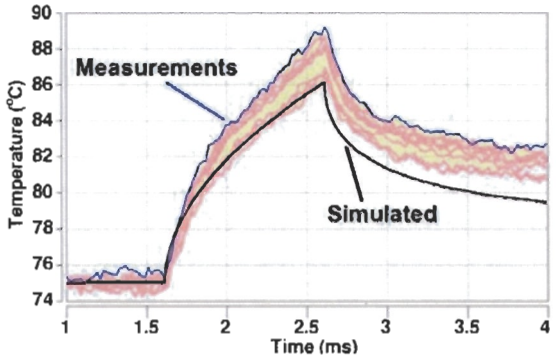

Figure 15. Comparison of the simulated power level used to obtain the infrared transient temperature measurements for the pixel location with the highest temperature shown in Fig.14 and its surrounding pixels. A 180 W power pulse was applied during 1 ms with a starting baseplate temperature of 75 °C.

The same power level was simulated with the thermal network components model template for validation, and the results are shown as a solid smooth line in Fig. 15. The baseplate temperature for this experiment was 75 °C. Notice that the hotspot does not represent necessarily the average temperature shown throughout the device surface, which according to the temperature color legend ranges mainly between 85 °C and 87 °C in most of this area. Based on this observation, the simulation output maximum of 86 °C is a good estimate of the internal semiconductor temperature under those power conditions, thus reinforcing the previous TSP validations that show the accuracy of the model template.

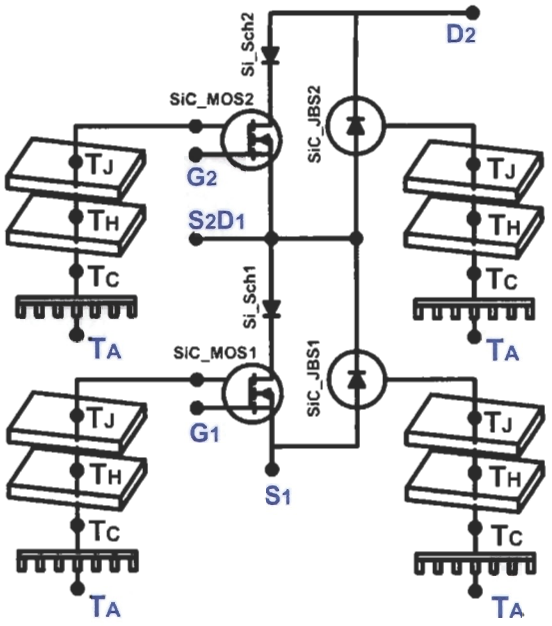

Figure 16. General circuit topology of a 100 A, 10 kV half-bridge SiC MOSFET/JBS power module that was simulated using the thermal network components model methodology.

IV. Electro-Thermal Power Module Simulation

The schematic shown in Fig. 16 depicts the electro-thermal 100 A, 10 kV half-bridge SiC MOSFET/JBS power module model [15] that is simulated using the thermal network component approach as described below.

The thermal models for the SiC semiconductors and their respective DBC thermal stack models are attached to the thermal connection node of each power semiconductor electrical network element in the half-bridge module. A full electro-thermal simulation is performed in Saber for a module configuration that has 10 MOSFETs in parallel. The junction temperature can be analyzed as the devices are switched at 20 kHz during a 60 Hz inverter cycle. These test conditions aid in determining that the devices are operating in safe temperature ranges and that the temperature cycles are in the acceptable range. Temperature fluctuations during the power cycles may cause stress in wire bonds and within the module materials with mismatched thermal expansion coefficients that could lead to reliability issues.

Fig. 17 shows the results of changing the dice separation from 0 mm to 10 mm. A configuration where all dice are closer together also produces higher temperature because the reflective boundary condition between adjacent dice reduces the effective area for heat conduction. These simulations show the combined heating effects that occur during the fast switching of the MOSFETs and during the lower heat dissipation during the on-state portion of each cycle.

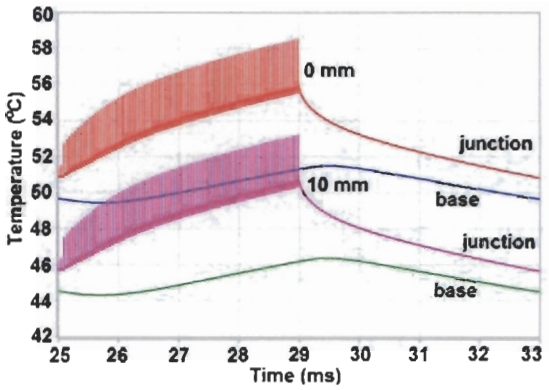

Figure 17. Half-bridge 10 kV, 100 A module electro-thermal simulation results showing how junction and stack base temperatures are affected by changing the die separation. The baseplate temperature was 25 °C in both cases.

V. Conclusions

Thermal network component models have been developed based upon scripts that are applicable to multiple package configurations for 10 kV SiC module packages. Model parameters can be changed to represent different chip size areas, material thicknesses, and number of chips. Temperature measurements are performed using various methods to validate the models for the full range of applicable power dissipation functions. For the intermediate frequencies representing 60 Hz or system start-up power cycles, high-speed temperature-sensitive parameter measurements are employed, whereas a high speed thermal imaging system is used to validate the models for near-adiabatic heating conditions. The flexibility and wide range of validity of the models enables optimization of SiC module parameters to meet system requirements using electro-thermal simulations.

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