High-Speed Nb/Nb–Si/Nb Josephson Junctions for Superconductive Digital Electronics

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***Abstract*—Josephson junctions with cosputtered amorphous Nb–Si barriers are being developed at NIST for use in voltage standard circuits. These junctions have the potential for a wide range of applications beyond voltage standards because their electrical properties can be tuned by controlling both the composition and the thickness of the barrier. If the composition of the barrier is tuned so that the resistivity is close to the metal-insulator transition, the high resistivity allows junctions with a large characteristic voltage and reproducible critical-current densities, which should be ideal for high-speed digital superconductive device applications. Because these junctions are intrinsically shunted, there is no need for external shunt resistors, which could start to become a limitation as the development of devices leads to higher critical-current densities and greater circuit densities. Presently, the AlO_x-barrier junctions used in digital superconducting electronics suffer from poor reproducibility, particularly for the high critical-current densities needed for high-speed applications. In this paper, amorphous Nb–Si barrier junctions with characteristic voltages on the order of 1 mV and characteristic frequencies on the order of hundreds of gigahertz are demonstrated. This junction technology looks promising for applications in high-speed digital electronics.**

***Index Terms*—Amorphous alloy, Josephson junctions, superconducting devices.**

I. Introduction

DUE to its stability and relatively high critical temperature, Nb has been the superconductor of choice for the development of Josephson junction electronics. In the case of digital superconducting electronics, the currently preferred choice of junctions is Nb-based superconductor–insulator–superconductor (SIS) junctions, because they have a long history of providing robust Josephson junctions for a wide variety of applications [1]. These junctions have large intrinsic hysteresis and require external shunting in order to be critically damped. Externally shunted junctions have a disadvantage over self-shunted junctions in that the external shunts increase the complexity of the fabrication process and circuit layout, reduce the circuit density, and introduce parasitic inductances, all of which can become limitations as new developments with higher current density junctions start to require smaller and more densely packed devices. These difficulties are not present in self-shunted and nonhysteretic junctions, such as the superconductor-normal metal-superconductor (SNS) junctions that are widely used in voltage standard applications. The main reason such junctions have not been used in high-speed applications is that they generally are not capable of high-speed operation due to their low characteristic frequency f_c. The speed of the junction is given by the characteristic frequency, which, in turn, is related to the characteristic voltage V_c through $V_c = (h/2e)f_c$, where h is Planck's constant and e is the electronic charge.

Another challenge with SNS junctions is the exponential dependence with barrier thickness of both the critical current I_c and the characteristic voltage V_c, which is also the product of I_c and the normal resistance R_n. Large characteristic voltages, and thus operating speeds, require thin normal-metal barriers because of their typically low resistivity. Unfortunately, such junctions also have impractically large values of the critical-current density J_c, so that junctions with practical 100-μA critical currents must have an area far smaller than $(1\ \mu\text{m})^2$, dimensions that are very challenging to reproducibly and uniformly fabricate. These difficulties can be solved by making junctions with a high-resistivity barrier that have high-speed electrical properties and practical critical-current density.

There are a number of approaches to making such junctions. One is to use silicide-based barriers that contain a small amount of Nb or other metal and become an insulator at sufficiently low temperature [2]–[4]. Niobium–silicide barrier junctions have the additional advantage of having small specific capacitance, so that the junctions' current–voltage (I–V) characteristics have small or nonexistent hysteresis. This same approach has been used with other high-resistivity barrier materials, including TiN_x, NbN_x, and TaN_x [5]–[7]. For these barrier materials, the resistivity is controlled by adjusting the nitrogen pressure in the deposition chamber while the material is being deposited with reactive sputtering. Junctions with these nitride-barrier materials have been demonstrated, although reproducibility and suitably low hysteresis have yet to be shown for high-characteristic voltage junctions. Another approach to increasing junction damping is based on Nb/Al–AlO_x/Nb junctions that have a thick Al layer and one thin oxide layer, and Nb/Al/AlO_x/Al/AlO_x/Al/Nb SINIS junctions [8]–[10]. Unfortunately, these junctions suffer from poor reproducibility, as do most other junctions based on aluminum–oxide barriers [11].

Results thus far with Nb–Si-barrier junctions show good uniformity across a wafer and good reproducibility from run to run. In fact, using the term "SNS" to describe these junctions is inaccurate, because the barrier is actually no longer a "normal-

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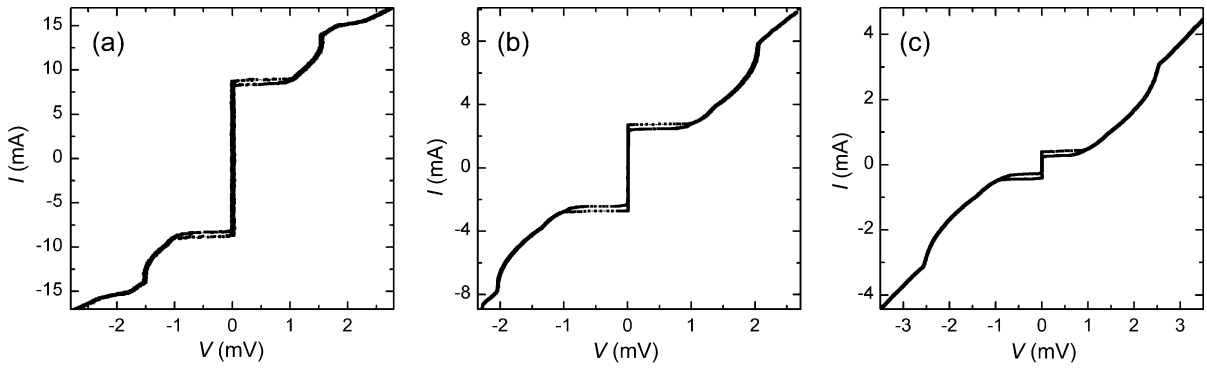

Fig. 1. I–V curves of single junctions with lateral dimensions $2.5\ \mu\text{m} \times 2.5\ \mu\text{m}$ for barrier thicknesses (a) 5, (b) 6, and (c) 7.5 nm having respective characteristic voltages V_c of 2.3, 0.83, and 0.29 mV.

metal," but a poor conductor near the metal-insulator transition (M-I-T). In order to distinguish these barriers from typical normal metals, we adopt the acronym "SCS," where the "C" refers to a conductor material, in our case a nearly insulating poor conductor. The Nb–Si barrier's higher resistivity, being beyond the M-I-T, has the additional beneficial side effect of reduced temperature dependence of the critical current. Junctions with metallic barriers have a rapid rise in critical current as the temperature is decreased. Near the M-I-T, the rapid increase in barrier resistance (or reduced transparency) counteracts this increase, so that the temperature dependence of I_c in SCS junctions approaches the weak temperature dependence of I_c in SIS junctions. For $\text{Nb}_x\text{Si}_{1-x}$, the value of the concentration at which the material crosses the M-I-T is $x \sim 11\%$ [2].

NIST has been developing SNS junctions with amorphous Nb–Si as the barrier material for use with voltage standard devices, which require larger values of I_c and smaller V_c than is typically desired for high-speed digital superconductive electronics (HDSCE). However, because the composition of the barrier can be tuned over a wide range on both sides of the M-I-T, a variety of high-quality, highly reproducible SCS and SIS junctions may be fabricated by changing the barrier composition. By controlling the relative power of the sputtering guns during cosputtering of Nb and Si, the composition of the amorphous barrier may be continuously varied. For example, decreasing the Nb content increases the resistivity of the barrier. For a given value of J_c, the V_c increases as the resistivity of the barrier increases. For this work, a fixed composition of 5% Nb was used and values of V_c above 1 mV were obtained in self-shunted silicide-barrier junctions with critical-current densities on the order of 1 $\text{mA}/\mu\text{m}^2$. Our recent results lead us to propose this type of junction as a promising candidate for HDSCE applications.

II. Fabrication and Measurements

Details of the Nb–Si-barrier junction fabrication process have previously been described [12]. In order to make high-speed junctions, some modifications to the standard fabrication process are needed. After the Nb base-electrode deposition, an RF-plasma sputter-cleaning step is performed to obtain a smooth Nb surface on which the barrier is deposited. This step produces smoother and more uniform barriers. Thermal annealing of the barrier is known to reduce its resistivity and the junction critical-current density, with a net reduction of J_c and V_c [13]. The wafer temperature is maintained below 150 °C in order to minimize these annealing effects. The composition of the barrier is controlled by the power applied to the Nb and Si sputtering guns. For the data presented in this report, the power was fixed at 15 W for Nb and 200 W for Si, which gave a composition of approximately $\text{Nb}_{0.05}\text{Si}_{0.95}$.

Junctions were fabricated with different lateral dimensions ranging from $1.5\ \mu\text{m} \times 1.5\ \mu\text{m}$ to $10\ \mu\text{m} \times 10\ \mu\text{m}$. Both single junctions and 400-junction series arrays were fabricated and measured. Measured I–V curves were qualitatively similar for junctions and arrays that had the same composition. All measurements were made at a temperature of 4 K by immersion in liquid helium. For currents greater than I_c, the curves show a nonlinear regime that transitions to a linear response for voltages greater than the superconducting gap of the electrodes. The value of R_n is obtained from the linear regime of the I–V curves.

Fig. 1 shows I–V curves of single junctions with the same $2.5\ \mu\text{m} \times 2.5\ \mu\text{m}$ lateral dimension and three different barrier thicknesses: 5, 6, and 7.5 nm. The curves show small hysteresis and high values for the normal resistance. For SIS junctions, the conductivity below the gap can be quantified through the subgap resistance $R_{\text{sg}} = 2\ \text{mV}/I(2\ \text{mV})$. The junction normal resistance R_n is obtained from the I–V characteristic at voltages greater than $2\Delta/e$, where 2Δ is the energy gap of the superconductor. Our junctions have rather different I–V characteristics, and the subgap current around 2 mV (and R_{sg}) shows a large variation, as can be seen in Figs. 1 and 2. For our junctions, the values of R_n are obtained from the linear region of the I–V curves above the gap inflexion point.

We observe heating effects due to the high J_cs, as can be seen in Fig. 1 on the reduced gap as the barrier thickness is decreased. Consequently, for the thinnest barriers it was difficult to determine the values of R_n. Only for the smallest junctions we could obtain estimates of R_n from the linear region of the I–V curves just above the sharp peak of $\Delta I/\Delta V$ marking the energy gap, similar to the one shown in Fig. 2.

The I–V curves show a weak subgap structure appearing as a small kink in the curve. This structure can be seen more clearly in a $\Delta V/\Delta I$ versus voltage plot such as Fig. 2, which shows this relation for the single junction whose I–V curve appears in Fig. 1(b). Small variations in the voltage of the subgap feature

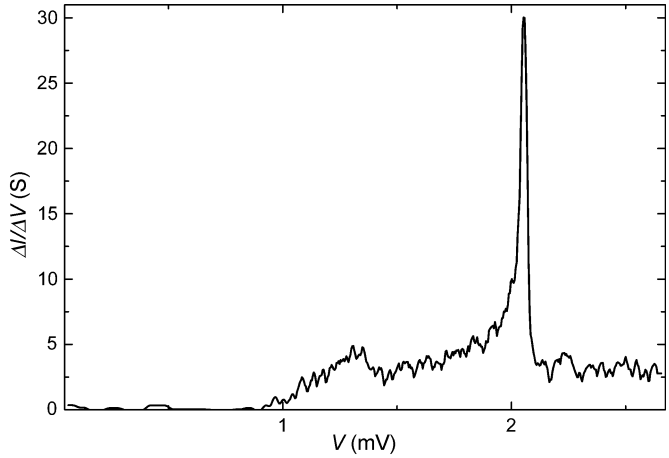

Fig. 2. Plot of $\Delta I/\Delta V$ versus voltage for a single junction with dimensions $2.5\ \mu\text{m} \times 2.5\ \mu\text{m} \times 6$ nm showing a weak subgap structure with a peak around 1.3 mV. Around 2 mV, the plot shows a strong variation; for this reason, we use the region after the strong peak to obtain the value of R_n.

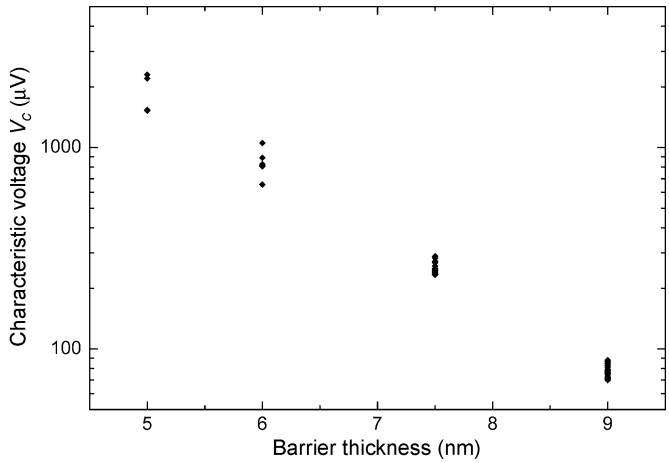

Fig. 3. Plot of V_c versus junction-barrier thickness. Data include results from junctions of different lateral sizes. Large scatter for thin barriers is due to difficulty in evaluating R_n.

are observed between wafers. One explanation of the subgap structure is the presence of multiple Andreev reflections between superconducting electrodes, which give rise to current steps in the I–V characteristics at voltages equal to $2\Delta/ne$, where n is an integer equal to the number of reflections in the multiple Andreev reflection cycle [14], [17].

Fig. 3 shows the values of V_c versus barrier thickness that were measured from the I–V curves of single junctions as well as arrays, and includes junctions of different areas. The highest values of V_c are on the order of 1 mV, which give a characteristic frequency near 500 GHz. The scatter in the data gives an indication of the uniformity and the run-to-run reproducibility of the fabrication process. The values of V_c for junctions with 5- and 6-nm-thick barriers show a large variance due to the difficulty in measuring the value of R_n. For these junctions, J_cs were the highest, and the smallest junctions fabricated had an area of $1.5\ \mu\text{m} \times 1.5\ \mu\text{m}$ and $2\ \mu\text{m} \times 2\ \mu\text{m}$, respectively, so that large currents were needed to bias the junctions into the linear part of the I–V curves from which R_n was obtained. For the rest of the junctions that were measured, the uniformity in values of

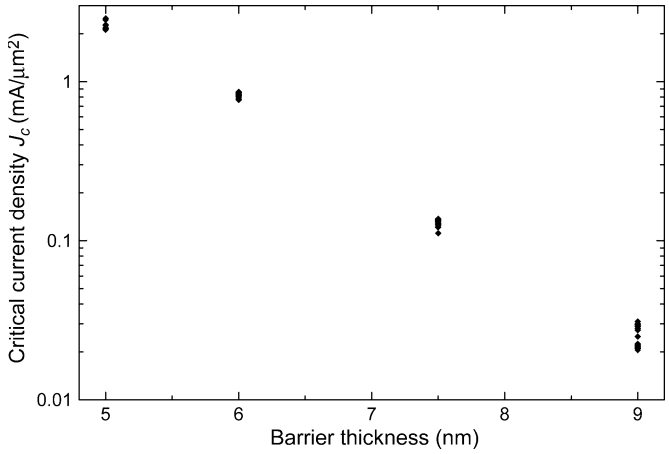

Fig. 4. Plot of critical-current density versus junction barrier thickness for $Nb_{0.05}Si_{0.95}$ barrier devices.

V_c is within 8% (standard deviation), considering junctions of different sizes, in arrays, and as single junctions.

Fig. 4 shows the critical-current density versus barrier thickness. In this case, the uncertainty in measurement is smaller and we can see a good uniformity for all thicknesses. On-chip uniformity is within 6%. For the 9-nm barrier junctions, two wafers were prepared 7 months apart; the discrepancy, 15%, could be attributed to drift in deposition rates in the sputtering system due to aging of the targets. With careful measurement and control of rates, we believe this can be readily improved. The data of Figs. 3 and 4 show that both J_c and V_c follow an exponential decay with barrier thickness. The data suggest that this type of junction has good reproducibility within a chip, within a wafer, and between samples fabricated on different wafers, months apart in time. The wafers for this study were fabricated over a period of 10 months.

It should be noted that the data presented in Figs. 3 and 4 are for a fixed composition of the barrier. By changing the composition, similar plots of current density and characteristic voltage can be obtained by correctly tuning the barrier thickness, such as a higher Nb concentration with thicker barriers. This ability to tune the barrier should allow one to obtain junctions with similarly high V_cs, as shown here, and lower J_cs, similar to the state-of-the-art tunnel junctions with $J_c\text{s} \sim (10 - 20)$ kA/cm^2 [15], [16]. Because the composition should remain stable (as suggested by the small amount of scatter in these plots), junctions fabricated with different compositions should also retain the good uniformity and reproducibility that has been shown here.

III. Conclusion

We have fabricated junctions using an amorphous Nb–Si barrier whose electrical conductivity is close to the metal-insulator transition. The high resistivity of this material allows the fabrication of junctions with high values of characteristic voltage, while maintaining reasonable values for the critical current density, which still enable junctions with useful electrical properties that have micrometer-scale lateral dimensions. These junctions' electrical properties may be of use in superconductive digital circuits because they should be capable of generating

high-speed pulses, they have small hysteresis, and they are self-shunted. Limited results so far suggest good reproducibility and stability, making possible the fabrication and design of large-scale high-speed superconductive digital circuits.

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