Nanotechnology **20** (2009) 085304 (7pp) doi:10.1088/0957-4484/20/8/085304

Controlled formation and resistivity scaling of nickel silicide nanolines

Bin Li[1,5], Zhiquan Luo[1], Li Shi[2], JiPing Zhou[3], Lew Rabenberg[2], Paul S Ho[1], Richard A Allen[4] and Michael W Cresswell[4]

[1] Microelectronics Research Center, University of Texas, Austin, TX 78758, USA
[2] Texas Materials Institute and Department of Mechanical Engineering, The University of Texas at Austin, 1 University Station C2200, Austin, TX 78712, USA
[3] Texas Materials Institute, The University of Texas at Austin, ENS 31N, Mail Code C2201, Austin, TX 78712, USA
[4] Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899, USA

Received 4 October 2008, in final form 17 December 2008
Published 2 February 2009
Online at stacks.iop.org/Nano/20/085304

Abstract
We demonstrate a top-down method for fabricating nickel mono-silicide (NiSi) nanolines (also referred to as nanowires) with smooth sidewalls and line widths down to 15 nm. Four-probe electrical measurements reveal that the room temperature electrical resistivity of the NiSi nanolines remains constant as the line widths are reduced to 23 nm. The resistivity at cryogenic temperatures is found to increase with decreasing line width. This finding can be attributed to electron scattering at the sidewalls and is used to deduce an electron mean free path of 6.3 nm for NiSi at room temperature. The results suggest that NiSi nanolines with smooth sidewalls are able to meet the requirements for implementation at the 22 nm technology node without degradation of device performance.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

As devices continue to scale below the 65 and 45 nm technology nodes, the formation of transition metal silicides and their electrical properties at the nanoscale generate significant interest. Metal silicides are used in the self-aligned silicide (SALICIDE) process to form gate and ohmic contacts in complementary metal-oxide-semiconductor (CMOS) devices [1–4]. The NiSi phase is of particular interest as a gate and contact material beyond the 45 nm node due to its low resistivity, low silicon consumption, and low formation temperature [5–8]. NiSi nanolines[6] (NiSi NLs) formed on silicon nanolines (Si NLs) by a bottom-up growth process were found to have a low resistivity of $\sim$10 $\mu\Omega$ cm at room temperature and a high critical current capacity of 10^8 A cm^{-2} for feature sizes down to 29 nm [8, 9]. However, it can be a challenge to employ NiSi NLs grown by a bottom-up process for ultra-large-scale integrated (ULSI) devices. For this reason, a top-down process has recently been applied to fabricate NiSi NLs using focused ion beam patterning [10]. An abrupt increase in the room temperature resistivity from 15 to 22.7 $\mu\Omega$ cm was observed as the line width was reduced from 50 to 32 nm. These measurements used Pt contacts, and the resistivity jump was attributed to the effect of grain boundary scattering on electron transport in the NiSi nanolines (NiSi NLs). Interestingly, Ni_2Si NLs formed by a top-down process using sidewall transfer lithography (STL) did not show a resistivity jump down to 37.5 nm line width [11]. In a recent development of the Ni-fully silicided (FUSI) gate process, a gate-width effect on the silicide composition was observed. A Ni-rich silicide was formed at short gate widths below 100 nm, leading to increased resistivity and work function and to degradation of the device performance [12, 13]. These studies of NiSi NLs formed by top-down processes pose fundamental questions concerning the effect of scaling on phase formation and its impact on the resistivity and electron transport in Ni silicides.

[5] Present address: Intel, 5000 West Chandler Boulevard, Chandler, AZ 85226, USA.
[6] These are also often referred to as nanowires (NWs).

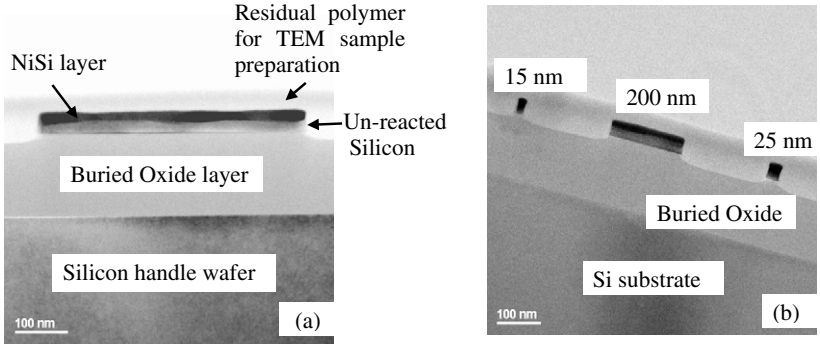


Figure 1. (a) Low-magnification cross-sectional TEM image of the 500 nm wide silicide lines on SOI wafer, showing a ∼17 nm thick silicide layer formed in the (110) device layer. (b) Cross-sectional TEM image of a set of silicide lines on SOI wafer, showing that the silicide layer thickness on the fine lines (25 nm line and 15 nm line) was larger than on the 200 nm wide lines.

2. Fabrication and characterization

In this work, NiSi NLs were formed by annealing a Ni coating layer deposited on silicon nanolines (Si NLs). The Si NLs were fabricated on a (110) SOI wafer using e-beam lithography and anisotropic wet etching (AWE). AWE is a pattern transfer method, which when combined with high-resolution e-beam lithography (EBL) can yield very high-quality Si NLs [14, 15]. The Si NLs have well-controlled (111) sidewalls that are vertical and nearly atomically flat, without the usual damage induced by ion bombardment from reactive ion etching (RIE) [15]. The Si NLs were used as the base structure to fabricate NiSi NLs by material reaction down to a line width of 23 nm.

The fabrication of the Si NLs began with chemical vapor deposition of a 9 nm thick SiO_2 film followed by thermal evaporation of a 15 nm thick Cr film onto a (110) SOI wafer. The Cr layer served as a hard mask for pattern transfer while the SiO_2 layer was used as a buffer to prevent Cr alloying with the silicon device layer. A positive tone EBL resist was spun onto the Cr layer, and the resist pattern was transferred to the Cr layer by plasma etching through the oxide layer. Subsequently, the residual resist was removed and tetra-methyl-ammonium hydroxide (TMAH) was used for anisotropic etching of silicon along the {111} planes, with Cr as the etching mask and the buried oxide layer as the etch stop layer. When the pattern features were aligned with one of the ⟨112⟩ directions in the (110) plane of the wafer, the anisotropic wet etch formed vertical and nearly atomically flat sidewalls on the silicon lines. After anisotropic etching, the Cr mask was etched away and the oxide buffer layer was removed by RIE, followed by wet etching using a diluted buffered oxide etchant. This two-step process avoided the etching undercut of the buried oxide layer and also cleaned the silicon surface after plasma etch of the oxide buffer layer.

In order to form Ni silicides, a Ni overlayer was e-beam evaporated onto the Si NLs at a base pressure of about 10^{-4} Pa, then reacted to form NiSi using a two-step annealing process to suppress the lateral silicide growth [13, 16]. The initial silicidation was performed at 320 °C to minimize the thermal budget. Following the initial silicidation, the unreacted Ni was removed using a selective (H_2O_2:H_2SO_4:H_2O = 1:1:4) etchant, and the silicide was converted to orthorhombic NiSi in a second anneal at 420 °C for 1 min. Sheet resistance measurements of blanket NiSi films on (110) wafers showed no resistance change before and after the Ni removal step, indicating that the entire Ni overlayer was reacted during the first annealing step.

The NiSi NLs were formed by reacting 8 nm Ni layers deposited on a set of Si NLs fabricated in the device layer of the (110) SOI wafer. Figure 1 shows low-magnification cross-sectional TEM images of the 500, 200, 25, and 15 nm wide silicide lines formed on the SOI wafer. The thickness of the Si device layer and the buried oxide layer were 34 nm and 153 nm, respectively. Figure 2(a) shows a higher-magnification TEM image of the interface between silicide and unreacted silicon at the center of a 500 nm wide silicide line. After annealing, a silicide layer of about 17 nm thickness was formed on top of the 21 nm thick unreacted (110) silicon layer. The thickness of the silicide layer was the same as that of a NiSi film formed on a silicon wafer, which is 2.2 times the thickness of the as-deposited Ni layer [7]. The sheet resistance of the NiSi film was measured to be 11.8Ω/□, corresponding to a resistivity of about 20 $\mu\Omega$ cm; this is consistent with values reported for NiSi films formed on single-crystal Si substrates [3, 7, 17].

The HRTEM image of the interface area shown in figure 2(a) and the corresponding FFT in figure 2(b) identify the silicide layer to be orthorhombic NiSi. In the FFT, the $[2\bar{3}1]$ zone axis of the NiSi is parallel to the $[\bar{1}12]$ zone axis of the Si. In figure 2(c), the Ni silicide formed at the line edge was found to have a 'beak' shape, and a similar trapezoidal feature was observed in the 15 nm silicide line as shown in figure 2(d). Although no lattice images were obtained from the 15 nm wide Ni silicide line in figure 2(d), energy-dispersive x-ray (EDS) measurements showed a Ni:Si composition ratio identical to that of the 500 nm line. Resistivity was measured to be 18–20 $\mu\Omega$ cm, similar to that of the wider films. For this silicide line, the width at half height was found to be about 15 nm, slightly wider than the 13 nm width of the underlying silicon line. The thickness of the silicide layer was about 22 nm, which is 5 nm thicker than that of the wider silicide lines or the silicide films. These results clearly indicate an apparent effect of excessive growth of NiSi at the

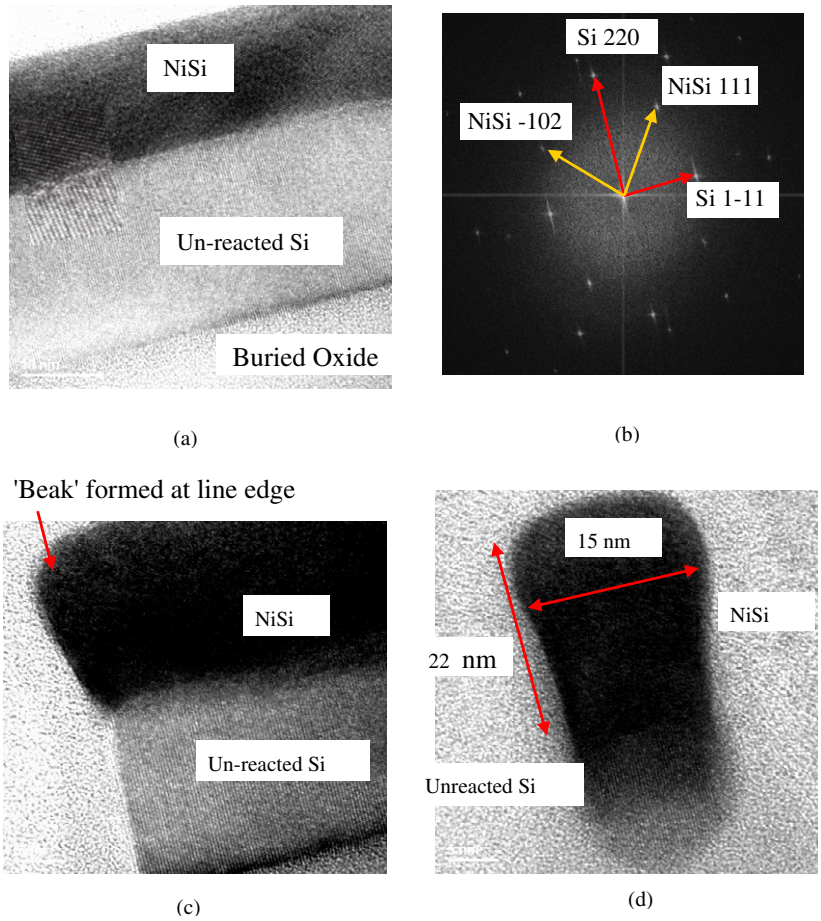


Figure 2. Cross-sectional TEM images of the silicide lines formed on a SOI wafer. (a) TEM image of the interface between silicide and the unreacted silicon at the center of a 500 nm wide silicide line. Inset, HRTEM image shows NiSi/(110) Si interface. (b) Two-dimensional Fourier transform of (a) identifies the silicide layer as orthorhombic NiSi with zone axis [2$\bar{3}$1] parallel to the [$\bar{1}$12] Si zone axis. (c) Cross-sectional TEM image of one side of the wide line, showing the formation of a 'beak' at the line corner, and (d) TEM image of a 15 nm wide silicide line, showing a trapezoidal silicide layer formed on top of the unreacted (110) silicon.

corner of the NL. The local mass flux responsible for shaping the morphology at the line corner is driven by the Gibbs–Thomson chemical potential gradient which depends on the local radius of curvature [18], as well as any stress gradients generated during silicide formation. Since a low stress level was reported for NiSi formation at 400 °C or above [19, 20]; the excessive growth seems to be caused by enhanced diffusion of Ni driven by the chemical potential gradient at the corner of the Si NL. Further investigation is underway to understand this phenomenon because of its importance for silicide FUSI gate technology.

The SEM image in figure 3(a) shows the electrical resistance measurement test structure with integrated contact pads that was fabricated in the NiSi on the (110) SOI wafer. A schematic of the overall four terminal test structure, which was designed to minimize e-beam lithography time, appears in figure 4. As shown, probe pads 1 and 2 are current pads, and probe pads 3 and 4 are voltage pads, and the structure was used to determine the current carrying capability by I–V measurements for a 5.5 μm long silicide line. Here, anisotropic wet etching yielded an inner angle of 70.5° for the probe pad, as defined by two {111} planes. This design enables the formation of a Kelvin test structure simultaneously with the NiSi line structure. It also eliminates separate steps for forming the contact pads as in previous studies using Pt deposition in a FIB system [10] or for additional metal 'lift-off' processes [23]. The NiSi NLs fabricated on the Si NLs were straight, well defined, and much smoother than those obtained by a dry etching process [15]. The quality of the contacts and the NL morphology enabled precise measurements of the line cross-sections in order to determine the resistivity and the current carrying capacity of the NiSi NLs.

Silicide test structures with nominal line widths of 30 and 460 nm were fabricated on [110] SOI wafers with 60 nm thick Si device layers and a 12 nm thick Ni layers. For the fine silicide lines like those shown in figure 3(c), the cross-section consisted of a trapezoidal silicide layer, 31 nm in thickness and 23 nm in width, on top of the unreacted SiNL. In figure 3(d), the HRTEM image of the interface between the silicide and the unreacted Si reveals a crystalline silicide phase with a grain size exceeding the NiSi line width. In comparison, the silicide thickness formed on 455 nm wide Si NLs was found to be 27 nm, which is the same as that formed on a blanket Si substrate with no excessive growth of silicide.

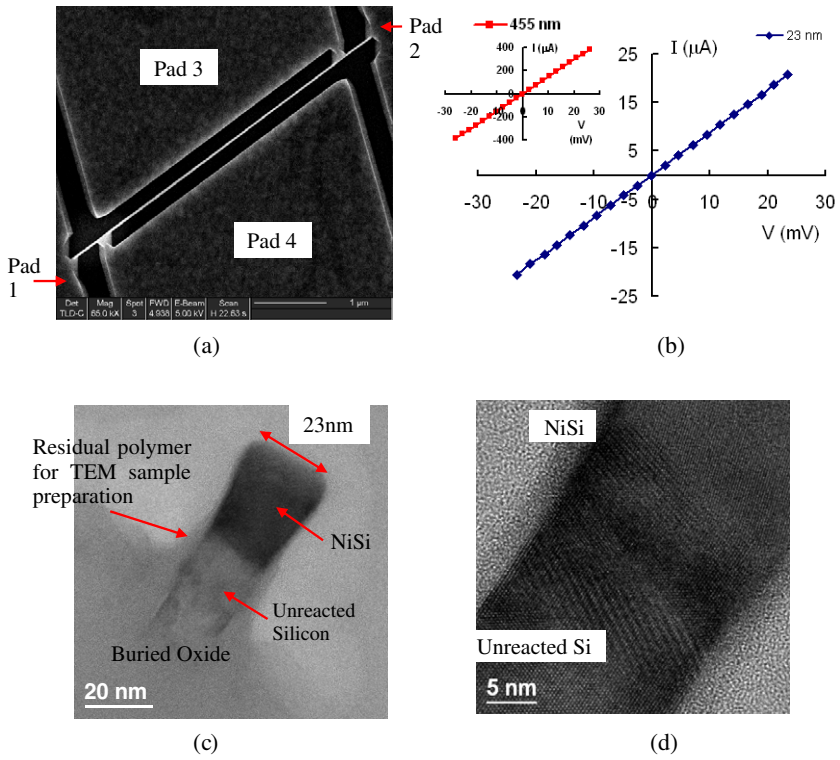


Figure 3. (a) SEM image of the test structure after silicide line formation. The width of the separation trench was 200 nm and the grain size of the polycrystalline NiSi was around 100 nm. (b) Current versus voltage curves from the electrical measurements on the 455 and 23 nm wide NiSi NLs. (c) Cross-sectional TEM image of a NiSi fine test line. Line width and line height were determined to be 23 nm and 31 nm, respectively. (d) HRTEM image of the interface area between silicide and unreacted Si, showing the formation of a crystalline silicide on top of (110) Si and a transition zone. The NiSi grain size is larger than the line width.

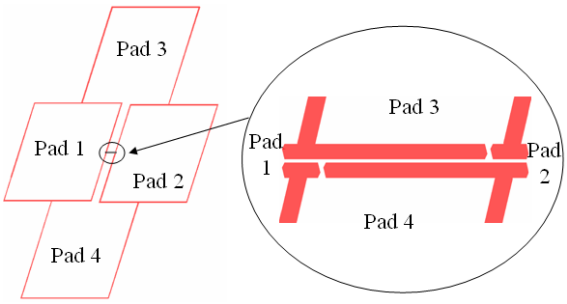


Figure 4. Schematic of the test structure formed by e-beam lithography. Shaded regions correspond to areas where a positive resist was exposed to the e-beam and then removed by the developer. The blank areas are where conductive NiSi formed during the annealing processes. In the measurement, probe pads 1 and 2 were used to force current, and probe pads 3 and 4 were used to provide V/I measurements for line lengths of 5.5 μm.

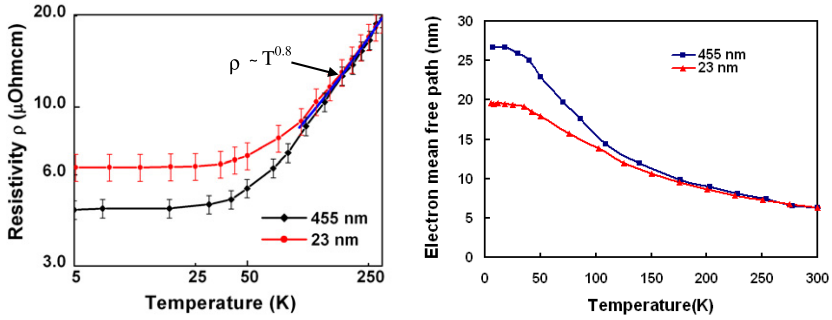
3. Resistivity

The results of room temperature Kelvin resistance measurements are shown in figure 3(b). The room temperature resistances of the NLs, as determined from the slopes of the linear I–V curves, are summarized in table 1. Current leakage through the separation trenches or the intrinsic unreacted silicon layer was measured to be negligible. The I–V curve for the 23 nm wide line remained linear up to a maximum current of 70 μA. This indicates a current carrying capacity exceeding 10^7 A cm^{-2} where the electrical characteristics of the NiSi contact remains linear, meeting the requirements for FUSI gate and contact formation beyond the 22 nm node [9, 24].

Table 1. Room temperature resistances and resistivities for 5.5 μm long NiSi NLs of two different line widths. Errors were estimated to be 6% and 9% of the nominal resistivity values for the 455 nm and 23 nm wide NiSi NLs, respectively, based on uncertainties in the measurement of the cross-sectional area of each NL.

Measured line width (nm)	Measured thickness (nm)	Measured line resistance at 300 K (Ω)	Resistivity at 300 K ($\mu\Omega$ cm)
455	27	66.4	19.7
23	31	1136.0	19.5

In order to further investigate the effect of line width scaling on electron transport, resistance measurements were performed on NiSi lines in a cryostat for temperatures down to 7 K. Results appear in figure 5(a). Above 100 K, the resistivities for both wide and narrow NiSi line structures are very close, and follow a power law dependence of $\approx T^{0.8}$, suggesting that phonon scattering dominates the electron mobility in this temperature range [25]. The effective residual resistivity of the 23 nm line below 30 K (6.3 $\mu\Omega$ cm) was about 26% larger than that of the 455 nm line (4.6 $\mu\Omega$ cm).



(a) (b)

Figure 5. (a) Resistivity of NiSi lines as a function of temperature. (b) Calculated electron mean free path as a function of temperature for the silicide NLs.

4. Discussion

The measured resistivities for both line widths were approximately 20 $\mu\Omega$ cm at room temperature, in good agreement with published results [3, 7, 22] and our own data for polycrystalline NiSi blanket films. However, these resistivities are significantly higher than those reported for NiSi NLs formed on vapor–solid–liquid (VSL) Si NLs [8, 9]. The VSL NLs were reported to have resistivities close to the value of 10 $\mu\Omega$ cm for NiSi single crystals [21]. Higher resistivities must be attributed to (i) the polycrystalline nature of blanket films and NLs, to (ii) electron scattering by the top and bottom surfaces, or to (iii) electron scattering at the sidewalls. It has been reported that the room temperature resistivity of NiSi films is independent of film thickness in the range of 300–70 nm [22]. Our own measurements show no significant thickness dependence for 22–135 nm thick NiSi films. These results suggest that electron scattering at the top and bottom surfaces does not significantly increase room temperature resistivity of the polycrystalline NiSi films. Similarly, the line width independence indicates that sidewall scattering does not reduce the electron mean free path at room temperature. This implies that the room temperature mean free path (λ) for electron scattering in bulk polycrystalline NiSi is significantly smaller than our line widths and film thicknesses, and is consistent with the 5–6 nm room temperature λs previously reported [17, 22].

In general, the contribution from sidewall scattering can be estimated from the Fuchs–Sondheimer (FS) model [26–28] as:

$$\frac{\rho_s}{\rho_0} = \left[1 - \left(\frac{3}{2\kappa}\right)(1-p)\int_1^\infty \left(\frac{1}{t^3} - \frac{1}{t^5}\right)\frac{1-\mathrm{e}^{-\kappa t}}{1-p\mathrm{e}^{-\kappa t}}\,\mathrm{d}t\right]^{-1} \quad (1)$$

where ρ_s is the resistivity of the thin film, ρ_0 is the bulk resistivity, κ is the ratio of the film thickness to the bulk λ, and p is the probability that an electron will undergo specular, as opposed to inelastic and diffuse, reflection from the film surface. The calculated ρ_s/ρ_0 curve is shown in figure 6 for the NiSi film as a function of thickness. For the calculation, λ was assumed to be 5.5 nm as a reasonable compromise between reported values [17, 22] and our own estimates (see below). As the film thickness scales down to 23 nm, the resistivity

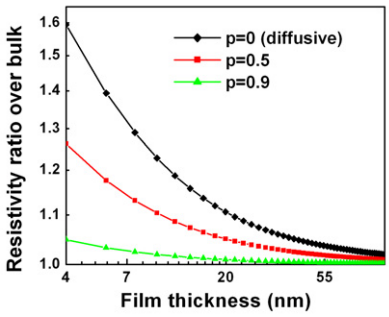


Figure 6. The ratio of film resistance to bulk resistance (ρ_s/ρ_0) as a function of film thickness, as calculated based on the Fuchs–Sondheimer model [26–28]. p is the probability that an electron is specularly reflected from the surfaces. For this calculation, mean free path at room temperature was assumed to be 5.5 nm.

increases by about 9.5% for the case of diffuse electron-surface scattering, i.e. $p = 0$. The resistivity increase would be smaller for larger values of p associated with smoother surfaces. This result suggests that the small λ at room temperature precludes line width effects above 23 nm [29], especially for smooth sidewalls obtained using our fabrication process. Moreover, since the grain size of about 100 nm is much larger than λ, grain boundary scattering is not expected to be dominant.

Matthiessen's rule,

$$\rho = \rho_\mathrm{r} + \rho(T), \quad (2)$$

states that the resistivity, ρ, is the sum of the residual resistivity ρ_r and the temperature-dependent resistivity $\rho(T)$. Here ρ_r includes contributions of scattering from sidewalls, surfaces, grain boundaries, defects, and impurities, and $\rho(T)$ comes from electron–phonon scattering and temperature-dependent electron–impurity scattering. The $T^{0.8}$ dependence above 100 K indicates that phonon scattering dominates the electron mobility in this temperature range [25].

The residual resistivity difference can come from electron scattering by various structural defects or sidewalls. Among the structural defects, the grain boundary scattering can readily be eliminated since the grain sizes in the NiSi lines are about 100 nm, much larger than the thickness and the width of the 23 nm lines. In addition, contributions from more

severe defects, such as cracks, should not be present since the resistivity is essentially the same for the 23 nm and the 455 nm lines above liquid nitrogen temperature. Thermal stress in NiSi NLs at low temperatures could be of concern, because the coefficient of thermal expansion (CTE) of NiSi is highly anisotropic and about 5–15 times larger than that of silicon [30]. However, the larger free surface to volume ratio should be more effective in relaxing the thermal stress in the narrower 23 nm line [30, 31]. Moreover, unlike the effect of strain on carrier mobilities in semiconductors such as silicon, the effects of elastic stress or strain on the resistivity of metals such as NiSi is usually minimal [32]. Hence, we conclude that the residual resistivity difference at low temperatures is mainly caused by additional side wall scattering of electrons, instead of other structural defects or thermal stress, at low temperatures.

In order to test this idea, we deduce λ in the NiSi lines as a function of temperature and calculate the specularity parameter of electron sidewall scattering. For the 455 nm wide NiSi NL, the thickness is only 27 nm, much smaller than its width, and its resistivity ρ shows a plateau at low temperatures. If electron–phonon scattering were to dominate λ at $T < 0.2\Theta_D$, (where $\Theta_D = 430$ K is the Debye temperature of NiSi), the resistivity would be expected to show a T^5 dependence [17]. The low-temperature plateau indicates that the electron–phonon scattering mean free path at cryogenic temperature becomes comparable to, or exceeds, the thickness of 27 nm. Thus surface scattering, which is temperature-independent, limits λ to the line thickness.

Since NiSi is metallic and has a temperature-independent electron concentration (n), the product of ρ and λ is not expected to change with temperature and line width. In other words, $\lambda\rho = [h(3/8\pi)^{1/3}]/[e^2 n^{2/3}]$, where h is the Planck's constant and e is the electron charge, is approximately constant under the conditions of these experiments. Accordingly, with λ at cryogenic temperatures estimated to be about 27 nm for the 455 nm wide line, the values of λ for the 455 and 23 nm NiSi lines can be deduced as a function of temperature as shown in figure 5(b). This yields a λ value of 6.3 nm at room temperature for both the 455 and 23 nm lines, which is in good agreement with the data reported in the literature for polycrystalline NiSi films [17, 22]. In figure 5(b), as the temperature falls below 100 K, λ exceeds 14 nm where the effect of sidewall scattering on electron transport becomes evident for the 23 nm line. Below 20 K, λ for the 455 nm line increases to about 27 nm, comparable to the line thickness, suggesting that the low-temperature electron mean free path could be limited by scattering at the top and bottom surfaces of the 455 nm line. For the 23 nm line below 20 K, λ increases to about 19 nm. This is still smaller than the λ value for the 455 nm line, primarily due to additional scattering at the two sidewalls.

The specularity of electron sidewall scattering can also be calculated, based on the various mean free paths. According to Matthiessen's rule,

$$1/\lambda_{455\ \mathrm{nm}} = 1/\lambda_{\mathrm{electron-phonon}}(T) + 1/\lambda_{\mathrm{defects}} + 1/\lambda_{\mathrm{top-bottom\ surfaces}} \quad (3)$$

$$1/\lambda_{23\ \mathrm{nm}} = 1/\lambda_{\mathrm{electron-phonon}}(T) + 1/\lambda_{\mathrm{defects}} + 1/\lambda_{\mathrm{top-bottom\ surfaces}} + 1/\lambda_{\mathrm{sidewalls}}, \quad (4)$$

where $\lambda_{455\ \mathrm{nm}}$ and $\lambda_{23\ \mathrm{nm}}$ are the mean free path for scattering of electrons in the 455 nm and 23 nm NLs, respectively. $\lambda_{\mathrm{defects}}$ and $\lambda_{\mathrm{sidewalls}}$ are defect scattering and sidewall scattering mean free paths, and $\lambda_{\mathrm{top-bottom\ surfaces}}$ is the mean free path of electron scattering from the top and bottom surfaces of the NiSi layer. Assuming the scattering from defects and top–bottom surfaces to be similar for NLs of any width, the sidewall scattering effect can be estimated by subtracting equation (4) from equation (3) to yield:

$$\lambda_{\mathrm{sidewalls}} \approx \frac{1}{1/\lambda_{23\ \mathrm{nm}} - 1/\lambda_{455\ \mathrm{nm}}} \approx 64\ \mathrm{nm}. \quad (5)$$

Thus the specularity of electrons scattered at the sidewalls is estimated to be

$$p \approx 1 - \lambda_{23\ \mathrm{nm}}/\lambda_{\mathrm{sidewalls}} \approx 0.7. \quad (6)$$

In comparison, the specularity p is close to 0 for the surface scattering in copper interconnects [33]. The difference is in agreement with that the fact that the sidewall surface of the 23 nm NiSi lines formed on anisotropically etched Si NLs is much smoother than that of typical copper interconnects.

5. Conclusions

In summary, single-phase NiSi NLs with straight and smooth sidewalls have been fabricated on (110) SOI wafers down to 15 nm line widths using a top-down process. The process is compatible with the self-aligned silicide (SALICIDE) process in CMOS technology. It can also be applied for hybrid orientation technology that uses mixed orientation silicon surfaces with p-type field-effect transistors (p-FETs) built on (110) silicon and n-FET on (100) to optimize mobility [34]. The effect of scaling on electrical transport in the smooth NiSi NLs was investigated as a function of line width and temperature. Electrical measurements using a test structure fabricated with integrated electrical contacts revealed no significant resistivity differences between the 455 nm and the 23 nm wide lines at room temperature. This indicates that the mean free path λ for electron scattering in NiSi is dominated by electron–phonon scattering at room temperature and is considerably smaller than the 23 nm line width. The residual resistivity at cryogenic temperatures was found to increase with decreasing line width, suggesting a decrease in λ due to sidewall scattering with decreasing line width. Based on resistivity measurements, we deduce λ to be 6.3 nm at room temperature, increasing to more than 14 nm below 100 K. The specularity of electrons scattering at sidewalls was estimated to be about 0.7, indicating much smoother sidewalls than those of typical copper interconnects. The current carrying capacity for the 23 nm NiSi NLs was found to exceed 10^7 A cm^{-2} in the linearly ohmic region.

Acknowledgments

The fabrication and characterization experiments were carried out in the Microelectronic Research Center (MER) and the Center of Nano and Molecular Science and Technology (CNM) at The University of Texas at Austin. This work is supported by the National Institute of Standards and Technology, Office of Microelectronics Programs.

References

[1] Chen L J and Tu K N 1991 *Mater. Sci. Rep.* **6** 53
[2] Mann R W, Clevenger L A, Agnello P D and White F R 1995 *IBM J. Res. Dev.* **39** 403
[3] Iwai H, Ohguro T and Ohmi S 2002 *Microelectron. Eng.* **60** 157
[4] Weber W M *et al* 2006 *Nano Lett.* **6** 2660
[5] Morimoto T *et al* 1995 *IEEE Trans. Electron Devices* **42** 915
[6] Lauwers A *et al* 2004 *Mater. Sci. Eng.* B **114/115** 29
[7] Chen X, Shi Z, Banerjee S K, Zhou J P and Rabenberg L K 2003 *J. Electron. Mater.* **32** 1171
[8] Wu Y, Xiang J, Yang C, Lu W and Lieber C M 2004 *Nature* **430** 61
[9] Kim J and Anderson W A 2006 *Nano Lett.* **6** 1356
[10] Wang Q, Luo Q and Gu C Z 2007 *Nanotechnology* **18** 195304
[11] Zhang Z, Lu J, Hellström P-E, Östling M and Zhang S-L 2006 *Appl. Phys. Lett.* **88** 213103
[12] Ohguro T, Nakamura S, Koike M, Morimoto T, Nishiyama A, Ushiku Y, Yoshitomi T, Ono M, Saito M and Iwai H 1994 *IEEE Trans. Electron Devices* **41** 2305
[13] Kittl J A *et al* 2006 *Microelectron. Eng.* **83** 2117
[14] Cresswell M W, Guthrie W F, Dixson R G, Murabito C E and De Pinillos J V M 2006 *J. Res. Natl Inst. Stand. Technol.* **111** 187
[15] Li B, Kang M K, Lu K, Huang R, Ho P S, Allen R A and Cresswell M W 2008 *Nano Lett.* **8** 92
[16] Lauwers A, Steegen A, de Potter M, Lindsay R, Satta A, Bender H and Maex K 2001 *J. Vac. Sci. Technol.* B **19** 2026
[17] Pomoni K and Krontiras C 1988 *J. Phys. D: Appl. Phys.* **21** 780
[18] Tu K N, Mayer J W and Feldman L C 1992 *Electronic Thin Film Science* (New York: Macmillan)
[19] Cacho F, Cailletaud G, Rivero C, Gergaud P, Thomas O and Jaouen H 2006 *Mater. Sci. Eng.* B **135** 95
[20] Torregiani C, Van Bockstael C, Detavernier C, Lavoie C, Lauwers A, Maex K and Kittl J A 2007 *Microelectron. Eng.* **84** 2533
[21] Meyer B, Gottlieb U, Laborde O, Yang H, Lasjaunia J C, Sulpice A and Madar R 1997 *J. Alloys Compounds* **262/263** 235
[22] Colgan E G, Mäenpää M, Finetti M and Nicolet M-A 1983 *J. Electron. Mater.* **12** 413
[23] Chung S-W, Yu J-Y and Heath J R 2000 *Appl. Phys. Lett.* **76** 2068
[24] International Technology Roadmap for Semiconductors 2007 http://public.itrs.net
[25] Ziman J M 2001 *Electron and Phonons: The Theory of Transport in Solids* (Oxford: Clarendon)
[26] Fuchs K 1938 *Math. Proc. Camb. Phil. Soc.* **34** 100
[27] Sondheimer E H 1952 *Adv. Phys.* **1** 1
[28] Yarimbiyik A E, Schafft H A, Allen R A, Zaghloul M E and Blackburn D L 2006 *Microelectron. Reliab.* **46** 1050
[29] Zhang W, Brongersma S H, Richard O, Brijs B, Palmans R, Froyen L and Maex K 2004 *Microelectron. Eng.* **76** 146
[30] Detavernier C, Lavoie C and d'Heurle F M 2003 *J. Appl. Phys.* **93** 2510
[31] Gan D, Ho P S, Huang R, Leu J, Maiz J and Scherban T 2005 *J. Appl. Phys.* **97** 103531
[32] Morten B, Pirozzi L, Prudenziati M and Taroni A 1979 *J. Phys. D: Appl. Phys.* **12** L51
[33] Zhang W, Brongersma S H, Li Z, Li D, Richard O and Maex K 2007 *J. Appl. Phys.* **101** 063703
[34] Sung C-Y *et al* 2005 *IEDM Technical Digest*