MEASUREMENTS FOR THE RELIABILITY AND ELECTRICAL CHARACTERIZATION OF SEMICONDUCTOR NANOWIRES†

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ABSTRACT

Nanoelectronic devices based upon self-assembled semiconductor nanowires are excellent research tools for investigating the behavior of structures with sub-lithographic features as well as a promising basis for future information processing technologies. We describe two unique approaches to successfully fabricate nanowire devices, one based upon harvesting and positioning nanowires and one based upon the direct growth of nanowires in predefined locations. Test structures are fabricated and electronically characterized to probe the fundamental properties of chemical-vapor-deposition grown silicon nanowires. Important information about current transport and fluctuations in materials and devices can be derived from noise measurements, and low frequency 1/*f* noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices. Both low frequency 1/*f* noise and random telegraph signals are shown here to be powerful methods for probing trapping defects in nanoelectronic devices

[*Keywords:* nanoelectronics, semiconductor nanowires, 1/*f* noise, test structures]

INTRODUCTION

There is growing interest in the development of novel nanoelectronic devices to enable either enhanced performance or new functionality. Semiconductor nanowires have emerged as powerful building blocks for the assembly of nanoscale devices by the bottom-up paradigm (see for example reference [1]). Such "bottom-up" nanowire devices hold the promise to overcome some of the fabrication challenges associated with making devices with sub-30 nm feature sizes. Liquid-vapor-phase growth catalyzed by metal nanoparticles can control the nucleation and subsequent growth of semiconductor nanowires. [2-4] By using this process, nanowires can be readily grown with diameters ranging from the sub-lithographic (as small as 3 nm [5]) to 100's of nanometers and lengths that are tens of micrometers long. In addition to single-crystal structures with a homogeneous composition, axial heterostructures and radial heterostructures can be grown. [1] Furthermore, since they are grown directly from catalyst, nanowires can be grown with smooth (nominally atomically smooth) sidewalls. Thus, there are none of the artifacts and processing difficulties associated with line-edge roughness that would be associated with wires formed by using conventional lithography and etching techniques.

While it is relatively straight-forward to grow small diameter nanowires, it is a challenge to reliably contact the nanowires to form test structures and demonstrate prototypical devices. We present two fabrication approaches that can be used to form semiconductor nanowire devices: one based upon harvesting and positioning nanowires [6] and one based upon the direct growth of nanowires in predefined locations. [7] These approaches can be applied generically to nanowires of nominally any material, and they do not rely on deep sub-μm electron beam or projection lithography. Because of the pervasive nature of silicon in today's integrated circuit technology, we demonstrate these fabrication methods by fabricating nanoelectronic test structures for silicon nanowires (SiNWs).

Because of the large surface-to-volume ratio of nanowire field effect transistors (FETs) and subsequently enhanced scattering from surface states, the low frequency current noise fluctuations can be pronounced in such devices. Therefore, a thorough understanding of the noise properties is critical to reduce the noise and fluctuations in nanowire devices and for the eventual design and integration of semiconducting nanowire functional units in nanoelectronics. Noise contains important information about current transport and fluctuations in materials and devices, and low frequency 1/*f* noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices. [8-11] Because noise is more sensitive to traps and defects as the size of devices is reduced, the use of noise as a defect characterization method has become more popular in recent years due to device scaling (unlike capacitance-voltage and charge pumping measurement methods which become less accurate as the device size decreases and require a substrate contact). The noise properties of individual SiNW FETs (formed by using directed assembly) were measured and are reported here. The Hooge's parameter is determined from the gate dependence of the noise amplitude. A direct correlation between 1/f noise and interface state density is observed by characterizing devices before and after annealing to passivate many of the scattering sites.

Discrete switching events in the drain current measured as a function of time or random telegraph signals (RTSs) arise from the fluctuating occupancy of individual electron traps near the conduction channel of nanowire FETs. [12] The study of RTS can provide a novel technique to probe a single trap and allows one to understand the fundamental physics behind the carrier transport and current fluctuations in nano-scale devices. [9,14-18] In this work, two- and three-level RTSs are observed at low-temperatures in n-type ZnO nanowire FETs. The physical nature of the traps responsible for this switching is analyzed.

SINGLE NANOWIRE MANIPULATION SYSTEM

We have developed a single nanowire manipulation system (SNMS) to precisely maneuver and align individual nanowires to form prototypical nanowire devices and test structures. [6] With this SNMS individual nanowires can be picked up and transferred to a predefined location by electrostatic force. Compatible fabrication processes have been developed to simultaneously pattern multiple aligned nanowires by using one level of photolithography. After growth, the SiNWs are harvested into a suspension of DI water by

sonication (1 min) (Figure 1(b)). The SiNW solution is dispersed onto a template substrate and dried for 4 h under vacuum at 100 mTorr (Figure 1(c)). As shown schematically in Figures 1 (c) and (d), the SNMS is then used to pick up selected nanowires and transfer them to predefined locations on a photolithographically patterned device substrate. The nanowires were further precisely aligned to the device substrate as needed. Finally, top metal contacts were patterned via conventional photolithography (Figure 1 (e)) to complete the nanowire devices and test structures.

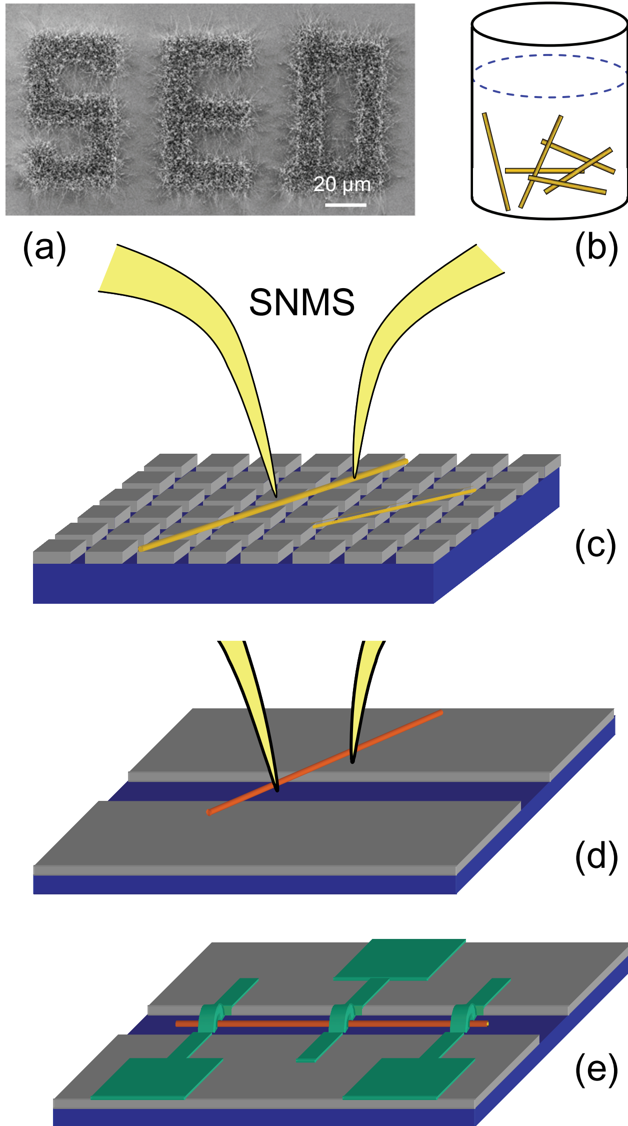

Figure 1: Single Nanowire Manipulation System (SNMS) fabrication approach: (a) SEM image of Si nanowires grown from patterned Au catalyst on a silicon wafer. (b) Nanowires removed into a suspension of DI water. A drop of the nanowire solution was dispersed on a template substrate and evaporated under a vacuum of 100 mtorr for 4 h. (c) Schematic of manipulator tips picking up a nanowire from a template substrate. (d) Placing a single nanowire on a substrate containing an alignment trench. (e) Device after formation of metal contacts.

The SiNWs used in this study (Figure 1a) were prepared by using low-pressure chemical vapor deposition (LPCVD) under 500 mTorr SiH_4, at 450 ^oC, with thin Au films (~ 2 nm) as the catalyst via a vapor-liquid-solid mechanism. Nanowires of 20 nm to 300 nm in diameter and 2 µm to 150 µm in length were obtained for this approach. An example of SiNWs on a patterned catalyst substrate is shown in Figure 1(a). From transmission electron microscopy (TEM) characterization (data not shown), the SiNWs have a hexagonal cross-section and grow along the expected [111] direction [4] with a spacing between the (111) planes, which are oriented perpendicular to the SiNW growth direction ≈ 0.31 nm as determined from TEM images.

The SNMS is an excellent approach for fabricating test structures to probe the fundamental properties of semiconductor nanowires. For example, it can be used to fabricate Kelvin test structures and transfer length method (TLM) structures which rely on multiple contacts to a single nanowire to separate the contact resistance from the nanowire resistance.

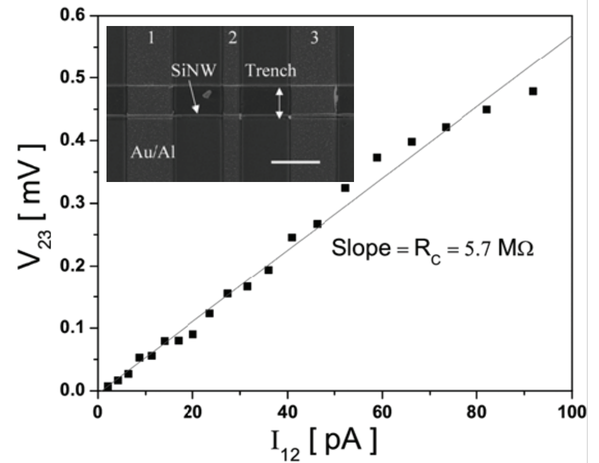

Figure 2: Kelvin test structure to extract metal/nanowire contact resistance. Insert: SEM image of Kelvin test structure (Scale bar: 5 µm). This structure, fabricated by using the SNMS, has three electrodes 1, 2 and 3. Plot of voltage across metal/SiNW contact (V_{23}) as a function of current through electrode 1 and 2 (I_{12}). The slope is the contact resistance (≈5.7 MΩ) of the SiNW (78 nm in diameter).

The Kelvin test structure is a conventional semiconductor characterization technique widely used to measure contact resistance. [19] As shown in the insert to Figure 2, a nanowire-based Kelvin test structure was fabricated by using the SNMS. This three-contact structure was annealed in nitrogen at 420 ^oC for 60 s to improve the Al/Si contacts. With current, I_{12}, flowing from contact 1 to contact 2, the contact resistance, R_C, is

$$R_C = \frac{V_{23}}{I_{12}} \quad , \qquad \text{Eq. 1}$$

where V_{23} is the voltage drop measured between contact 2 and contact 3. The plot of I_{12} as a function of V_{23} is shown in Figure 2. The contact resistance (≈ 5.7 MΩ) is determined from the slope of the plot by using a linear least square fit (LLSF).

The TLM test structure has been widely used as a precise technique for extracting contact and sheet resistance. [19] As shown in the insert to Figure 3, a nanowire-based TLM test structure with a SiNW and Al contacts was fabricated by using the SNMS followed by annealing with N at 420 ^oC for 60 s to improve the Al/Si contact. For the TLM test structure, the total resistance (R_T) of any two contacts is

$$R_T = 2R_C + p_\ell L \, , \qquad \text{Eq. 2}$$

where R_C is the contact resistance, ρ_ℓ is the resistance per unit length of this relatively large SiNW (165 nm in diameter), and L the contact spacing. The plot of total resistance, R_T, as a function of contact spacing is shown in Figure 3 for a range of current levels. From a LLSF, for this particular SiNW, the intercept 2 R_C ranges from 4.5 MΩ to 5.1 MΩ, and the slope of each curve is ρ_ℓ for currents of 0.8 nA to 1.4 nA (ρ_ℓ is fully listed in Figure 3).

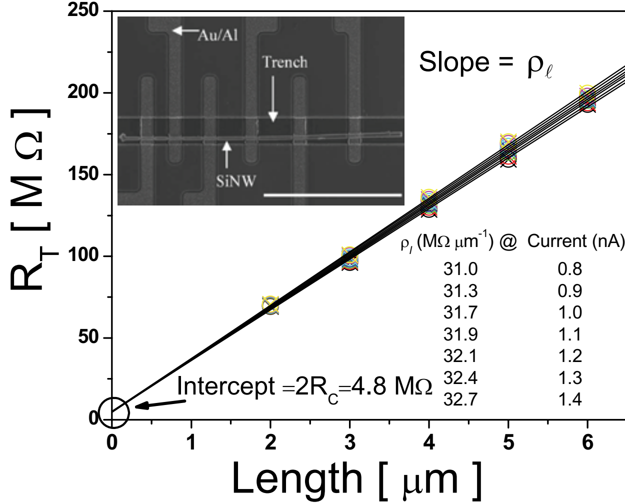

Figure 3: insert: SEM image of a transfer length method test structure for characterization of metal/SiNW contact resistance fabricated by using the SNMS. (Scale bar: 20 μm) Plot of total resistance (R_T) as a function of contact spacing, length: 2 μm to 6 μm. The total resistance of seven curves was obtained under currents of 0.8 nA to 1.4 nA. Intercept is $2R_C$, where R_C is the contact resistance (R_C is 2.5 MΩ on average). Slopes of each curve are the resistance of the SiNW (150 nm in diameter) per micrometer, ρ_ℓ, under different currents: 0.8 nA to 1.4 nA.

In addition to fabricating field effect transistors and electronic test structures, the SNMS fabrication approach has been shown to be effective for fabricating nanowire electromechanical (NEM) switches which are very attractive for logic device applications. [20] These NEM devices, consisting of CVD grown silicon nanowires suspended over metal electrodes, are operated by bending the suspended part of the nanowire to touch a metal electrode via electromechanical force created by applying voltage. They can also be used to extract material properties such as Young's Modulus which can be challenging to determine in nm-sized device components.

Directed Self Assembly

While most research on self-assembled nanowire devices involves forming a nanowire solution by harvesting nanowires from the preparation substrate and suspending them in liquid, these approaches are likely to introduce contaminants on the surface of the nanowires. Such a contaminated surface could increase the device interface states (D_{it}) and seriously deteriorate the device performance. Growing semiconductor nanowires in place from pre-defined catalyst locations is an approach that enables both the simultaneous, batch fabrication of large numbers of nanowire devices, and can reduce the processing steps that may contaminate the nanowire surfaces.

To illustrate this self-aligned nanowire growth approach, we have fabricated SiNW FETs with HfO_2 as the gate dielectric. In this directed assembly approach, [7] devices are fabricated from SiNWs that are grown in place from Au catalyst (~ 1 nm thick) patterned in pre-defined locations on 50 nm thermal SiO_2. In the simplest structures, the p-type silicon substrate can be used as a bottom gate electrode. The SiNWs were grown in a low temperature chemical vapor deposition furnace, at 420 °C, under 500 mTorr SiH_4 via a vapor-liquid-solid mechanism. Under these conditions SiNWs are nominally 20 nm in diameter and regularly ≈20 μm to 30 μm in length. The SiNWs are thermally oxidized at 700 °C for 30 min to grow a thin oxide that will be the basis of the dielectric interfacial layer.

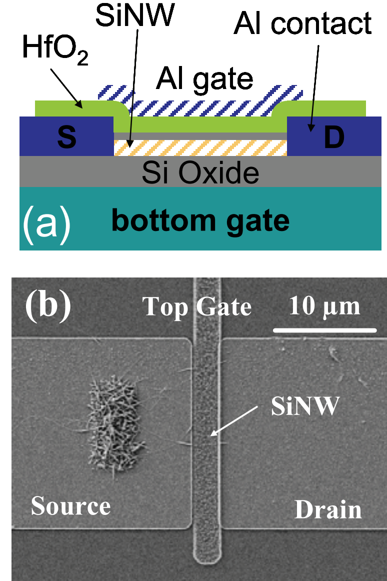

Figure 4: SiNW FET formed by directed self-assembly: (a) schematic drawing of device cross-section along the length of the SiNW; (b) SEM of a typical top-gated, SiNW FET with no gate to source/drain overlap. Note the patterned catalyst region in the source from which the SiNWs were grown.

After oxide growth and before HfO_2 deposition, Ni source/drain contacts were formed by thermal evaporation and metal lift-off. A layer of HfO_2 was then deposited as the top gate dielectric of the SiNW FET by atomic layer deposition at 250 °C. The top gate electrode (Al) is formed by using lift-off processes similar to those used in forming the source and drain electrodes. A schematic of the resulting devices is shown in Figure 4 (a) along with a scanning electron micrograph of a top-gated FET device in Figure 4 (b). The transfer curves for a typical, top-gated SiNW FET (with a nominal diameter of 20 nm and a nominal length of 6 μm) formed by directed self-assembly are shown in Figure 5 (a) to illustrate the effectiveness of this fabrication approach. Data are obtained for a device both before and after a forming-gas rapid-thermal anneal for 300 s at 300 °C. The increase in the saturation current (Figure 5 (a)) and the dramatic decrease in the subthreshold slope (Figure 5(b)) after annealing indicate the importance of this final processing step. A large number of interface defects are passivated by the forming-gas anneal.

This directed self-assembly fabrication approach has been shown to be effective for fabricating a range of devices in addition to the simple FETs illustrated here. SiNWs have been grown *in situ* on oxide/nitride/oxide for memory applications [7] and Si NW FETs with a HfO_2 gate dielectric fabricated by using this technology have exhibited excellent electrical performance with large I_{on}/I_{off} ratios ~10^6 and sharp subthreshold slopes, S ~ 85 mV/dec. [21]

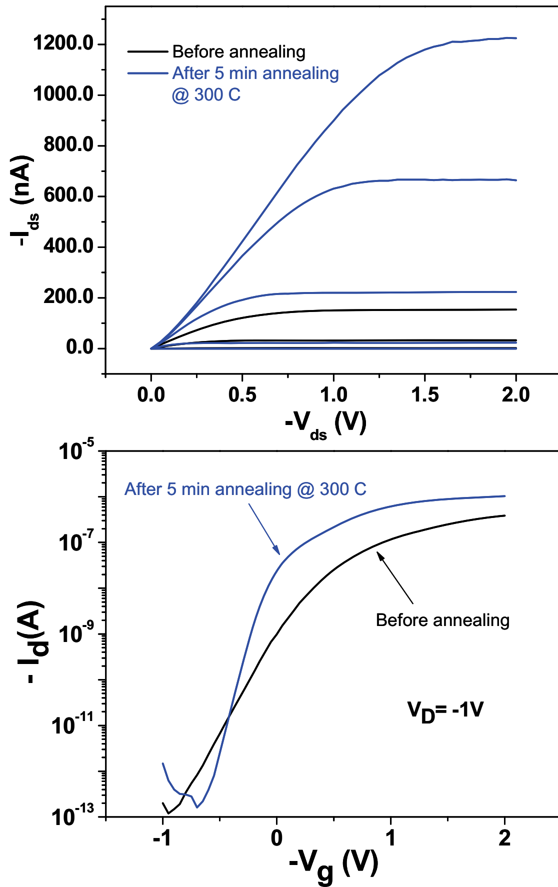

Figure 5: Electrical characterization of a typical, top-gated SiNW FET (with a nominal diameter of 20 nm and a nominal length of 6 μm) formed by directed self-assembly before annealing and after forming gas rapid thermal annealing for 300 s at 300 °C. (a) I_{DS}-V_{DS} curves at V_g = +0.5 V to -1.5 V in -0.5 V steps. I_{ds} and V_{ds} are negative and shown in the positive quadrant for convenience sake. (b) I_{ds} as a function of V_g for V_{ds} = -1V.

Noise Measurements

A thorough understanding of the noise properties of emerging nanoelectronic devices such as those based on semiconductor nanowires is critical because the signal-to-noise ratio is a fundamental factor limiting their performance. Noise measurements also can give great insights into defects and scattering mechanisms in nanowire devices. Because semiconductor nanowire devices have a very small total area (by definition), the capacitance associated with such devices is extremely difficult to measure accurately. This capacitance measurement challenge makes it impossible to use traditional capacitance-voltage/conductance-voltage techniques [19,22-26] to determine the interface trap capacitance and subsequently information about the properties of the interface traps themselves. In addition, semiconductor nanowire devices have no body contact; therefore, charge-pumping techniques [19,24,27] cannot be used to investigate charge trapping centers. However, the trapping and detrapping of charge carriers from the nanowire conduction channel lead to low-frequency noise. [12,28,29] Under some conditions (such as at low-temperatures or in extremely small nanowire devices) the trapping and emission of carriers by discrete interface or border traps leads to experimentally observed RTS's. Thus, noise measurements are the most experimentally accessible method to probe trap-induced scattering in semiconductor nanowire devices.

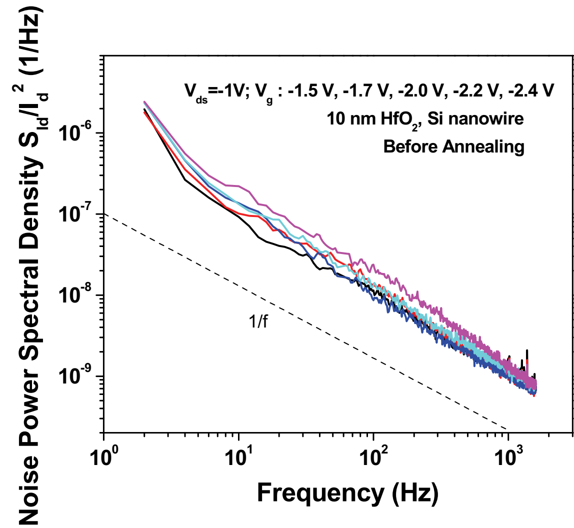

Figure 6: Typical normalized drain current noise spectra for a SiNW device fabricated by using directed self-assembly. V_{ds}= -1 V and the gate bias varies from -1.5 V to -2.4 V. The frequency range is from 1 Hz to 1.6 kHz. (Note: data are from same device as in Figure 5).

Typical normalized drain current noise spectra, S_{Ids}/I_{ds}^2, for a SiNW device fabricated by using directed self-assembly are plotted in Figure 6 with the device biased at V_{ds}= -1 V and the gate bias varying from -1.5 V to -2.4 V. The frequency range is from 1 Hz to 1.6 kHz. For consistency sake, this is the same device from which the results in Figure 5 are obtained. The low frequency noise spectra are predominantly $1/f^{\alpha}$, with the frequency exponent α close to 1.

According to Hooge's empirical law, the 1/*f* noise amplitude can be expressed as [30]

$$A = \frac{\alpha_H}{N}, \qquad \text{Eq. 3}$$

where α_H is the Hooge's constant and N is the total carrier number in the system. This relationship was introduced to describe the 1/*f* noise in homogenous bulk materials, and α_H can be used to compare 1/*f* noise in different systems regardless of the specific device parameters and measurement conditions. [30,31] For bulk materials α_H is typically on the order of 10^{-3}. By using Eq. 3 and the expression of the gate capacitance, the inverse of A can be expressed as [28,32]

$$\frac{1}{A} = \frac{C_g L}{e\alpha_H} | V_g - V_{th} |. \qquad \text{Eq. 4}$$

Thus α_H can be determined from the relationship 1/A versus (V_g – V_{th}) which can be calculated from the gate dependence of the noise amplitude (Figure 6)). For these ≈20 nm SiNWs with a top-gate and an interface oxide/HfO_2 dielectric, α_H is estimated to be 1.5 × 10^{-2} (after annealing). Figure 7 shows the Hooge's constant of these unoptimized SiNW FETs, compared with previously published data of poly-silicon gate/HfO_2 [33] metal gate/HfO_2, [34] single-wall nanotube FET devices, [32,35] and ZnO nanowires. [28] The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node. [36,37] As can be seen from Figure 7, the Hooge's constant of our SiNW devices is similar to, but slightly higher than, values reported recently for these other emerging FET technologies. Due to the high surface-to-volume ratio of nanowires it is not unexpected that noise may be larger in such devices compared with similar structures based on bulk substrates. In addition, it is anticipated that by optimizing the processing – particularly for the

Si/dielectric interface formation and ALD HfO_2 deposition – the noise level of these research-grade devices will be greatly reduced.

As shown in Figure 5, a forming gas anneal (300 s at 300 °C) greatly improves the performance of the SiNW FETs. Figure 8 shows that a decrease in the normalized drain current noise power spectrum density is also observed after annealing. From the dramatic change in the slope of the $I_{ds} – V_g$ subthreshold curves (Figure 5b), it can be seen that a substantial number of interface traps were passivated during the anneal. [38] This decrease in trap density is directly observable as a reduction in the noise power spectrum.

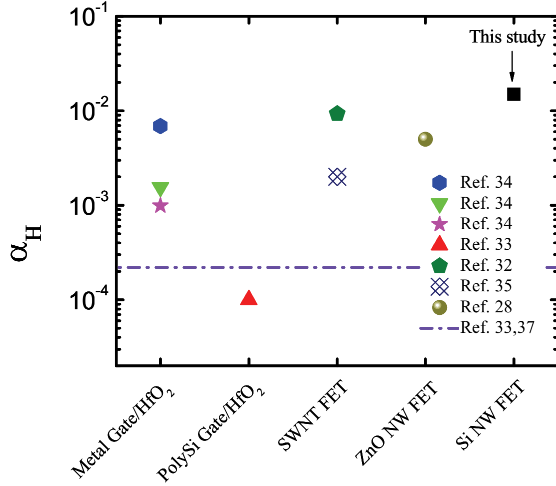

Figure 7: Summary plot of the Hooge's constant obtained in this study (black square) with previously published data for poly-silicon gate/HfO_2, metal gate/HfO_2, single-wall nanotube FET, and ZnO nanowire FET devices. Different values of the same type of device are from different reports. The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node.

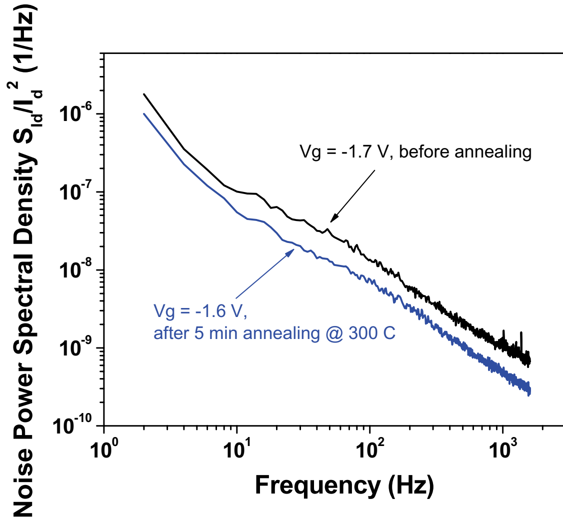

Figure 8: Normalized drain current noise spectra for a SiNW device before (black) and after (blue) a 300 s forming gas anneal at 300 °C. V_{ds}= -1 V.

As just shown, at room temperature, the noise power spectra of nanowire FETs typically have a classic 1/*f* dependence. When the temperature is lowered to 4.2 K, the low frequency noise often changes from 1/ f to a Lorentzian spectrum, and the current traces as a function of time show RTSs. [12] We illustrate that here for single nanowire FETs fabricated from ZnO nanowires that were synthesized by thermally vaporizing a mixed source of commercially available ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1:1 in a tube furnace.[28] In these ZnO nanowire FETs, the low frequency noise in the same device changes from 1/*f* to a Lorentzian spectrum when the temperature is lowered to 4.2 K. [12] Figure 9 (a) shows the a typical Lorentzian noise spectrum of a ZnO nanowire FET biased at V_{ds}=2 V and V_g=8 V at 4.2 K. Such a Lorentzian spectrum is caused by the trapping and detrapping of a single defect in the dielectric around the nanowire and can be described by

$$\frac{S_{I_{ds}}}{I_{ds}^{\;2}} = \frac{K}{\left(1 + f / f_c\right)^2} \quad \text{Eq. 5}$$

where K is a constant independent of frequency and f_c is the corner frequency of the Lorentzian. The signature of this single trap state is also shown in the RTS of the top drain current time trace (for V_{ds}=2 V and V_g=8 V) of Fig. 9 (b), where the channel current switches between two discrete values. The change of temperature to 4.2 K primarily decreases the number of defects in the dielectric accessible to the carriers in the wire and responsible for the fluctuations to a few single traps due to the shrinking of the activated energy window ($\approx 4k_BT$, where k_B is the Boltzmann constant) in the dielectric band gap. In addition, there is a three orders of magnitude decrease of current at 4.2 K compared to room temperature. As a result, the trapping/detrapping of carriers from the traps causes more dramatic fluctuations of the channel current. The corner frequency f_c can be estimated to be ≈18 Hz by locating the peak in the $S_{Ids}{\cdot}f$ vs f plot (not shown). This frequency is consistent with the calculation from mean time at high current τ_{on} and low current τ_{off} obtained from the data in the current time trace in Figure 9 (b), where f_c=1/2$\pi\tau_0$ and $1/\tau_0=1/\tau_{on}+1/\tau_{off}$.

Figure 9 (b), shows drain current traces recorded at V_{ds}=2 V for 300 s as a function of gate bias. There is a great deal of information in these time dependent current traces, and such data can be quantitatively analyzed by estimating a hidden Markov model based on a Gaussian mixture, and quantified by using a Viterbi decoder to measure the discrete current switching events. Such an analysis enables the estimation of parameters such as event lifetime, event amplitudes, and trap cross-section.

Qualitatively, two discrete levels (such as seen in the V_g=8 V trace), indicates that there is only one near interface oxide (border) trap, A, interacting with the carriers through tunneling. At this bias condition, only one trap in the dielectric resides in the band gap within $\approx 2k_BT$ of the channel Fermi level and is within a favorable distance from the channel to be able to be electrically active in the reversible capture and emission processes with the channel carriers. The low current level corresponds to the state that one electron is captured by trap A while the high current level corresponds to the empty state. As the gate bias increases, the trap occupancy increases. When Vg is increased to 9 V, negative peaks appear and the current trace shows three levels, (which is confirmed by three distinctive peaks in the corresponding histogram – not shown). It has been argued that such three-level switching could be due to multiple electron trapping at one defect site, [9] an unlikely situation due to the repulsive force between an electron and a negatively charged trapping center. We propose a more likely scenario in which there is a second border trap, [39] B, with a slightly higher energy than trap A, located within ≈2kBT of the Fermi level in the ZnO nanowire when the bias on the gate is increased, which causes more band bending. In this description, the high current value corresponds to the state where both traps are unoccupied, the middle current level is observed when trap A is charged while trap B is empty, and the low current level likely corresponds to the state where both traps are

filled. The band structure of the measured device with two traps is illustrated in the insert to Figure 9 (a). As the gate voltage increases to 13 V, only trap B aligns with the Fermi level so that simple two level RTS is again observed. Trap B gives a larger RTS amplitude compared to trap A, presumably due to a closer proximity to the channel.

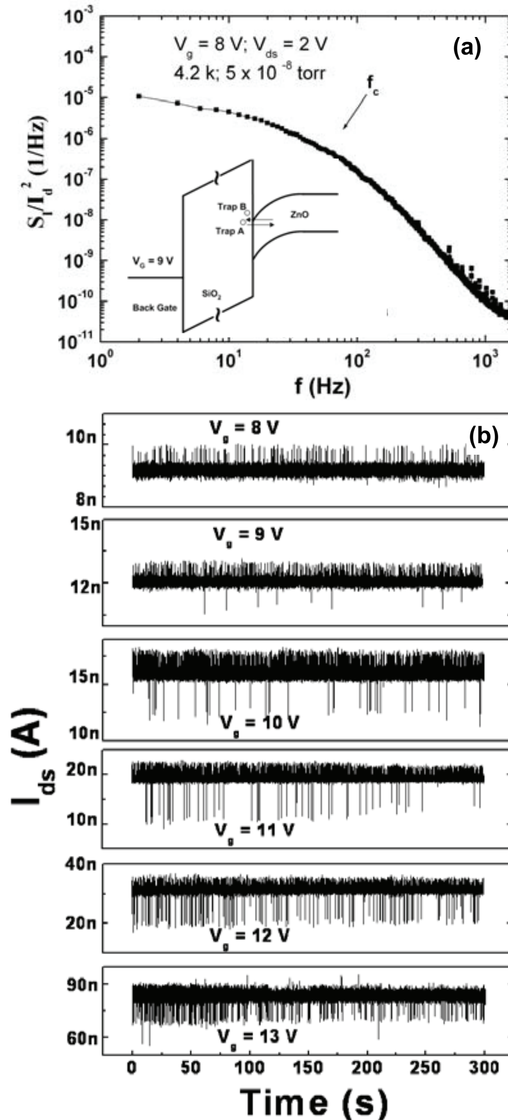

Figure 9: (a) Typical Lorentzian spectrum with corner frequency at ~ 18 Hz when the device is biased at V_g = 8 V and V_{ds} = 2 V; insert: band diagram for back gate voltage at 9 V with two near interface oxide (border) traps; (b) the time domain random telegraph signals. Raw drain current for a time interval of 300 s observed in the ZnO nanowire FET at 4.2 K as a function of gate bias. The drain bias is kept constant at 2 V.

CONCLUSION

While bottom-up semiconductor nanowire devices are a promising nanoelectronic technology of the future, they are already an important research tool today. We have shown here two methods for fabricating nanoelectronic devices based on nanowires. Because these simple fabrication approaches do not rely on extremely expensive processing and lithography equipment they should enable a large range of scientists to use them to advance nanowire research and technology. We have used noise measurements, an under utilized experimental approach, to characterize the low-frequency, 1/*f*, noise and RTS properties of nanowire FETs. The examples described here illustrate that noise measurements are the most experimentally accessible method for probing trapping defects in nanoelectronic devices.

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