

STRESS-INDUCED DEFECT GENERATION IN HfO₂/SiO₂ STACKS OBSERVED BY USING CHARGE PUMPING AND LOW FREQUENCY NOISE MEASUREMENTS

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ABSTRACT

The technique of combining the low frequency drain current noise and the frequency-dependent charge pumping techniques has been employed to extract the trap densities in both the interfacial SiO₂ layer and high-k layer in the n-type MOSFETs with HfO₂/SiO₂ stacks. It is found that positive bias stress creates more traps in the gate dielectric stack near the gate electrode while negative stress increases the density of traps generated in the proximity of the Si substrate. The results show that under electrical stress new traps are predominantly created close to the anode side and the degree of asymmetry is surprisingly large.

[Keywords: Charge pumping, 1/f noise, oxide trap, defect generation, HfO₂]

INTRODUCTION

Hafnium-based dielectrics are prime candidates for the replacement of SiO₂ in the next generation CMOS technology. However, these materials exhibit a much higher defect density when compared to SiO₂, aggravating some major device reliability issues including the bias temperature instability, the reduction in mobility, and possibly the time dependent dielectric breakdown. The knowledge of the trap location and density can improve the understanding of their effects on device reliability. The combination of low frequency (LF) noise and charge pumping (CP) measurements performed on the same set of samples is well suited to obtain this information, with LF noise sampling traps located further away from the interface [1] while CP current sampling traps closer to the interface [2].

Furthermore, the mechanism of device degradation under constant voltage (positive or negative) stress is still under debate due to the lack of techniques to separate the traps in the interfacial and the high-k layer. Monitoring both the LF noise and the charge pumping current during the interruption of a constant voltage stress (CVS) allows an extended spatial profiling of traps created during the stress, enabling the study of the defect generation mechanism in both the high-k dielectric layers and interfacial layers (IL).

In this paper, we use the charge pumping and the low frequency noise signals to monitor the trap densities in the interfacial SiO₂ and the HfO₂ layers, and compare the creation of new traps in both layers during the positive and negative stress.

SAMPLES

Fully processed nMOSFETs with HfO₂/SiO₂ (3 nm/1 nm physical thicknesses) gate dielectrics fabricated on 200 mm p/p+ epitaxial Si <100> wafers using a standard CMOS process with 1000 °C/10-sec dopant activation anneal were used in this work.

ELECTRICAL CHARACTERIZATION

Carrier exchange (trapping and detrapping) via tunneling between the inversion layer and the trap sites causes LF noise [3]-[5]. Each tunneling depth corresponds to a specific time constant for the charge exchange process, and is given by

$$\tau = \tau_0 \exp(-\alpha_t x) \quad (1)$$

where τ_0 is the time constant at the interface typically taken to equal 10⁻¹⁰ s [6], and x is the distance into the oxide from the Si-SiO₂ interface. Depending on the thickness of the IL, the trap sites responsible for the LF noise can be within the IL only, within the HfO₂ only, or both. The tunneling parameter α_t is governed by the effective mass of the electron in the dielectric, m_e^* , and the barrier height from the Si conduction band edge to the dielectric conduction band edge, ϕ_B , with

$$\alpha_t = \sqrt{\frac{2m_e^*\phi_B}{\hbar^2}} \quad (2)$$

where \hbar is the Plank's constant divided by 2π . As a result, lower frequencies correspond to larger tunneling depths or further away from the Si/IL interface. The well-established number fluctuation model can be used to calculate the volume trap density in the high-k layer by using the following formula [7]

$$N_t = \frac{S_{ld}\alpha_t C_{EOT}^2 WL^2}{g_m^2 q^2 kT} \quad (3)$$

where kT is the thermal energy, q is the elementary charge, C_{EOT} is the capacitance associated with equivalent oxide thickness, W is the channel width, L is the channel length, f is the frequency, S_{ld} is the spectral density of the current noise, and g_m is the transconductance.

LF noise measurements were performed using a low frequency noise measurement setup shown in Fig. 1 (a), which includes two low noise DC biasing sources, a low noise voltage pre-amplifier, and a dynamic signal analyzer. The drain voltage-noise power spectral density was measured at the drain bias of 50 mV.

The CP technique is a very efficient tool for studying the interface traps in high-k gate MOSFETs. Recently, the frequency dependent CP technique has been used to determine the depth profile of traps in the high-k gate dielectric stacks [8]-[14]. Fig. 1 (b) shows the schematics of the CP measurement. A square wave applying to the gate switches the transistors between inversion and accumulation. The hold time in accumulation and inversion (roughly half a period of the square wave) determines the depth at which traps can contribute to the charge pumping current. Trap profiles are extracted from the CP data using (4) [2]

$$N_{ot}(x_m) = -\frac{1}{q\lambda_n A\Delta E_t} \frac{dQ_{cp}}{d\ln(f)} \quad (4)$$

where A is the gate area, Q_{cp} the charge pumped per cycle, f the measurement frequency, and λ_n the attenuation coefficient.

The combined qualitative trap density profile is plotted in Fig. 1 (c). A continually increasing trap density as a function of distance from the substrate is extracted (from CP current) in the SiO_2 layer. In the HfO_2 layer, a relatively flat trap density is extracted (from noise) except in the vicinity of metal gate region [8]. The LF noise measurement frequency range is 1 Hz to 1.6 kHz, limited by instrument. The CP measurement frequency range is 10 kHz to 5 MHz. Lower frequencies are possible but the gate leakage current may become a source of error.

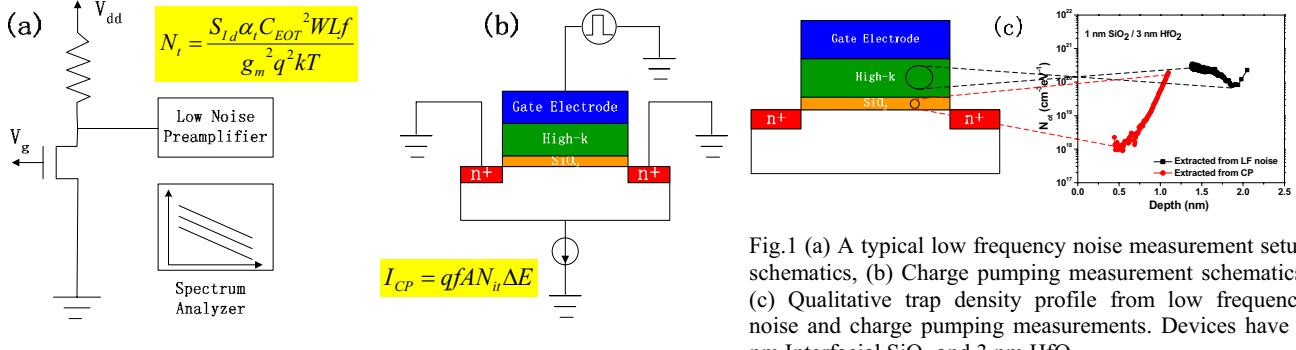


Fig.1 (a) A typical low frequency noise measurement setup schematics, (b) Charge pumping measurement schematics, (c) Qualitative trap density profile from low frequency noise and charge pumping measurements. Devices have 1 nm Interfacial SiO_2 and 3 nm HfO_2 .

Fast I_d - V_g with the setup described in [15] was also performed along with the CP, and LF noise measurements at the end of each stress period. After each stressing step, a negative 1 V was applied on the gate for 30 s to empty the “fast” component so only permanent non-recoverable defects remain. The gate pulse had a rise time of $t_{rise} = 5 \mu\text{s}$.

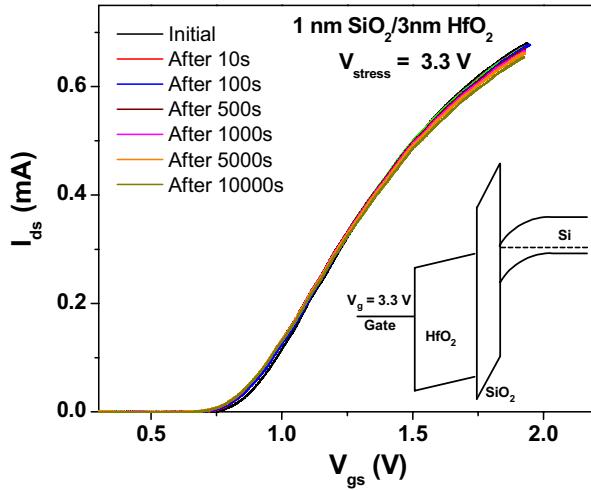


Fig.2 Change of the I_d - V_g characteristic during positive bias stress. After each stress step, a negative 1 V was applied on the gate for 30 s to discharge. The inset shows the band diagram of a nMOSFET high-k gate stack under 3.3 V gate bias.

Figs. 2-6 show the resulting device degradations under positive constant voltage stress. In order to measure the trap density during stress, the constant voltage stress is interrupted at a regular time interval to perform both the LF noise and the charge pumping measurements after a 30 seconds discharge period. In Fig. 2, the fast I_d - V_g curves are plotted before and after different periods of stress. The threshold voltages shift to the left while the currents at high V_g

drop due to mobility degradation. The 1 MHz variable base-level charge pumping results are plotted in Fig. 3, showing the trap density evolution as a function of stress time. It suggests that traps are generated at and/or very near the Si/SiO_2 interface. The trap density at the peak position is almost doubled, increasing from $1.9 \times 10^{10} \text{ cm}^{-2}$ to $4.3 \times 10^{10} \text{ cm}^{-2}$. The frequency dependent charge pumping data between 10 kHz and 5 MHz are plotted in Fig. 4, showing the evolution of the trap density in the IL at different stress time. A monotonic increase in trap density of all frequencies is detected.

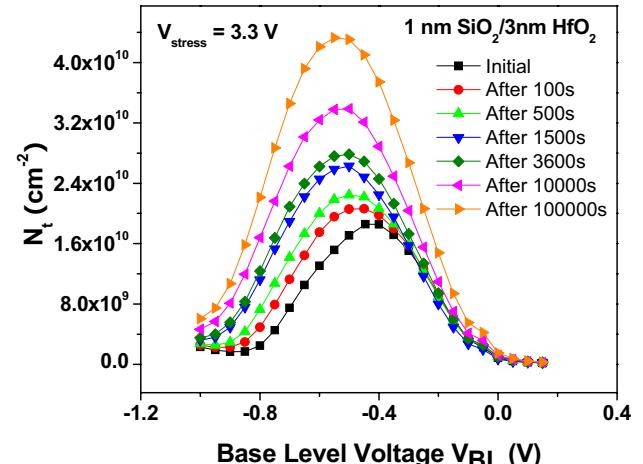


Fig.3 N_t calculated from 1MHz base level CP as a function of constant voltage stress time at $V_{stress} = 3.3 \text{ V}$. The amplitude of the CP pulse is $V_{amp} = 1 \text{ V}$.

LF noise is also measured as a function of V_g at each stressing step, and the noise spectrum at $V_g - V_{th} = 0.1 \text{ V}$ is used to monitor the increase in bulk trap density. The frequency axis can be translated to the tunneling depth through equ. (1). α , can be estimated to be 10^8 cm^{-1} if parameters for $\text{Si}-\text{SiO}_2$ system are used in equ. (2) [1]. The noise spectra are converted to trapping density profiles using equ.

(3). A representative illustration of the trap density extracted from $1/f$ noise spectra is shown in Fig. 5. In the frequency range of the LF measurement, below 1.6 kHz, the $1/f$ noise is caused by the traps located in the HfO_2 layer [13].

The trap density change as measured from CP and LF noise are quite different. This difference is most apparent when the relative (vs. initial value) trap density changes with the stress time are compared, as shown in Fig. 6. As the stress time increases, more traps are created in the HfO_2 layer than in the IL layer. After 10 hours of positive stressing, the noise extracted trap density increased 10 folds while the CP extracted density only doubled. This suggests that under the positive high voltage stress the trap generation rate in HfO_2 is much higher than in SiO_2 although the electric field across the SiO_2 layer is higher.

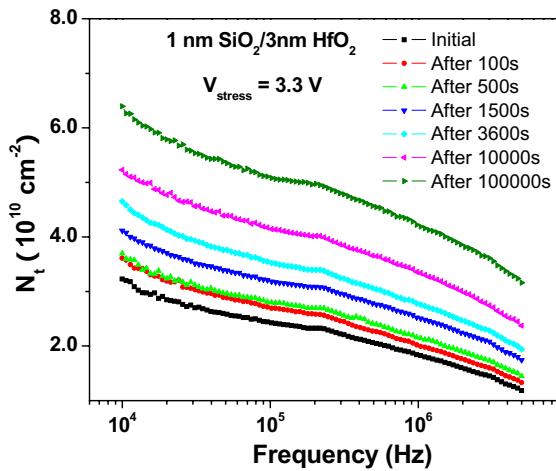


Fig.4 N_t calculated from frequency dependent CP as a function of constant voltage stress time at $V_{\text{stress}} = 3.3$ V. $V_{\text{amp}} = 1$ V.

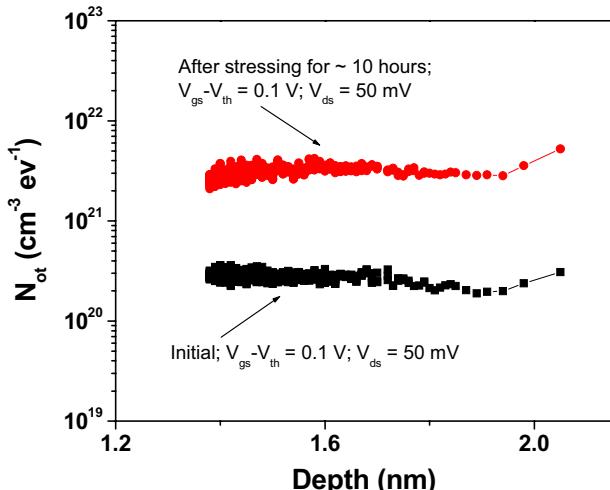


Fig.5 N_{ot} extracted from LF noise measurements at $V_{\text{gs}} - V_{\text{th}} = 0.1$ V for a fresh device and after it is stressed at $V_{\text{stress}} = 3.3$ V for 10 hours.

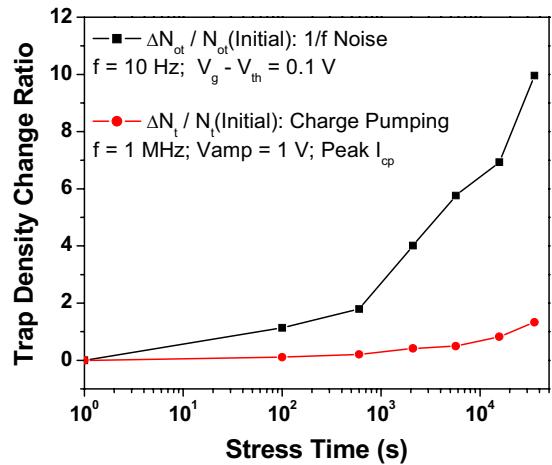


Fig.6 Comparison of the relative increase of the generated trap density calculated from LF noise and CP data as a function of stress time. $V_{\text{stress}} = 3.3$ V.

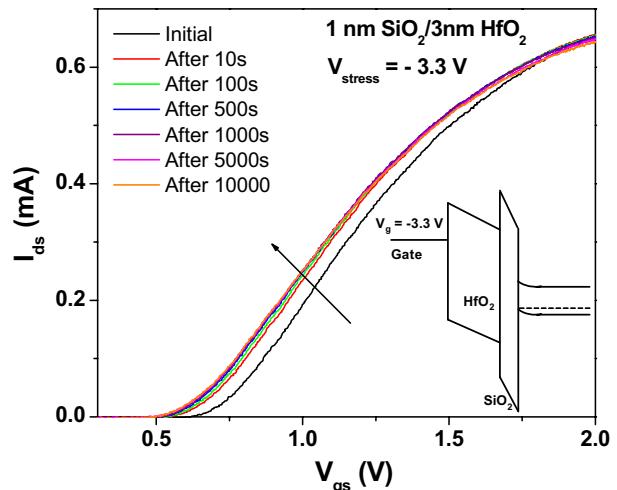


Fig.7 Change of the I_d - V_g characteristics during negative bias stress. The inset shows the band diagram of a nMOSFET with high-k gate stack under -3.3 V gate bias.

Figs. 7-10 show the resulting device degradation under negative constant voltage stress. After each stress step, a positive 1 V was applied on the gate for 30 s to empty the traps that can be detrapped, and fast I_d - V_g , CP, and LF noise measurements were performed. Negative CVS shifted the I_d - V_g curves to the left and decreased the threshold voltage linearly with stress time, as shown in Fig. 7. The variable base-level CP data at 1 MHz in Fig. 8 show an increase in the CP currents and trap density at and/or near the Si/SiO₂ interface. The shift of the peak location to the left indicates a larger amount of negatively trapped charge in the dielectrics, compared to the positive CVS results in Fig. 3. More importantly, the trap density at the peak position increased 10 folds, from $2.3 \times 10^{10} \text{ cm}^{-2}$ to $2.3 \times 10^{11} \text{ cm}^{-2}$, which is a much more dramatic degradation of the IL compared to

the positive CVS case. Frequency dependent CP measurements confirmed this change.

Comparison between the relative increase of the generated trap density from the CP and LF noise data, as shown in Fig. 10, points to a much larger defect generation rate in the interfacial SiO₂ region near the Si substrate than in the high-k bulk – an exact opposite to the case of the positive bias CVS. These results are in agreement with the traditional view that the traps are predominantly created close to the anode side, while the degree of asymmetry is larger than commonly assumed for such a thin dielectric layer.

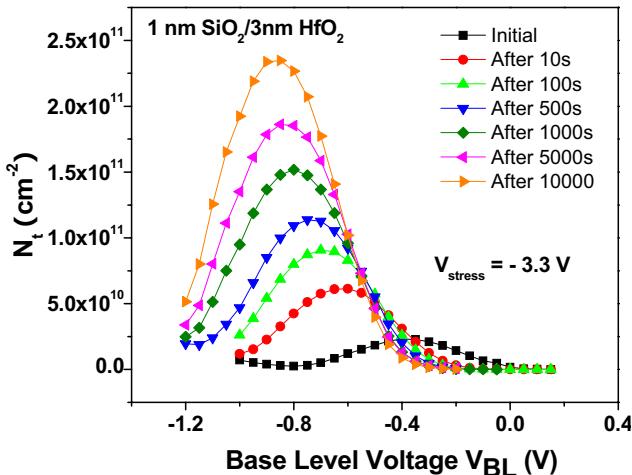


Fig.8 N_t calculated from 1MHz base level CP as a function of constant voltage stress time at $V_{\text{stress}} = -3.3$ V. The amplitude of the CP pulse is $V_{\text{amp}} = 1$ V.

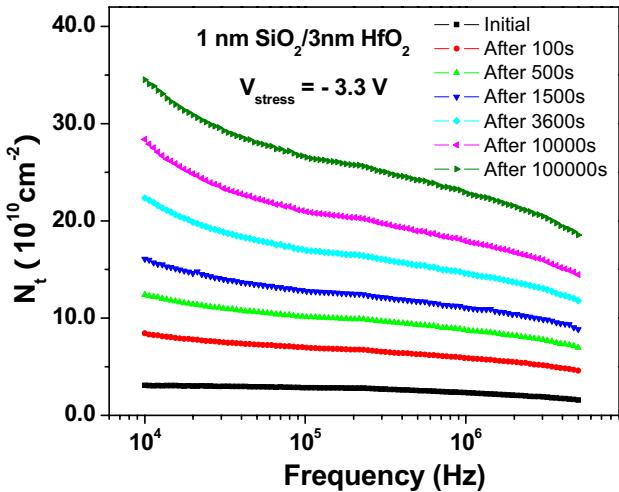


Fig.9 N_t calculated from frequency dependent CP as a function of constant voltage stress time at $V_{\text{stress}} = -3.3$ V. $V_{\text{amp}} = 1$ V.

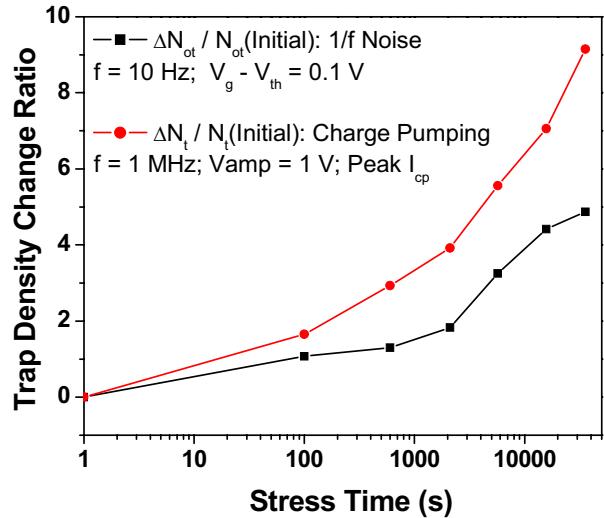


Fig.10 Comparison of the relative increase of the generated trap density calculated from LF noise and CP data as a function of stress time. $V_{\text{stress}} = -3.3$ V.

CONCLUSION

The low frequency drain current noise and frequency-dependent charge pumping current techniques have been used to obtain the volume trap profile for a large depth range where the traps can actively affect the current transport in the channel of the state-of-the-art CMOS transistors with high-k/SiO₂ dielectric stacks. Comparing the creation of new traps in both layers during the positive and negative stress, it is found that electrical stress in the substrate injection mode creates more traps in HfO₂ while gate injection mode generates more traps in interfacial SiO₂. The results show that the traps are predominantly created close to the anode side. Charge pumping and low frequency noise measurements have been demonstrated to provide a unique advantage to monitor the trap generation in both the High-k and IL layers. However, relation between higher trap density sensed by the noise measurements and SILC/breakdown characteristics of the gate stacks is not yet clear and needs further study.

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