THE FAST INITIAL THRESHOLD VOLTAGE SHIFT: NBTI OR HIGH-FIELD STRESS

J.P. Campbell[1]*, K.P. Cheung[1], J.S. Suehle[1], A. Oates[2]
[1]Semiconductor Electronics Division, NIST, Gaithersburg, MD 20899, 301-975-8308, *email: jason.campbell@nist.gov
[2]TSMC Ltd. No. 121, Park Ave. 3, Science-Based Industrial Park, Hsin-Chu, Taiwan 300-77, R.O.C.

ABSTRACT

Recent negative bias temperature instability (NBTI) studies have come to involve very high electric fields, yet these same studies are used to criticize the lower field "NBTI" models. This study examines both high- and low-field degradation phenomena by monitoring the initial threshold voltage shift (ΔV_{TH}) as a function of stress time and stress voltage. We demonstrate that the initial ΔV_{TH} is recoverable and decays rapidly as the stress voltage is reduced. We also monitor the transient transconductance (G_M) degradation which surprisingly indicates the presence of an electron trapping/de-trapping component. We argue that the initial ΔV_{TH} and G_M degradation behaviors are consistent with high-field stress degradation. The electron trapping component of the "recoverable" degradation is unexpected and must be addressed to insure accurate NBTI lifetime predictions. [*Keywords:* NBTI, High-Field Stress, hole-trapping, electron-trapping.]

INTRODUCTION

The emergence of NBTI as the major reliability concern in advanced CMOS technology has led to an explosion of recent literature concerning innovative methods to more accurately characterize this elusive phenomenon.[1-9] The main obstacle associated with NBTI characterization is that the degradation (negative threshold voltage shift (ΔV_{TH}) and drain current (I_D) reduction) is not permanent.[10] A portion of the degradation "recovers" very quickly towards the pre-stress state as soon as the stress is terminated.[10] This fast recovery is thought to contaminate most conventional electrical characterization techniques as the measured degradation (and consequent lifetime prediction) is strongly dependent on the time delay between stress and sense measurements.[7-11] This recovery-induced measurement contamination has led researchers to develop new measurement characterization schemes to either avoid [1, 5, 7-9, 11, 12] or carefully account for [2, 3] NBTI recovery. A particularly attractive technique, fast-I_DV_G, measures the full I_D-V_G characteristic within microseconds.[7-9, 13-16] This measurement approach greatly limits recovery and allows for a more accurate observation of degradation. Recent fast-I_DV_G measurements report an exceedingly large initial ΔV_{TH} (V_{TH}(time1) – V_{TH}(time0)) after short stress times in SiON pMOSFETs.[7-9] Such reports raise serious concerns regarding the lifetime of modern circuits.[17] While characterization of this fast recoverable degradation has been the topic of many recent publications, the origin of the fast-recoverable degradation is still quite controversial.

Despite many decades of NBTI study [18], the degradation mechanism is still not well understood. While hydrogen depassivation mechanisms have gained popularity in the last decade, [19-21] early experiments have suggested the presence of a hole-trapping mechanism.[22] Until recently, most NBTI studies involved relatively low oxide stress fields and no tunneling current. However these stress fields have been recently increasing, with most current stress fields >10 MV/cm (some even >15 MV/cm [23]). These higher stress fields induce high levels of tunneling current and consequent hot holes at the anode.[24] These hot holes, as well as the high density of cold holes in the channel, are attracted to the oxide-semiconductor interface by this increased vertical field. The consequence is a much higher level of hole-trapping and de-trapping. Under these modern NBTI stress conditions, one might expect that the resultant degradation should resemble a more severe high-field stress mechanism rather than the less severe NBTI mechanism. Most recent NBTI models depict a scenario in which the high-field stress-induced tunneling current is not emphasized. Such models will not be useful if a different mechanism (high-field stress) is dominating this degradation.

In this study, we report ΔV_{TH} and, for the first time, $\%G_M$ degradation extracted from fast-I_DV_G measurements before and after "NBTI" stress as well as after a recovery period. Our ΔV_{TH} measurements confirm recent reports concerning a recoverable degradation component.[3, 7-9] However, we find that the fast recoverable degradation is absent at operation conditions. We also conclude that this fast recoverable degradation is due to a high-field stress mechanism. Our G_M measurements illustrate a *post-recovery improvement* (to values better than before stress). We argue that this behavior is a signature of electron trapping/de-trapping phenomenon and is consistent with high-field stress degradation. Our results strongly suggest that what many NBTI researchers consider "reasonable" NBTI stress conditions actually involve this high-field stress component. The absence of this effect at operation conditions suggests a more optimistic NBTI-limited lifetime predictions.

EXPERIMENTAL METHODS

This study utilizes 2 x 0.07 μm^2 and 2 x 0.09 μm^2 (physical gate area) fully-processed pMOSFETs with SiON gate dielectrics (t_{ox} = 1.6 nm). A schematic diagram of our fast-I_DV_G measurement is shown in figure 1. In this measurement, a voltage pulse is applied to the gate electrode while the drain current is monitored by a fast operational amplifier circuit. The gate voltage and drain current waveforms are captured by a digital oscilloscope. The fast-I_DV_G measurement time is limited to 2 μsec in these measurements. The details of this measurement methodology have been discussed elsewhere. [15, 25]

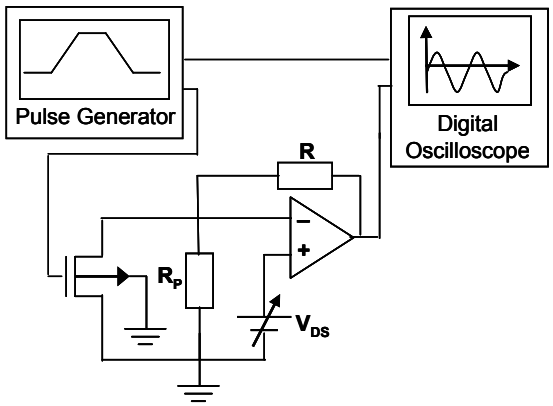

FIGURE 1. FAST-I_DV_G EXPERIMENTAL SET-UP USING A PULSE GENERATOR, DIGITAL OSCILLOSCOPE, AND FAST AMPLIFIER CIRCUIT.

978-1-4244-2050-6/08/$25.00 ©2008 IEEE

IEEE CFP08RPS-CDR 46th Annual International Reliability Physics Symposium, Phoenix, 2008

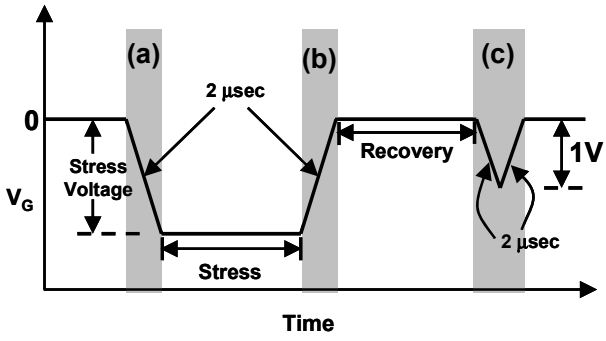

FIGURE 2: SCHEMATIC DIAGRAM OF THE GATE VOLTAGE PULSES DURING STRESS AND MEASUREMENT SEQUENCES. V_{TH} AND G_M VALUES ARE EXTRACTED AT (A), (B), AND (C).

The gate voltage pulses used in this study are schematically shown in figure 2. The pulse train consists of a trapezoidal "stress" pulse and a triangular post-recovery "sense" pulse separated by a variable recovery time where the gate voltage is held at 0 V. Fast-I_DV_G measurements were taken at all rising and falling edges of the pulse train to obtain pre-stress (a), post-stress (b), and post-recovery (c) fast-I_DV_G measurements. The post-recovery V_{TH} and G_M values consist of the average of the falling and rising measurements of the sense pulse (c). Throughout this manuscript we report two different sets of ΔV_{TH} and $\%G_M$ degradation values as per the following relations with reference to figure 2:

$$\Delta V_{TH}(ab) = V_{TH}(b) - V_{TH}(a) \quad (1a)$$

$$\Delta V_{TH}(ac) = V_{TH}(c) - V_{TH}(a) \quad (1b)$$

$$\%G_M \text{ Degradation } (ab) = \frac{G_M(a) - G_M(b)}{G_M(a)} \times 100 \quad (1c)$$

$$\%G_M \text{ Degradation } (ac) = \frac{G_M(a) - G_M(c)}{G_M(a)} \times 100 \quad (1d).$$

All reported V_{TH} values are derived from a tangent line drawn at the peak-G_M position. All $\%G_M$ degradation data reflect changes in the peak G_M values. A drain voltage of -50 mV is maintained at all times while the source and substrate remain grounded.

Typical fast-I_DV_G measurements using digital oscilloscopes are too noisy to extract V_{TH} and G_M directly. Therefore, digital filtering techniques must be used. We have developed a filter that is formally equivalent to the well-known Savitzky-Golay method. While our filter is far less efficient in computation than the Savitzky-Golay method, its ability to handle unequally spaced data is the motive for developing our own routine. Figures 3a and 3b illustrate the raw and filtered I_DV_G characteristics collected using our fast-I_DV_G apparatus as well as a semiconductor parameter analyzer. We note that our filtered I_DV_G curves exhibit very good agreement with the DC characteristics. Figure 3c illustrates the corresponding G_M-V_G characteristic curves from the fast-I_DV_G and DC parameter analyzer measurements, where $G_M = dI_D/dV_G$. Again, we observe very good agreement between the fast-G_M and DC-G_M measurements. This agreement is sufficient to allow for accurate observations of NBTI-induced G_M degradation.

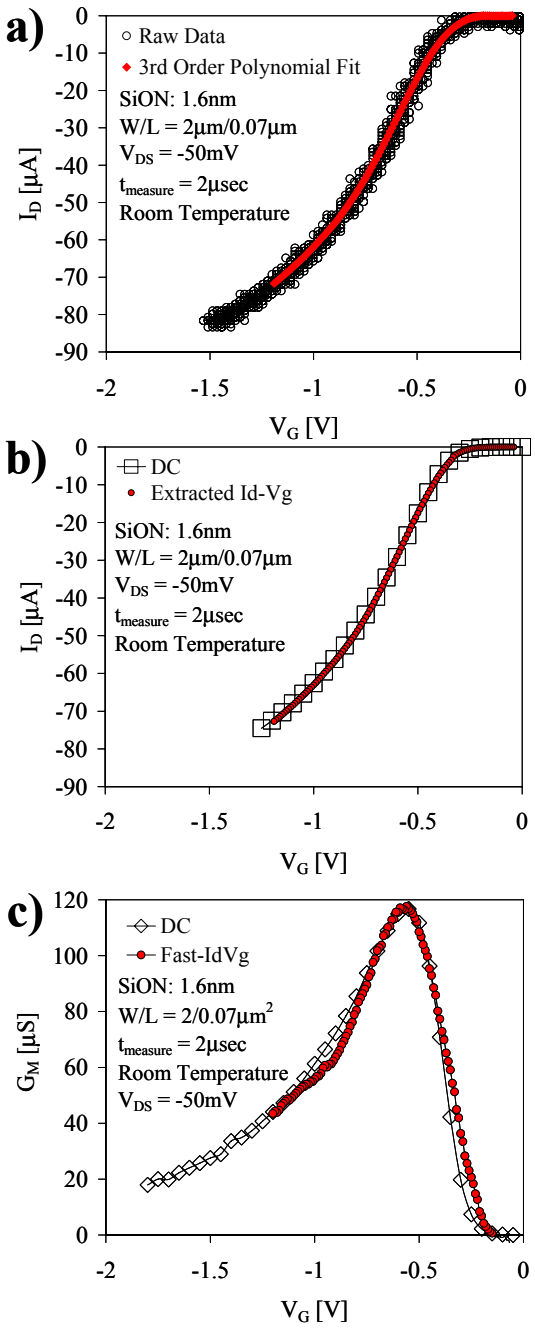

FIGURE 3: OUR FAST-I_DV_G CHARACTERISTICS ARE SUBJECT TO SIGNIFICANT NOISE. WE UTILIZE A "MOVING" THIRD-ORDER POLYNOMIAL FITTING PROCEDURE TO EXTRACT THE I_DV_G CHARACTERISTIC CURVES FROM THE RAW DATA (A). OUR EXTRACTED I_DV_G (B) AND G_M (C) CHARACTERISTICS AGREE VERY WELL WITH DC MEASUREMENTS.

RESULTS

Figure 4 illustrates ΔV_{TH}(ab) as a function of stress voltage (-1.2 V to 2.7 V) for various stressing times (0.1 to 1000 seconds). To improve the accuracy of the ΔV_{TH} extraction, we repeat the measurement sequence (figure 2) 12 times for the 0.1, 1, and 10 second stress times, 3 times for the 100 second stress time, and 1

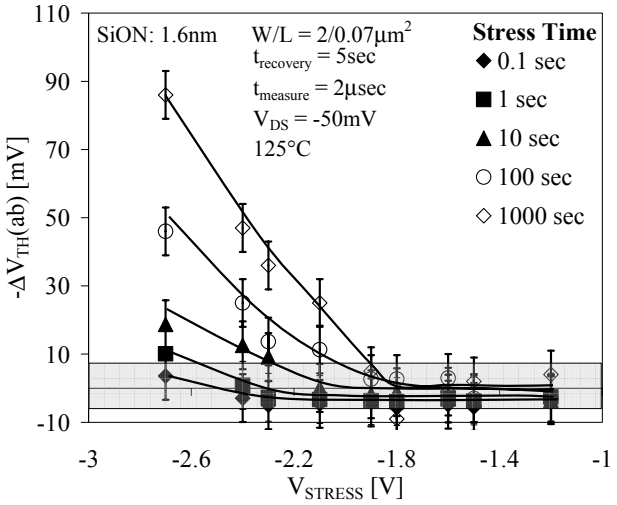

FIGURE 4: ΔV_{TH}(ab) AS A FUNCTION OF STRESS VOLTAGE FOR VARIOUS STRESS TIMES. IT IS CLEAR THAT THE FAST NBTI DEGRADATION ONLY OCCURS FOR EXCEEDINGLY HIGH STRESS VOLTAGES AND LONGER STRESS TIMES. THE BOX CENTERED ABOUT 0MV REPRESENTS 1 STANDARD DEVIATION ERROR BAR. THE LINES ARE ONLY A GUIDE FOR THE EYE.

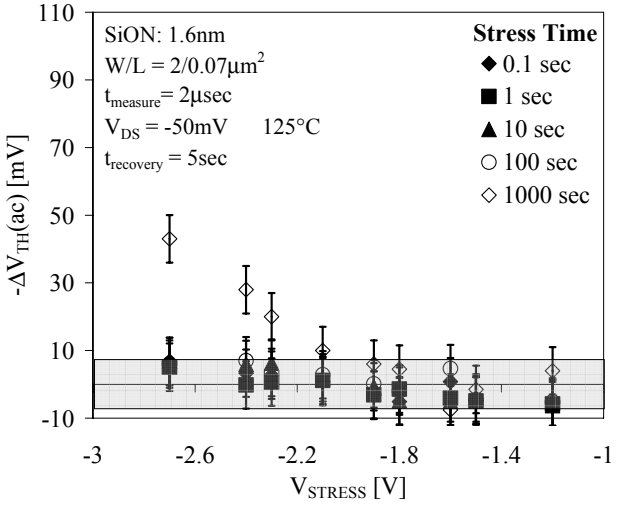

FIGURE 5: ΔV_{TH}(ac) AS A FUNCTION OF STRESS VOLTAGE FOR VARIOUS STRESSING TIMES. WITH THE EXCEPTION OF THE 1000 SECOND STRESS, ALL OF THE STRESS INDUCED ΔV_{TH} IS "RECOVERABLE".

time for the 1000 second measurement. We repeated the experiments on the same device (to improve statistics) only for the shorter stress times which do not generate significant degradation. It is clear from these ΔV_{TH}(ab) measurements that a large initial ΔV_{TH} is only observable at *exceedingly high* stress voltages and long stress times. Throughout the rest of this paper, we will argue that the high stress voltage (not a traditional NBTI degradation) is responsible for the large initial ΔV_{TH}.

Figure 5 illustrates ΔV_{TH}(ac) as a function of gate bias for the same stress voltages and times as shown in figure 4 (recovery time = 5 seconds). An increase in ΔV_{TH}(ac) indicates that the stress introduces a "permanent" (not recoverable in 5 seconds) ΔV_{TH}. With the exception of the 1000 second stress measurement at high stress voltages, all other stress voltages and times are dominated by a fast "recoverable" component and exhibit insignificant permanent ΔV_{TH}. This is true even for exceedingly high stress voltages. An examination of figures 4 and 5 allows us to safely conclude that the large initial "recoverable" ΔV_{TH} is strongly dependent on stress voltage and, with the exception of longer stress durations, has little to do with traditional permanent NBTI degradation mechanisms.[20]

To further examine the dependence of stress voltage on the initial recoverable ΔV_{TH}, we have utilized our filtering scheme to examine the corresponding G_M characteristic curves. Figure 6 illustrates $\%G_M$ degradation(ab) as a function of stress voltage and stress times corresponding to figure 4. We observe a $\%G_M$ degradation(ab) trend that mimics the ΔV_{TH} trend (increased G_M degradation at higher stress voltages and longer stress times), which also exhibits a very strong dependence on the stress voltage.

Figure 7 illustrates $\%G_M$ degradation(ac) as a function of stress voltage for various stress times (recovery time = 5 seconds). Surprisingly, as the stress voltage and stress duration increase, we observe negative $\%G_M$ degradation(ac) values. Negative $\%G_M$ degradation(ac) values represent an improvement in G_M to values which are better than before stress. Clearly, this G_M behavior does not mimic the ΔV_{TH} trends observed in figure 5.

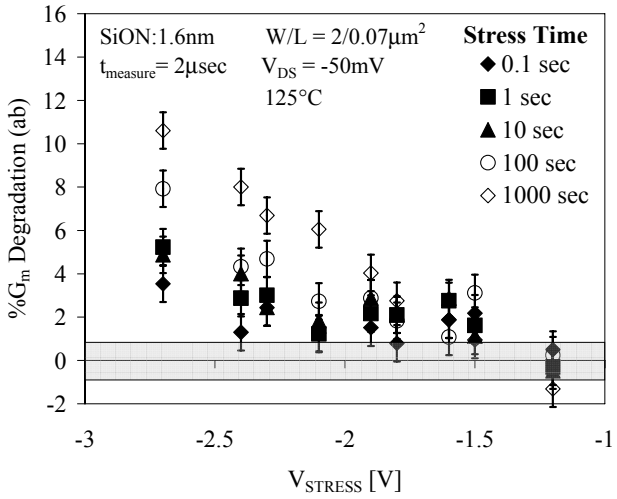

FIGURE 6: $\%G_M$ DEGRADATION(ab) AS A FUNCTION OF STRESS VOLTAGE FOR VARIOUS STRESS TIMES. THE G_M DEGRADATION(ab) FOLLOWS A SIMILAR TREND (LARGE DEGRADATIONS ONLY AT HIGH VOLTAGES) AS ΔV_{TH}(ab) (FIGURE 4). THE BOX CENTERED ABOUT 0 MV REPRESENTS ONE STANDARD DEVIATION ERROR BAR.

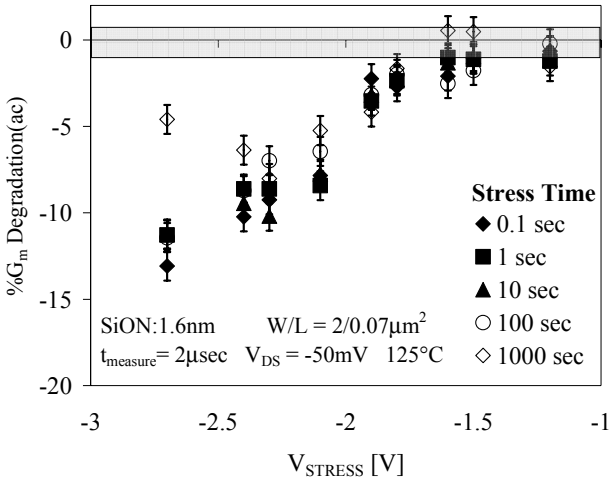

FIGURE 7: %GM DEGRADATION(ac) AS A FUNCTION OF STRESS VOLTAGE FOR VARIOUS STRESS TIMES. WE OBSERVE AN IMPROVEMENT IN G_M (BETTER THAN PRE-STRESS). THIS CAN BE EXPLAINED BY THE PRESENCE OF ELECTRON TRAPPING/DE-TRAPPING PHENOMENON. THE TRAPPED ELECTRONS CAN COMPENSATE POSITIVELY CHARGED INTERFACE TRAPS AND REDUCE THE COULOMBIC SCATTERING.

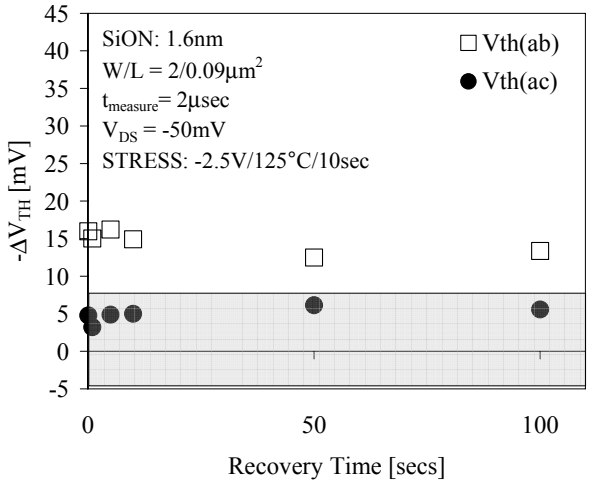

FIGURE 8: ΔV_{TH}(ab) AND ΔV_{TH}(ac) AS A FUNCTION OF RECOVERY TIME. THE BOX CENTERED ABOUT 0 MV REPRESENTS 1 STANDARD DEVIATION ERROR BAR.

DISCUSSION

We have argued that the observed stress voltage degradation trends are consistent with high-field stress phenomena. The observed G_M improvement after a 5 second recovery period is particularly clear evidence. It is well known that high-field stress leads to hole *and electron trapping* as well as interface state generation.[26, 27] At the conclusion of our stress, there are very likely trapped holes (positive charge), trapped electrons (negative charge), and (in inversion) positively charged interface states. The positive charge due to trapped holes and interface states (in inversion) overwhelms the negative charge from the trapped electrons, and we observe a net negative shift in threshold voltage (figure 4) and G_M degradation (figure 6). During the recovery period, both the trapped holes and electrons de-trap. It is well known that the hole de-trapping rate is much higher than the electron de-trapping rate.[28] The result is a decrease in the net positive charge as a function of time (ΔV_{TH}(ac) recovery seen in figure 5). After the 5 second recovery period, a significant portion of the trapped holes have de-trapped while most of the trapped electrons still remain. This results in a net negative trapped charge in the oxide. This negative charge compensates the positively charged interface states, leading to a reduction in Coulombic scattering and an improvement in G_M (figure 7).

If we wait long enough, the trapped electrons will also de-trap, and the compensation effect will diminish. Therefore, we would expect the Coulombic scattering to increase over time and the G_M to decay towards the post-stress degraded state (due to the generated interface states). To examine this scenario, we stressed a second set of devices (-2.5V/125°C/10 seconds) and measured ΔV_{TH} and G_M degradations as a function of recovery time. Figure 8 illustrates the ΔV_{TH}(ab) and ΔV_{TH}(ac) as a function of recovery time. Again, we use a fresh device for each recovery time and average 12 measurements to improve accuracy. The ΔV_{TH}(ab) is independent of recovery time and is plotted for reference only. The ΔV_{TH}(ac) trend, as expected from figure 5, is located within the error of the measurement. However, the corresponding $\%G_M$ degradation(ac) (figure 9) indeed follow our electron trapping expectation with the $\%G_M$ degradation(ac) exhibiting improvement at short recovery times and degradation at longer recovery times. Again, $\%G_M$ degradation(ab) is independent of recovery time and is plotted for reference only.

The observed recoverable G_M degradation(ac) trend in figure 9 is consistent with our high-field stress interpretation. At the time of the first post-recovery measurement (0.1 seconds), a large portion of the trapped holes have de-trapped. This leaves a net negative charge in the bulk which compensates the positive interface state charges and is observed via $\%G_M$ degradation(ac) improvement. At longer recovery times, the slower electrons are given time to de-trap, and the net negative charge in the dielectric diminishes. This leaves the positive interface state charges, which are now uncompensated, and the $\%G_M$ degradation(ac) values return to degradation. This G_M behavior is further evidence that a high-field stress component (which includes an as-yet-unaccounted-for electron trapping/de-trapping component) is present during these measurements.

In addition to the electron trapping/G_M observations, an examination of figures 4 and 5 also yields some very interesting insights into the high-field stress component. We note that the initial ΔV_{TH}(ab) is only large for *exceedingly high stress voltages and stress durations*. In these devices, the measured ΔV_{TH}(ab) is only significant at gate bias stress >1.8 V. This roughly corresponds to a dielectric field of ≈9 MV/cm. At operation conditions (-1.2 V), there is no observable ΔV_{TH}(ab). With the exception of the 1000 second stress case, the measured ΔV_{TH} at stress voltages >1.8 V are completely recoverable. Within experimental error, we do not observe any significant non-recoverable threshold voltage shift for the 0.1 and 1 second stress times (open diamonds and open circles in figure 4) even at high stress voltages. The non-recoverable degradation seen in the 1000 second stress case is likely due to increased interface state generation. Since high-field stress and traditional NBTI are both known to generate interface states, this

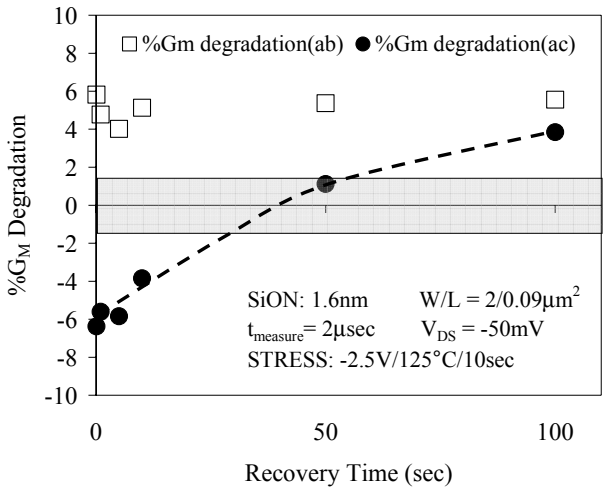

FIGURE 9: $\%G_M$ DEGRADATION(ab) AND $\%G_M$ DEGRADATION(ac) AS A FUNCTION OF RECOVERY TIME CORRESPONDING TO FIGURE 8. SINCE THE $\%G_M$ DEGRADATION(ab) MEASUREMENTS ALL EXHIBIT DEGRADATION, THE $\%G_M$ DEGRADATION(ac) VALUES MUST TRANSITION FROM DEGRADATION TO IMPROVEMENT BEFORE THE FIRST RECOVERABLE MEASUREMENT AT 0.1 SECONDS. AS THE RECOVERY TIME INCREASES, THE $\%G_M$ DEGRADATION(ac) VALUES RETURN TO THE DEGRADED STATE.. THE BOX CENTERED ABOUT 0 % REPRESENTS 1 STANDARD DEVIATION ERROR BAR. THE LINES ARE ONLY A GUIDE FOR THE EYE.

data set (1000 seconds stress) cannot distinguish which mechanism is more dominant. The realization that advanced CMOS operates at fields >6 MV/cm suggests that both mechanisms (high-field stress and NBTI) are relevant. However, the dominance of either mechanism may drastically change lifetime projections.

Since V_{TH} recovery is believed to be largely due to hole de-trapping, [29] this observation is in good agreement with known high-field stress behavior.[17] It is known that hole trapping is largely a function of the stress field [17] and that it is difficult to create significant densities of new hole-traps.[30] Therefore, the recoverable degradation due to hole trapping is simply a function of the stress field and will not increase over time. Our data suggest that hole trapping decreases with stress voltage such that it is not a factor at operation voltages. Thus, the current debate on the inclusion of the fast recoverable degradation in the NBTI lifetime projection can be settled.

On the other hand, our G_M data (figure 9) introduces a new, slower "recoverable" degradation due to electron trapping and de-trapping. It is well known from high-field stress phenomena that electron trap densities increase significantly with electrical stress over time. In most NBTI studies, the measurement conditions are such that, during measurement, all the trapped electrons are neutralized by the inversion layer holes. The electron trapping effect is only observable when the measurement time is fast (like in our case). Since the modern circuit frequencies are even faster than our measurements, the electron trapping effect cannot be ignored.

One might wonder why the $\%G_M$ degradation(ac) trend is not reflected in the V_{TH}(ac) measurements. We believe this is simply due to our signal-to-noise ratio (relatively small ΔV_{TH}). We verified this assumption using much harsher stress (higher voltage and longer time) and found a good correspondence between the V_{TH}(ac) and $\%G_M$ degradation(ac) trends (not shown).

The increase in advanced CMOS operation fields dictates that NBTI measurements result in both traditional NBTI and high-field stress. Since the avoidance of high-field stress, as was previously proposed by Mahapatra and co-workers, [31] is becoming less practical, the NBTI community must understand the contribution of high-field stress to NBTI. Our observations of electron trapping must be clarified to ensure accurate NBTI lifetime projections. Additionally, the net dominance of each mechanism is likely dependent on device processing [32] and circuit environment (AC/DC).[33] Recent reports, have detailed admirable attempts to separate these two different degradation mechanisms.[3, 4] However, the proper choice of stress conditions and measurement technique is no longer trivial.

CONCLUSIONS

We have utilized fast-I_dV_g measurements to examine the initial ΔV_{TH} and percentage change in peak-G_M in ultrathin SiON pMOSFETs subject to various NBTI stressing conditions. The large initial ΔV_{TH} is only observable at *exceedingly high* stress voltages and long stress times (conditions that are inconsistent with NBTI). This data strongly suggests that high-field stress (and likely electron traps) play significant roles in the initial recoverable ΔV_{TH} which many researchers attribute to NBTI. This result has obvious implications to lifetime extrapolations as the dominance of the initial high-field induced ΔV_{TH} alters the lifetime predictions. These factors greatly complicate the characterization and modeling of NBTI as well as the subsequent NBTI-limited lifetime predictions.

ACKNOWLEDGMENTS

This research was funded by the National Research Council and the National Institute of Standards and Technology Office of Microelectronic Programs. The authors would like to acknowledge M. Gurfinkel for fruitful conversations regarding measurement methodology.

REFERENCES

[1] M. Denais, A. Bravaix, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, Y. Rey-Tauriac, and N. Revil, "On-the-Fly Characterization of NBTI in Ultra-Thin Gate Oxide pMOSFET's," *IEEE Int. Electron Devices Meet.*, pp. 109-112, (2004)

[2] T. Grasser, W. Gos, V. Sverdlov, and B. Kaczer, "The Universality of NBTI Relaxation and its Implications for Modeling and Characterization," *IEEE Int. Reliability Phys. Symp.*, pp. 268-280, (2007)

[3] T. Grasser, B. Kaczer, P. Hehenberger, W. Goes, R. O'Connor, H. Reisinger, W. Gustin, and C. Schlunder, "Simultaneous Extraction of Recoverable and Permanent Components Contributing to Bias-Temperature Instabilities," *IEEE Int. Electron Devices Meet.*, pp. 801-804, (2007)

[4] V. Huard, C. Parthasarathy, N. Rallet, C. Guerin, M. Mammase, D. Barge, and C. Ouvrard, "New Characterization and Modeling approach for NBTI Degradation from Transistor to Product Level," *IEEE Int. Electron Devices Meet.*, pp. 797-800, (2007)

[5] A. E. Islam, E. N. Kumar, H. Das, S. Purawat, V. Maheta, H. Aono, E. Murakami, S. Mahapatra, and M. A. Alam, "Theory and Practice of On-the-fly and Ultra-fast V_T Measurements for NBTI Degradation: Challenges and Opportunities," *IEEE Int. Electron Devices Meet.*, pp. 805-808, (2007)

[6] A. T. Krishnan, C. Chancellor, S. Chakravarthi, P. E. Nicollian, V. Reddy, A. Varghese, R. B. Khamankar, and S. Krishnan, "Material Dependence of Hydrogen Diffusion: Implication for NBTI Degradation," *IEEE Int. Electron Devices Meet.*, pp. 705-708, (2005)

[7] C. Shen, M. F. Li, C. E. Foo, T. Yang, D. M. Huang, A. Yap, G. S. Samudra, and Y. C. Yeo, "Characterization and Physical Origin of Fast V_{TH} Transient in NBTI of pMOSFETs with SiON," *IEEE Int. Electron Devices Meet.*, pp. 333-336, (2006)

[8] T. Yang, M. F. Li, C. Shen, C. H. Ang, Chunxiang Zhu, Y. C. Yeo, G. Samudra, S. C. Rustagi, M. B. Yu, and D. L. Kwong, "Fast and Slow Dynamic NBTI Components in p-MOSFET with SiON Dielectric and Their Impact on Device Lifetime and Circuit Application," *Symp. on VLSI Technol.*, pp. 92-93, (2005)

[9] T. Yang, C. Shen, M. F. Li, C. H. Ang, C. X. Zhu, Y. C. Yeo, G. Samudra, and D. L. Kwong, "Interface Trap Passivation Effect in NBTI Measurement for p-MOSFET with SiON Gate Dielectric," *IEEE Electron Device Lett.,* vol. 26, pp. 758-760, (2005)

[10] M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, "Dynamic Recovery of Negative Bias Temperature Instability in p-type Metal-Oxide-Semiconductor Field-Effect Transistors," *Appl. Phys. Lett.,* 83, pp. 1647-1649, (2003)

[11] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal Recovery Behavior of Negative Bias Temperature Instability," *IEEE Int. Electron Devices Meet.*, pp. 341-344, (2003)

[12] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, "Analysis of NBTI Degradation- and Recovery-Behavior Based on Ultrafast V_T-Measurements," *IEEE Int. Reliability Phys. Symp.*, pp. 448-453, (2006)

[13] A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the V_T-Instability in SiO_2/HfO_2 Gate Dielectrics," *IEEE Int. Reliability Phys. Symp.*, pp. 41-45, (2003)

[14] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumor, and F. Martin, "Characterization and Modeling of Hysteresis Phenomena in High-K Dielectrics," *IEEE Int. Electron Devices Meet.*, pp. 737-740, (2004)

[15] C. Shen, M. F. Li, X. P. Wang, Y. C. Yeo, and D. L. Kwong, "A Fast Measurement Technique of MOSFET Id-Vg Characteristics," *IEEE Electron Device Lett*., 27, pp. 55-57, (2006)

[16] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, "Interfacial Layer Dependence of $HFSi_xO_y$ Gate Stacks on V_T Instability and Charge Trapping Using Ultra-short Pulse in Characterization," *IEEE Int. Reliability Phys. Symp.*, pp. 75-79, (2005)

[17] A. Haggag, G. Anderson, S. Parihar, D. Burnett, G. Abeln, J. Higman, and M. Moosa, "Understanding SRAM High-Temperature-Operating-Life NBTI: Statistics and Permanent vs Recoverable Damage," *IEEE Int. Reliability Phys. Symp.*, pp. 452-456, (2007)

[18] B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow, "Characteristics of Surface-State Charge (Qss) of Thermally Oxidized Silicon," *J. Electrochem. Soc.,* 114, pp. 266-274, (1967)

[19] M. A. Alam and S. Mahapatra, "A Comprehensive Model of PMOS NBTI Degradation," *Microelectron. Rel.,* 45, pp. 71-81, (2005)

[20] K. O. Jeppson and C. M. Svensson, "Negative Bias Stress of MOS Devices at High Electric-Fields and Degradation of MNOS Devices," *J. Appl. Phys.,* 48, pp. 2004-2014, (1977)

[21] S. Ogawa and N. Shiono, "Generalized Diffusion-Reaction Model for the Low-Field Charge-Buildup Instability at the Si-SiO_2 Interface," *Phys. Rev. B,* 51, pp. 4218-4230, (1995)

[22] D. J. Breed, "New Model for Negative Voltage Instability in MOS Devices," *Appl. Phys. Lett.,* 26, pp. 116-118, (1975)

[23] K. Sakuma, D. Matsushita, K. Muraoka, and Y. Mitani, "Investigation of Nitrogen-Originated NBTI Mechanism in SiON with High-Nitrogen Concentration," *IEEE Int. Reliability Phys. Symp.*, pp. 454-460, (2006)

[24] D. Varghese, S. Mahapatra, and M. A. Alam, "Hole Energy Dependent Interface Trap Generation in MOSFET Si/SiO_2 Interface," *IEEE Electron Device Lett.,* 26, pp. 572-574, (2005)

[25] M. Gurfinkel, J. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, "Ultra-Fast Characterization of Transient Gate Oxide Trapping in SiC MOSFETs," *IEEE Int. Reliability Phys. Symp.*, pp. 462-466, (2007)

[26] D. J. DiMaria and J. H. Stathis, "Anode Hole Injection, Defect Generation, and Breakdown in Ultrathin Silicon Dioxide Films," *J. Appl. Phys.,* vol. 89, pp. 5015-5024, (2001)

[27] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky, "Trap Generation and Occupation Dynamics in SiO_2 Under Charge Injection Stress," *J. Appl. Phys.,* 60, pp. 2024-2035, (1986)

[28] K. P. Cheung, D. Misra, K. G. Steiner, J. I. ColonelI, C. P. Chang, W. Y. C. Lai, C. T. Liu, R. Liu, and C. S. Pai, "Is NMOSFET Hot Carrier Lifetime Degraded By Charging Damage?," *Plasma Process-Induced Damage*, pp. 186-188, (1997)

[29] V. Huard and M. Denais, "Hole Trapping Effect on Methodology for DC and AC Negative Bias Temperature Instability Measurements in pMOS Transistors," *IEEE Int. Reliability Phys. Symp.*, pp. 40-45, (2004)

[30] T. Brozek and C. R. Viswanathan, "Generation of Hole Traps in Thin Silicon Oxide Layers Under High-Field Electron Injection," *Appl. Phys. Lett.,* 68, pp. 1826-1828, (1996)

[31] S. Mahapatra, P. B. Kumar, and M. A. Alam, "Investigation and Modeling of Interface and Bulk Trap Generation During Negative Bias Temperature Instability of p-MOSFETs," *IEEE Trans. Electron Devices,* 51, pp. 1371-1379, (2004)

[32] S. Mahapatra, K. Ahmed, D. Varghese, A. E. Islam, G. Gupta, L. Madhav, D. Saha, and M. A. Alam, "On the Physical Mechanism of NBTI in Silicon Oxynitride p-MOSFETs: Can Differences in Insulator Processing Conditions Resolve the

Interface Trap Generation versus Hole Trapping Controversy?," *IEEE Int. Reliability Phys. Symp.*, pp. 1-9, (2007)

[33] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, "A Comprehensive Framework for Predictive Modeling of Negative Bias Temperature Instability," *IEEE Int. Reliability Phys. Symp.*, pp. 273-282, (2004)