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Three-Dimensional Simulation Study of the Improved On/Off Current Ratio in Silicon Nanowire Field-Effect Transistors

Chang-Yong Choi, Won-Ju Cho and Sang-Mo Koo*
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 111-111

Sangsig Kim
Department of Electrical Engineering and Institute for Nano Science, Korea University, Seoul 111-111

Qiliang Li
Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA, U.S.A.

John S. Suehle and Curt A. Richter
Semiconductor Electronics Division, National Institute of Standards and Technology, MD, U.S.A.

Eric M. Vogel
Department of Electrical Engineering, University of Texas Dallas, Richardson, TX, U.S.A.

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In this paper, we report an approach based on three-dimensional numerical simulations for the investigation of the dependence of the on/off current ratio in silicon nanowire (SiNW) field-effect transistors (FETs) on the channel width. In order to investigate the transport behavior in devices with different channel geometries, we have performed detailed two-dimensional and three-dimensional simulations of SiNWFETs and control FETs with a fixed channel length L and thickness t but varying the channel width W from 5 nm and 5 μm. By evaluating the charge distributions and the current flowlines of both the two- and three-dimensional structures, we have shown that the increase in the 'on state' conduction current in the SiNW channel is a dominant factor, which consequently results in more than a two order of magnitude improvement in the on/off current ratio.

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I. INTRODUCTION

Silicon nanowires (SiNWs) have been regarded as a promising alternative for next-generation complementary metal-oxide-semiconductor field effect transistor (CMOS) devices and biosensors [1,2]. SiNW field effect transistors (FETs), without additional contact doping, typically have source/drain Schottky contacts and have merits compared with conventional MOSFETs; for example, fewer process steps due to no contact doping and good gate control characteristics due to high immunity to the short channel effect (SCE) [3]. Recently, an increase in the on/off current ratio (I_{ON}/I_{OFF}) of SiNWFETs was observed with decreasing channel dimensions [4–9], which contributed to their ultra-small channel dimensions. However, so far very little work examining this effect in detail has been published.

In this paper, in order to investigate this phenomenon, we performed both two- and three-dimensional numerical simulation by using the ATLAS simulator of Silvaco International [10]. We demonstrate a comparison between two devices with fixed channel lengths ($L \sim 10$ μm) and thicknesses ($t \sim 20$ nm) but varying the channel width ($W \sim 5$ μm and 5 nm). The inversion carrier distribution in the channel region was evaluated based on the two-dimensional (2-D) structures for both the on- and the off-bias conditions. Three dimensional (3-D) simulations have been performed to further investigate the drain current density and the carrier distribution in the channel for both on- and off-bias conditions.

II. EXPERIMENTS AND DISCUSSION

Two- and three-dimensional simulations were performed using the ATLAS numerical simulator of Silvaco

*E-mail: smkoo@kw.ac.kr; Fax: +82-2-940-5763

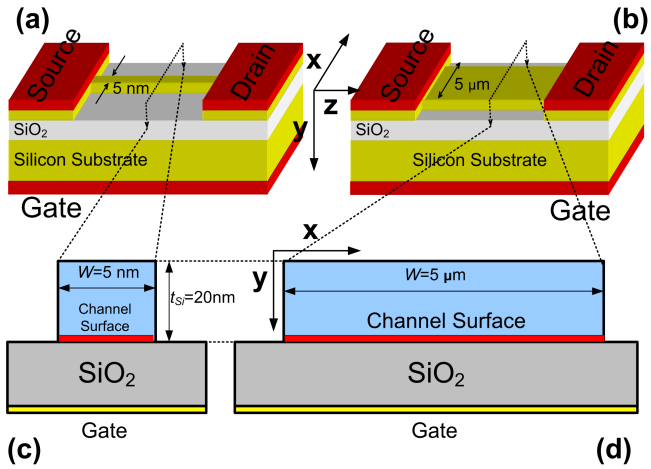

Fig. 1. Schematic diagrams of the (a) SiNWFET and (b) reference FET structures and the channel cross-sectional schematics of the (c) SiNW and (d) reference MOS structures.

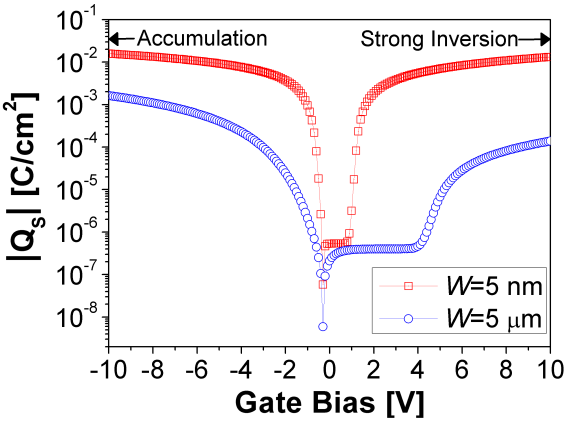

Fig. 2. Extracted absolute charge density $|Q_S|$ as a function of gate bias (−10 to 10 V) for the channels in the SiNW and the reference FETs.

International [10] to investigate the effect that occurs as the channel width becomes narrower on the inversion carrier generation. The schematic perspective views and channel cross-sections of the devices studied in this work are shown in Figures 1(a) and (b), respectively. The SiNWFET and the reference FET were simulated with a fixed channel length ($L \sim 10$ μm) and thickness ($t \sim$ 20 nm) but varying the channel width ($W \sim 5$ nm and $W \sim 5$ μm). Both the silicon channel and the substrate were doped with boron ($N_A \sim 2 \times 10^{15}$ cm^{-3}). We used 4.6 eV (similar to molybdenum or chromium [11]) for the workfunction of the source/drain and the gate. The thickness of the buried oxide (BOX) and the Si substrate layer are ∼100 nm and ∼300 nm, respectively. We assumed that no charge exists at each interface and in the BOX layer. The dimensions of the source and the drain contact were ∼5 × 5 μm. As shown in Figures 1(c) and (d), the 2D structures are from the cross-sectional planes of each three-dimensional FET device ($W \sim 5$ nm and

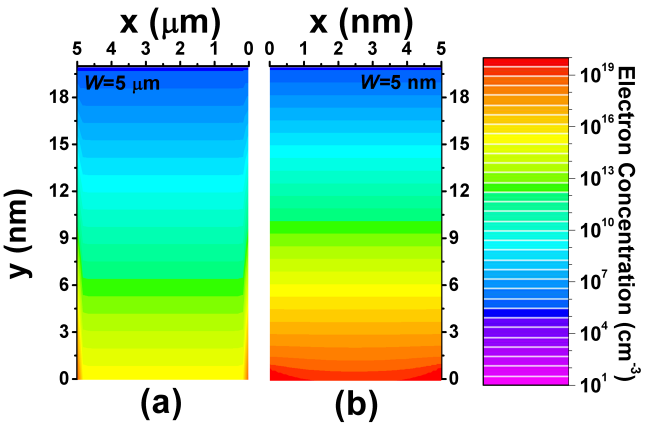

Fig. 3. Electron concentration distributions in the channels of the (a) reference and the (b) SiNW MOS structures at the on-state ($V_G \sim 10$ V). (Not drawn to scale. Note the difference in the X-axis scale.)

5 μm) and were cut in a direction of perpendicular to the channel length. The doping level of the channel was kept the same as that of 3-D structures ($N_A \sim 2 \times 10^{15}$ cm^{-3}).

The two structures shown in Figures 1(c) and (d) were simulated and compared to each other. First, we extracted the absolute quantity of charges per cm^2, Q_S, that exists in the region from the surface to a depth of 2 nm as a function of the gate bias, as shown in Figure 2. This quantity Q_S, corresponding to the inversion carrier concentration, may readily contribute to the conduction current for both on- and off-bias conditions. At zero gate bias $V_G \sim 0$ (off state), the absolute charge density $|Q_S|$ of the nanowire channel surface is just about double that of the reference device, but at a higher gate voltage of $V_G \sim 10$ V, which turns the device to the on state, the $|Q_S|$ of the nanowire channel surface is several hundred times that of reference device, which indicates a more than approximately two order of magnitude enhancement. This suggests that the increase in the on-state Q_S may possibly causes the improved on/off current ratio (I_{ON}/I_{OFF}) of the NW devices. On the other hand, the increase in the off-state Q_S is a factor that may degrade the on/off current ratio, I_{ON}/I_{OFF}, in the SiNW relative to that in the reference FET because the increase in the off-state charge would contribute to the off-state current (I_{OFF}). However, the difference in the values of the off-state Q_S between the two devices is marginal (∼ about 2 times) compared to the ∼2 order of magnitude difference for the on-state and it is not clear whether the charges generated at off-bias would contribute to the conduction current.

Figure 3 shows the electron concentration distribution in each silicon channel of the 2D structures at $V_G \sim 10$ V. At $V_G \sim 10$ V (on-state), about a 100 times higher inversion carrier concentration is observed in the SiNWFET than in the reference FET, which can contribute to the conduction current in the SiNW, as shown in Figure 3(b). The inversion carriers exist in the corner of

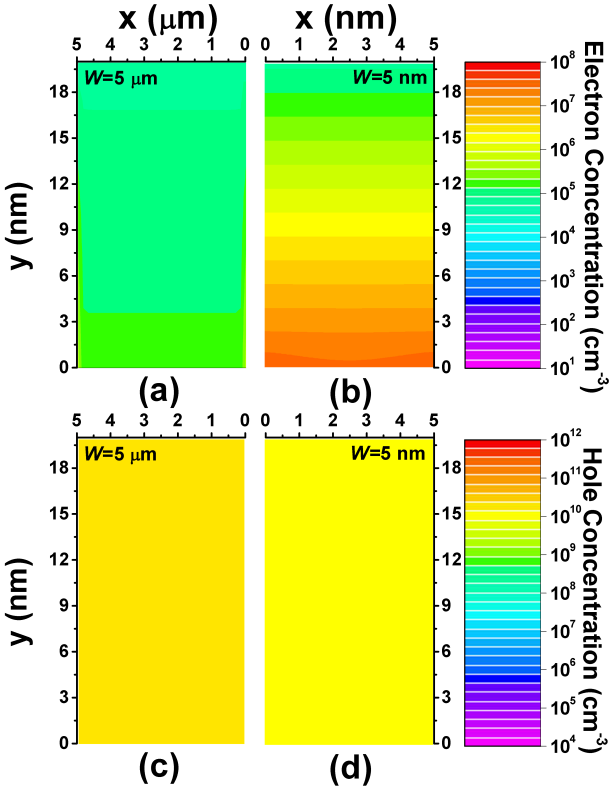

Fig. 4. Electron concentration distributions at the off-state ($V_G \sim 0$ V) in the channels of the (a) reference and the (b) SiNW devices. The hole concentration distribution at the off-state ($V_G \sim 0$ V) in the (c) reference and the (d) SiNW devices. (Not drawn to scale. Note the difference in the X-axis scale.)

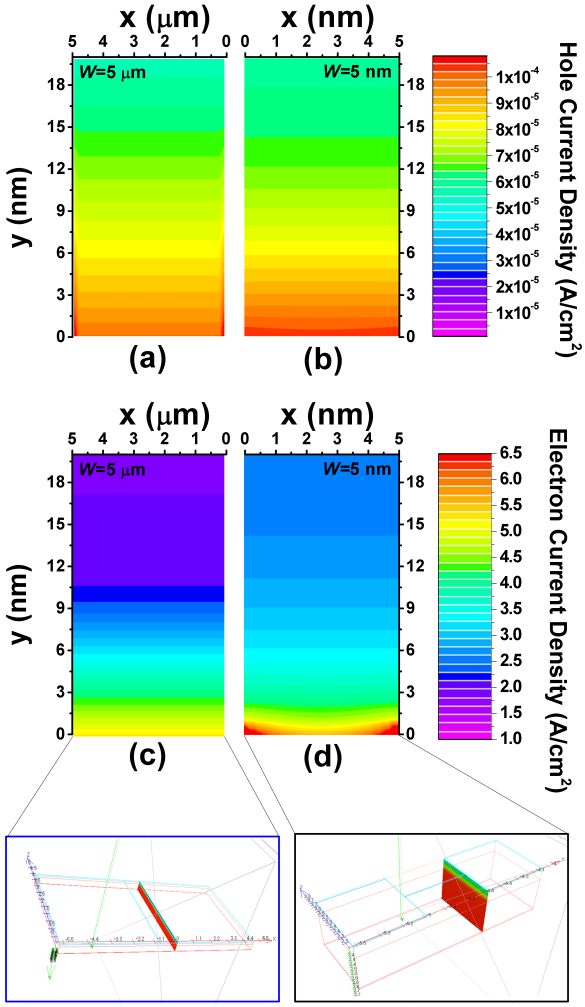

Fig. 5. Hole current distribution in the drain-side channel cross-sections of the (a) reference FET and the (b) SiNWFET at off-state ($V_G = 0$ V). The electron current distribution in the drain-side cross-section of the (c) reference FET and the (d) SiNWFET at on-state ($V_G \sim 10$ V). (Not drawn to scale. Note the difference in the X-axis scale.)

the channel rather than in the center of the channel due to the so-called corner effect [12], which also affects the center of the channel surface in the SiNW device. On the other hand, the center of the channel surface in the reference device is not affected by the corner effect due to the relatively long distance of ~2.5 μm from the corner, as opposed to the short distance ~0.25 nm from the corner in the SiNW device. After all, the inversion carrier density in the SiNW device's channel is found to be about ~100 times that in the reference device's channel as is also shown at the on-bias point $V_G \sim 10$ V of Figure 2, where the inversion carrier densities in the SiNW and the reference device are ~1.33 $\times$ 10^{-6} cm^{-2} and ~1.39 $\times$ 10^{-8} cm^{-2}, respectively.

Figure 4 shows the electron and the hole concentration distributions in each silicon channel of the 2-D structures at $V_G \sim 0$ V. The electron concentration density is only about in ~10^6 to 10^7, but the hole concentration density is ~10^{13} in both devices. This means that the dominant carriers, which contribute to the conduction current, are holes at zero bias. On the other hand, the surface charges Q_S, as shown in Figures 2, 4(a) and (b), can be considered as space charges, which are created mainly due to the fixed ionized acceptor atoms(*i.e.* the depletion mode)

[13]. In order to study this effect in further detail, we performed an additional simulation including 3-D device structures. The cross-sectional images of the drain-side channel are shown in Figure 5. These images show the current density distributions in the channel for both on- and off-bias conditions. As shown in Figures 5(a) and (b), the dominant current (@ $V_G \sim 0$ V and $V_D \sim 1$ V) was hole conduction and the hole current density stayed almost the same.

At zero bias, almost the same hole concentration density and the same uniform distribution were observed, as shown in both Figures 4(c) and (d), whereas most holes distribute on the bottom of the channel for 3-D simulations, as shown in Figures 5(a) and (b). This discrepancy is caused by the structural difference in simulations between the 2-D and 3-D structures; namely, the 3-D

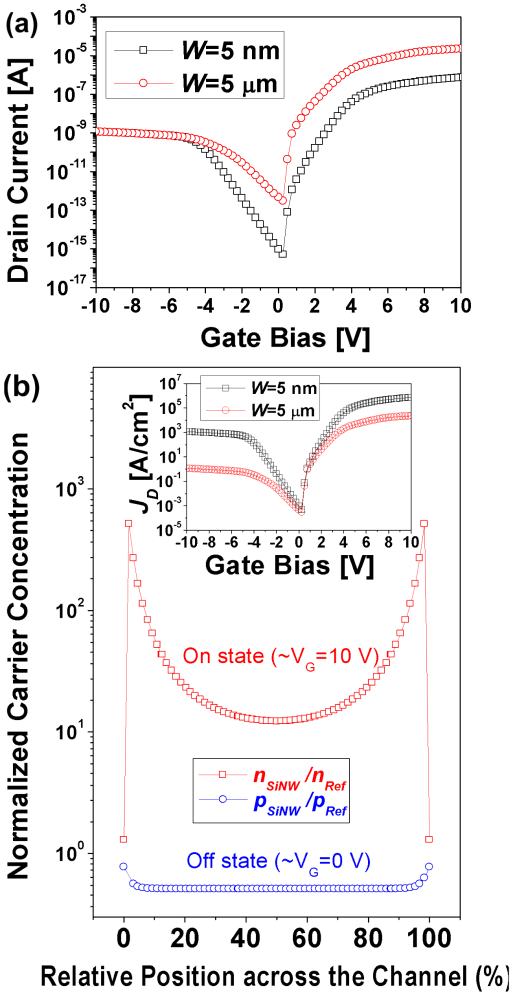

Fig. 6. (a) Gate transfer characteristics of the SiNWFET and the reference FET (@ V_D=1 V). (b) Normalized carrier concentration in the channel of the SiNW device with respect to the reference device in both the on- and the off-states. The inset represents current density (J) as a function of the gate bias for the SiNWFET and the reference FET.

structure has a drain electrode and the drain bias causes the holes to distribute in the bottom of the channel and causes an additional slight corner effect due to the drain. However, the hole concentrations for both the SiNWFET and the reference FET channels are almost the same in both the 2-D and the 3-D simulations, which can be verified in Figures 6(a) and (b) at zero gate bias.

As shown in Figures 5(c) and (d), a marked increase was observed in the on-current density in the SiNWFET. This can be identified by the gate characteristics of the two devices (see Figure 6). The 'off current' levels of the SiNWFET and the reference FET are $\sim 5.03 \times 10^{-16}$ A and $\sim 3.01 \times 10^{-13}$ A, respectively. The 'on-current' levels of the two devices are $\sim 7.36 \times 10^{-7}$ A and $\sim 2.26 \times 10^{-5}$ A, respectively. These values, considering the dimensions of the channel's cross-sectional area for the two different devices (5 × 20 nm and 5 μm × 20 nm), correspond to the current density, educed that the 'off-current' densities of the two devices are $\sim 5.04 \times 10^{-4}$ A/cm^2 and $\sim 3.01 \times 10^{-4}$ A/cm^2, respectively and the 'on-current' densities of the two devices are $\sim 7.36 \times 10^{5}$ A/cm^2 and $\sim 2.26 \times 10^{4}$ A/cm^2, respectively, as shown in the inset of Figure 6(b). We have also inspected normalized carrier concentration in the channel of the SiNW device with respect to the reference device as a verification to support these results. As can be seen in Figure 6(b), in the on-state the electron concentration of the SiNW device is observed to be about 600 times higher near both corners and 10 times higher at the center of the channel than that of the reference device. On the other hand, in the off-state the ratio is about 1 over the entire range. These results are in good agreement with our interpretations and are supported by recent experimental reports. After all, the on/off current ratios (I_{ON}/I_{OFF}) of the SiNWFET and the reference FET were shown to be about $\sim 1.46 \times 10^{9}$ and $\sim 7.5 \times 10^{7}$, respectively. Consequently, the SiNWFET results in more than two order of magnitude improvement in the on/off current ratio.

III. CONCLUSION

In conclusion, we have studied the enhanced on/off ratio in SiNWFETs by using 2-D and 3-D numerical simulations. The on/off current ratios for the SiNW and the reference FETs have been examined by separating two bias states, the on-state and off-state. Although in the 2-D simulation results of the 'off-state' it is not clear whether the charges at zero bias contribute to the conduction current, it has been confirmed that the charges in the SiNWFET channel surface in the 'on-state' are conduction carriers and with a concentration about 100 times higher than those in the reference FET channel. We have shown that this tremendous increase, which is two orders of magnitude improvement, of charges in the SiNWFET channel surface in the 'on-state' is ascribed to the corner effect and results in an increase in the on/off current ratio. The uncertainty in the 'off-state' conduction of the two different device structures in the 2-D simulation results was studied in more detail by using a 3-D simulation, which revealed that the dominant current at zero gate bias was hole conduction and that most charges generated at zero bias were space charges caused by fixed ionized acceptor atoms. The 'on-current' of SiNWFETs has been clearly shown to be significantly increases compared with that of reference the FETs, resulting in more than about a two order of magnitude improvement in the on/off current ratio.

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