Performance Analysis of 10 kV, 100 A SiC Half-Bridge Power Modules †

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Abstract: *The DARPA Wide Bandgap Semiconductor Technology (WBGS) High Power Electronics (HPE) Phase II program is developing high-voltage, high-frequency SiC device and package technology needed to meet the specific program objectives for a 13.8 kV, 2.75 MVA Solid State Power Substation (SSPS) being developed by the DARPA WBGS-HPE Phase III program. In this paper, the performance of the HPE Phase II SiC device and package technology is evaluated and a physics-based electro-thermal model is used to investigate the design trade-offs for 100 A, 10 kV SiC half-bridge power modules. This electro-thermal model is also used to demonstrate the expected performance of the half-bridge modules in a representative HPE Phase III SSPS topology.*

Keywords: Silicon carbide; power semiconductor; high-voltage; MOSFET; Junction Barrier Schottky (JBS); half-bridge power module; Solid State Power Substation.

Introduction

The Defense Advanced Research Projects Agency (DARPA) has made a significant investment to accelerate the development and application insertion of the high-voltage, high-frequency (HV-HF) SiC power devices necessary for improving military and industrial electrical power systems [1]. The goal of the DARPA Wide Bandgap Semiconductor Technology (WBGS) High Power Electronics (HPE) Phase II program is to develop 100 A, 10 kV, 20 kHz SiC power modules required to demonstrate the 13.8 kV, 2.75 MVA Solid State Power Substation (SSPS) in DARPA WBGS-HPE Phase III.

The new 10 kV SiC device technology developed in the WBGS-HPE Phase II program includes PiN diodes, Junction Barrier Schottky (JBS) diodes, MOSFETs, and Insulated Gate Bipolar Transistors (IGBTs). The MOSFETs and JBS diodes currently provide the best switching speed performance among these devices. The majority carrier type devices (MOSFETs and JBS diodes) also demonstrate excellent safe operating area (SOA) and expected long-term reliability. Although substantial progress has also been made in increasing the switching speed and eliminating the forward bias degradation of the minority carrier SiC device types (PiN diodes and IGBTs), the 10 kV SiC MOSFETs and JBS diodes are currently considered to be the most suitable candidates for the HPE Phase III power modules.

Substantial progress has also been made in developing package technology necessary for 10 kV, 100 A, 20 kHz power modules including the topology for the half-bridge with anti-parallel diodes, the 15 kV direct-bonded-copper (DBC) voltage isolation, the integrated liquid-cooled baseplate, and the high-voltage low-inductance electrical interconnects and potting compounds. Current efforts of the HPE program involve optimization and system integration of the SiC device and package technologies developed in Phase II to meet the specific requirements of the SSPS.

The purpose of this paper is to evaluate the performance of the HPE Phase II SiC device and package technology and to use physics-based electro-thermal circuit simulator models to investigate the design trade-offs for the 100 A, 10 kV SiC half-bridge power modules. The electro-thermal model for the half-bridge power module is also used to demonstrate the expected performance in a representative SSPS topology.

SiC MOSFET

Fig. 1 compares the simulated and measured output characteristics of an HPE Phase II 10 kV SiC MOSFET [2] area-scaled to 3.09 cm^2 for a) 25 ºC and b) 125 ºC. The SiC MOSFETs have achieved positive threshold voltage up to 200 ºC, resulting in low leakage at high temperature and high drain voltage [1]. The SiC MOSFETs have also achieved a high transconductance parameter (K_P) providing nearly 100 A/cm^2 peak current density capability at 25 ºC for a gate voltage below that corresponding to the maximum reliable gate oxide field (20 V for the devices discussed in this paper). The high transconductance of the MOSFETs along with the low specific on-resistance of the 10 kV voltage blocking layer provide nearly 30 A/cm^2 continuous current capability at 125 ºC for a 250 W/cm^2 package cooling capability.

The HPE Phase II MOSFETs are generally suitable for 20 kHz hard switching applications [3] where the required gate resistance scales inversely proportional with die area at approximately 0.5 Ω for the 3.09 cm^2 die area. Fig. 2 compares the simulated and measured inductive load turn-off waveforms of the 3.09 cm^2 area-scaled MOSFET for two different currents. In general, the turn-off switching speed is faster for the higher current density. However, the

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turn-on switching speed is also limited by the peak current density needed to provide the additional current (above the load current) to rapidly charge the output capacitance of both SiC MOSFETs and both SiC JBS diodes within the half-bridge module.

JBS Diode

Fig. 3 compares the simulated and measured forward conduction characteristics of an HPE Phase II 10 kV JBS diode [4] area-scaled to 5.0 cm^2 for junction temperatures from 25 ºC to 165 ºC. The low specific on-resistance of the 10 kV voltage blocking layer provides nearly 30 A/cm^2 continuous current capability at 125 ºC for a 250 W/cm^2 package cooling capability. The maximum on-state voltage at the peak current and high temperature is also an important parameter indicating the level of stress on other components in the half-bridge power module as discussed below (note the indicated value of V_{ON_MAX} = 20 V at 165 ºC and 40 A/cm^2).

Fig. 4 compares the reverse recovery characteristics of the HPE Phase II 10 kV JBS diode area-scaled to 5.0 cm^2 for different circuit-imposed dI/dt conditions. The diode reverse recovery charge (area under negative portion of the current waveform) is determined by the diode junction capacitance, which is proportional to the JBS diode area. Although reducing the JBS diode area increases the on-state loss of the diode, it may also result in a substantial reduction in MOSFET switching loss as described below.

Half-Bridge Module Model

Fig. 5 is an example circuit topology for the 10 kV, 100 A SiC half-bridge power module indicating the 10 kV SiC MOSFET switches (SiC_MOS), the 10 kV SiC JBS anti-parallel diodes (SiC_JBS), and the reverse blocking silicon Schottky diodes (Si_Sch). The reverse blocking diodes are used to prevent reverse conduction in the SiC MOSFETs during conduction of the anti-parallel diodes. The breakdown voltage of the reverse blocking diodes must be larger than the maximum on-state voltage of the anti-parallel SiC JBS diodes (V_{ON_MAX} of Fig. 3) and must have sufficient avalanche energy capability to conduct in the reverse direction during switching events.

Fig. 5 also indicates the thermal network component models representing heat transport within the module semiconductor devices, voltage isolation DBC layers, and integrated liquid-cooled baseplate [5]. Fig. 6 compares the simulated and measured junction temperature during a power cycle experiment. The measurements are made using both temperature sensitive parameters and infrared methods for a wide range of dissipated power levels and pulse widths. The electro-thermal model for the 100 A, 10 kV SiC half-bridge power module is discussed in detail in [6] and includes the 10 kV SiC power MOSFET model [3] and the 10 kV SiC JBS diode model [7]. The electrical interconnect parasitic inductances and capacitances are also being characterized, simulated, and optimized for the HPE Phase III module but are not shown in Fig. 5 for clarity.

Module Design Trade-offs

Table 1 summarizes the results of a 100 A, 10 kV half-bridge module design trade-off study [6]. The results are obtained using a circuit that emulates the conditions of a hard-switched inverter with a 5 kV bus and a continuous current of 100 A. These simulations assume that the coolant flow rate is sufficient to keep the baseplate bottom temperature at 25 ºC. Fig. 7 gives an example of the simulated temperature waveforms for the lower SiC MOSFET in the half-bridge module for Case 5 in Table 1.

As a baseline, Case 1 uses the MOSFET active area = 3.09 cm^2 and the JBS area = 5.0 cm^2 as in Figs. 1 through 4 with R_G = 0.5 Ω. Making the SiC MOSFET larger than the baseline reduces the losses slightly and reduces the MOSFET temperatures but requires the gate resistance to be scaled inversely proportional to the MOSFET area (see Cases 2 and 3). Making the SiC JBS diode smaller than the baseline reduces the losses and decreases the MOSFET temperature (see Cases 4 and 5). Further reduction of diode area does not reduce loss substantially and increases V_{ON_MAX} of the SiC JBS diode, thus increasing the voltage blocking requirement of the series blocking diode.

SSPS Simulation Results and Conclusions

Fig. 8 shows an example circuit that can be used as a building block to implement an SSPS. For example, to handle a 13.8 kV-rms AC primary voltage, four of these blocks can be connected in series at the primary for each phase. This would result in each block handling a nominal 5 kV operating DC bus voltage with the 10 kV SiC bridges. The outputs of the four blocks can be connected in parallel to provide the low voltage SSPS output. This configuration would require twelve blocks to implement a three-phase 2.75 MVA, 13.8 kV to 465 V SSPS.

The SSPS building block of Fig. 8 consists of several stages: 1) a front-end rectifier which converts the input 60 Hz AC into a nominally 5 kV MV-DC bus 2) a high frequency link (using 10 kV SiC half-bridge modules, a nano-crystalline core HF transformer, and a low-voltage rectifier bridge) that steps down the voltage, and 3) a low-voltage inverter bridge that creates the 60 Hz AC output.

Fig. 9 shows electro-thermal simulations for the circuit of Fig. 8 and a module configuration similar to Case 5 of Table 1. The simulations are for the worst case coolant temperature of 80 ºC. In this case the MOSFET junction temperature reaches about 100 ºC at rated load and 0.8 power factor lagging. This represents enough margin in the SiC modules to handle transient overloads or fault conditions and represents an acceptable temperature cycle for step load changes.

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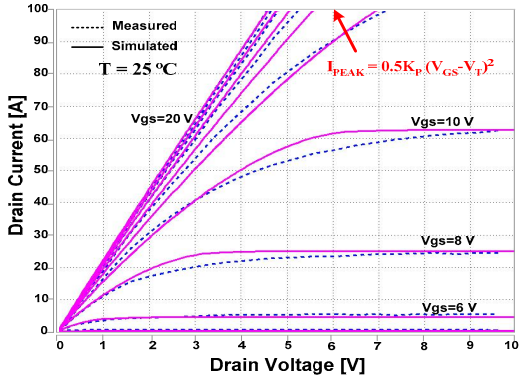
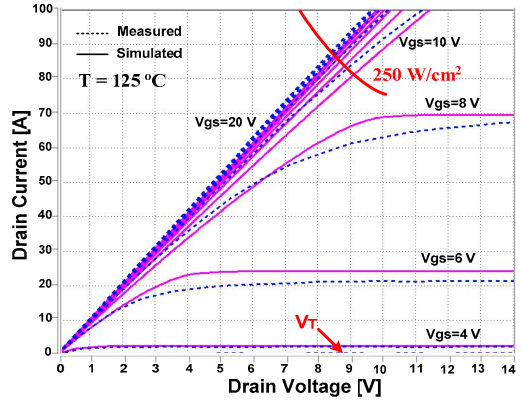


(a)



(b)

Fig. 1: Comparison of scaled measured (dashed) and simulated (solid) output characteristics at 25 ºC (a) and at 125 ºC (b) for a 100 A, 10 kV SiC power MOSFET.

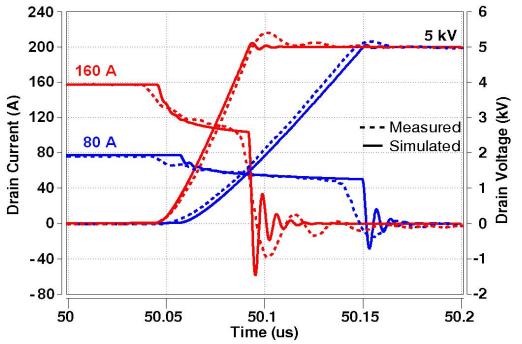


Fig. 2: Comparison of scaled measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms at 25 ºC for a clamp voltage of 5 kV and a 100 A, 10 kV SiC power MOSFET.

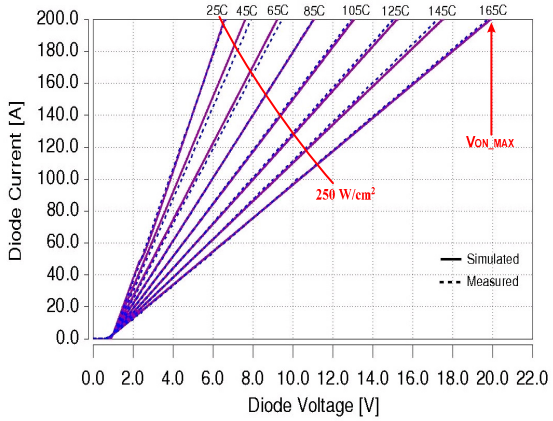


Fig. 3: Comparison of scaled measured (dashed) and simulated (solid) forward conduction characteristics at 25 ºC, 45 ºC, 65 ºC, 85 ºC, 105 ºC, 125 ºC, 145 ºC, and 165 ºC for a 100 A, 10 kV SiC JBS diode.

Table 1: Power and Energy Calculations for 10 kV SiC MOSFET/JBS Module

Case #	*Total*	MOSFET					JBS Diode				
	P [W]	P_{MOS} [W]	$E_{ON-STATE}$ [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,MOS}$ [º C]	P_{JBS} [W]	E_{COND} [J]	$E_{SW,ON}$ [J]	$E_{SW,OFF}$ [J]	$T_{PEAK,JBS}$ [º C]
1	801	721	0.019	0.056	0.005	71.15	80	0.0094	0.0077	0.0077	28.17
2	859	773	0.011	0.065	0.007	55.41	86	0.0101	0.0077	0.0077	28.25
3	780	695	0.011	0.057	0.007	54.87	85	0.0099	0.0077	0.0077	28.23
4	713	600	0.018	0.044	0.005	67.47	113	0.0133	0.0046	0.0048	32.51
5	694	533	0.018	0.037	0.005	61.30	161	0.0188	0.0030	0.0031	39.52
6	1055	933	0.021	0.072	0.010	77.31	122	0.0142	0.0047	0.0047	32.60

Case 1: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω. (baseline)
Case 2: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 5.00 cm^2, R_G = 0.5 Ω.
Case 3: A_{JBS} = 5.00 cm^2, A_{MOSFET} = 5.00 cm^2, R_G = 0.309 Ω
Case 4: A_{JBS} = 3.09 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω.
Case 5: A_{JBS} = 2.00 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 0.5 Ω. (Optimized)
Case 6: A_{JBS} = 3.09 cm^2, A_{MOSFET} = 3.09 cm^2, R_G = 2.0 Ω.

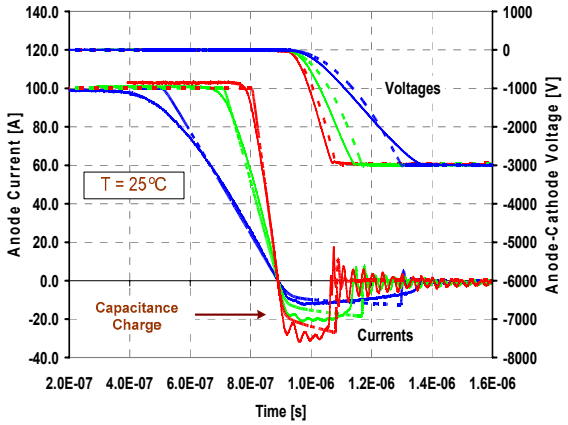


Fig. 4: Comparison of scaled measured (solid) and simulated (dashed) reverse recovery characteristics at 25 °C for a 100 A, 10 kV SiC JBS diode.

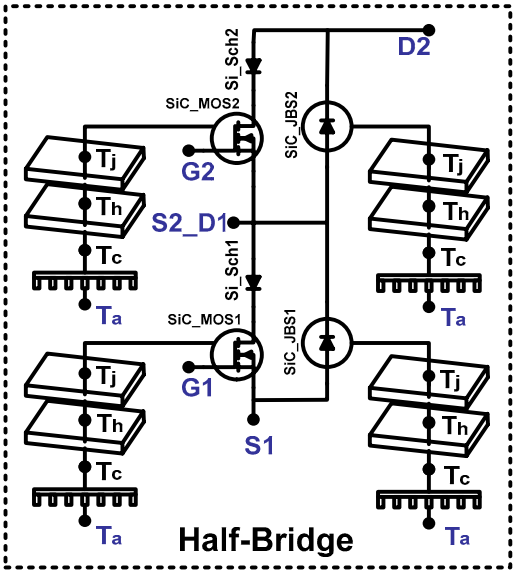


Fig. 5: Circuit topology of the half-bridge SiC MOSFET/JBS power module with low-voltage series diodes to prevent reverse conduction in the MOSFETs. The thermal network component models representing heat transport within the module are also indicated.

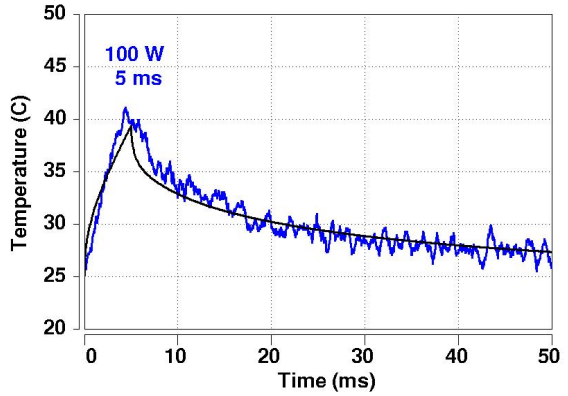


Fig. 6: Measured (blue) versus simulated (black) SiC MOSFET junction temperature for a 100 W, 5 ms chip dissipated power pulse (A_{MOSFET} = 0.1545 cm^2).

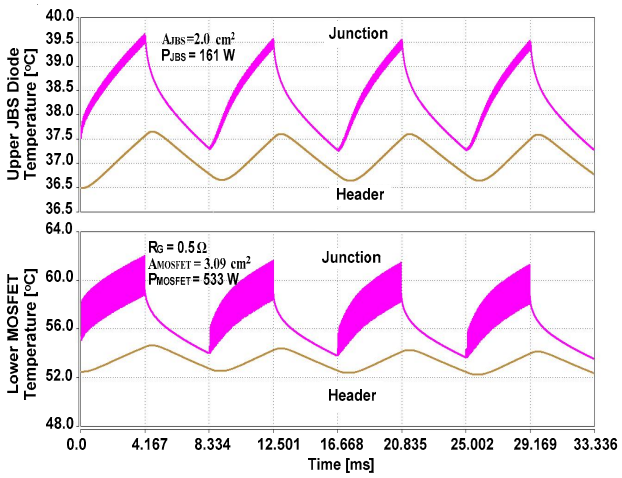


Fig. 7: Temperature waveforms for lower SiC MOSFET with R_G=0.5 Ω and A_{MOSFET} = 3.09 cm^2 and the upper SiC JBS diode with A_{JBS} = 2.0 cm^2 in the 100 A, 10 kV half-bridge power module.

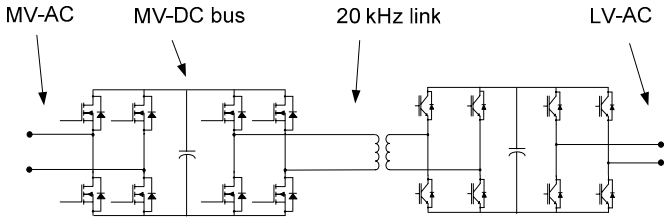


Fig. 8: Example of a building block circuit for an SSPS. This building block converts medium voltage AC (MV-AC) at the primary (PRI) to low voltage AC (LV-AC) at the secondary (SEC).

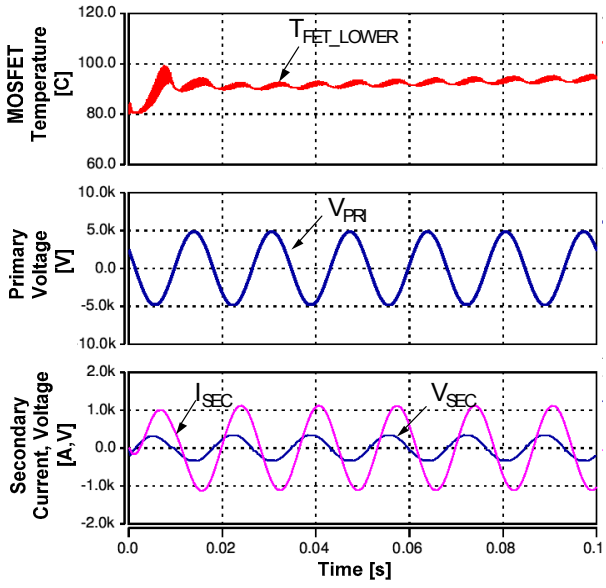


Fig. 9: Simulated waveforms for the circuit of Fig. 8 with an optimized module configuration similar to Case 5 of Table 1.