DESIGN OF A TURN-KEY 10 V PROGRAMMABLE JOSEPHSON VOLTAGE STANDARD SYSTEM

P.D. Dresselhaus, M. Elsbury[1], C.J. Burroughs, D. Olaya, S.P. Benz, N.F. Bergren, R. Schwall, and Z. Popovic[1]

National Institute of Standards and Technology, Boulder, CO, USA
[1]College of Engineering and Applied Science, University of Colorado, Boulder, CO, USA

Abstract

NIST is designing a 10 V Programmable Josephson Voltage Standard (PJVS) system with an improved microwave design and arrays of stacked Nb_XSi_{1-x}-barrier Josephson junctions. For this new design a "ground-up" approach was used that takes into account all system issues in order to produce a robust 10 V system. By improving the uniformity of the microwave drive along the length of each array, constant-voltage steps with a larger current range are generated allowing the use of smaller critical current junctions. Smaller critical currents are important for lowering the total overall power dissipated on chip. Reducing power dissipation also increases the operating margins. Thus, all aspects of the design are interrelated and important for an optimized system.

Introduction

Voltage standards made with conventional superconductor-insulator-superconductor (SIS) junctions have existed for many years [1-2], and more recently, PJVS 10 V systems have been fielded by PTB [3] and AIST [4]. The AIST PJVS circuit uses a 16 GHz microwave bias and 327 680 double-stacked NbN-$NbTi_x$-NbN junctions. These normal-metal-barrier (SNS) junctions have the advantage of working at 10 K on a cryocooler. The PTB 10 V PJVS system is based on 69 120 SINIS junctions running at 70 GHz, which is compatible with conventional JVS microwave electronics. Unfortunately, both of these systems have been plagued by chips with low device yield and small operating current margins, typically less than 1 mA.

In order to ensure noise immunity and robust operation, an easy-to-use, turnkey system should have large operating margins greater than 1 mA and high device yield. In pursuit of this goal, NIST has taken the stacked junction, filtered bias taps, and tapered transmission lines that were developed for the ac Josephson Voltage Standard system and applied them to a 10 V PJVS system design [5]. This "ground-up" approach also includes a complete redesign of every microwave component, including microwave dividers, bias taps, terminations, and transmission lines.

System Design

The schematic system design is shown in Fig. 1. A computer will control the overall system with simple commands to simplify the software and usability. The control electronics will have the bulk of the complexity, because it will interface with the computer and store information about the PJVS circuit, including information to control each array at the specified operating point. For simplicity, the initial circuit will be designed to produce only a small number of voltages to increase yield and avoid fine subdivision of the arrays.

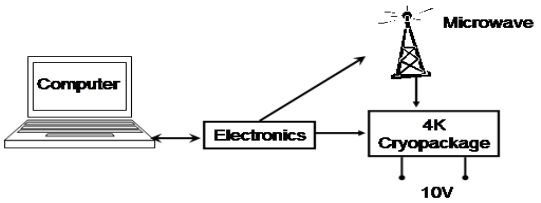

Fig. 1. 10V Turnkey system design. The computer interface will send and receive simple commands via a standard interface.

Packaging

Because users of voltage standards currently work at 4 K, the system is designed to work either in liquid helium or on a 4 K cryocooler. An operating frequency in the range 15 GHz to 25 GHz has been chosen, so as to be compatible with low-cost microwave sources and amplifiers. This leads to a junction count N of at least 200,000 junctions in order to reach 10 V. The amount of heat that needs to be dissipated in the circuit determines the thermal packaging requirements. This heat load is of the order 10 V * I_c, where I_c is the junction critical current. As a trade-off between increasing the thermal load and decreasing the operating margins, critical currents of 6 mA will be used for the junctions, which is about half that of our previous designs. This should reduce the heat load to approximately 100 mW, which has recently been demonstrated for 5 V PJVS chips on the cold stage of a cryocooler.

Because the standard NIST 1 cm x 1 cm chip size is too small to contain the large number of junctions, a chip size of 17 mm x 12 mm, has been chosen (which is also the maximum field size of our i-line stepper). The larger size will also increase the heat flow out of the substrate. Heat-sinking of the backside of the chip to a copper plate is accomplished with indium foil and applied pressure.

Josephson Junctions

Recent advances in Josephson junction technology at NIST have led to a focus on amorphous Nb_xSi_{1-x}-barrier junctions with Nb superconducting electrodes. These junctions have the dual advantages of (1) using the Nb content x of the barrier to tune the junctions from SIS behavior (small x) to SNS behavior (x ~0.12); and (2) having a well-defined process to fabricate stacks of three (or higher) junctions, which increases the junction count without increasing the chip size. Unfortunately, our operating margins currently decrease for stacks taller than three junctions, but we are working to understand this issue.

Having chosen the critical current to be 6 mA, the remaining junction parameter is the normal-state junction resistance R_n which also sets the characteristic frequency of the system, $f_c = I_c R_n K_J$, where K_J is the Josephson constant. There is a trade-off in choosing R_n between increasing f_c, and thus the voltage per junction, and increasing the dissipation of the array. Dissipation limits the number of junctions per array to $N_z \approx Z_0/R_n$, where Z_0 is the characteristic impedance of the transmission line.

Small values of R_n allow more junctions per array, but also lead to a smaller characteristic frequency f_c. Unfortunately the lower f_c leads to a lower optimal drive frequency and thus a lower voltage from the array[6]. To match our microwave source, $R_n \approx 5$ mΩ is used for $f_c \approx$ 15 GHz.

Microwave designs

The most novel aspect of this 10 V PJVS design is the improved microwave circuit components. The components that have been optimized include the launch onto the chip, microwave power splitters, impedance transformers, and tapered transmission lines. Microwave simulations with Ansoft HFSS [7] of these circuit elements compared favorably with measurements performed with a commercial network analyzer. For on-chip structures, a custom set of thru-reflect-line (TRL) calibration standards was fabricated to account for the microwave characteristics of the measurement system, including the probe.

Both the microwave launch onto the chip and the transition from the coaxial cable to the chip package (both the spring-fingers for testing and the flexible board for final packaging) were optimized. All extraneous metal was minimized in the launches (such as solder from the connectors) in order to reduce parasitic capacitance. Coplanar transmission lines on the packaging interface were found to be superior to microstrip lines because they better matched the coaxial feed-line with the on-chip coplanar geometry without incurring additional parasitic effects from through-substrate vias. The launch onto the chip reduces the 150 μm gap from the package down to the on-chip 7 μm gap used for 50 Ω transmission lines. It was found that a short linear taper, rather than a logarithmic taper, was sufficient.

Following the on-chip taper, the microwave power is split 16 ways with a binary tree of 180° hybrid and Wilkinson power dividers. A block diagram of the microwave chip design is presented in Fig. 2. The hybrid splitters use lumped-element phase shifters to simulate a cavity where the 180° port is driven. Both the 90º and 270º ports were used for in-phase power division, while the 0° isolated port is loaded [8]. The Wilkinson splitter uses two lumped-element quarter-wave sections with Butterworth-tuned impedances to split and match the input signal into two in-phase outputs [9]. The hybrid splitter has the advantage of not dissipating out-of-phase reflected power, whereas the Wilkinson splitter has broader low-end bandwidth and less sensitivity to the phase of downstream reflections. The present design uses hybrid splitters for the first three stages of microwave power division and the more compact Wilkinson splitter for the final stage. The Wilkinson is also designed to impedance transform the 50 Ω feed line to the 86 Ω transmission line feeding the Josephson array.

Rather than a standard transmission line, the Josephson array is distributed along a tapered transmission line. Tapering partially compensates for the microwave power attenuation caused by junction dissipation. By decreasing the impedance of the line, the ratio between microwave voltage and current is continuously changed to maintain a constant current range for the Josephson voltage steps. Tapering the transmission line thus allows more junctions to be distributed in each array, so that a single array produces larger voltages without significantly reducing operating margins.

This optimized microwave design also reduces the overall power required from a room-temperature amplifier to less than 1 W, which fulfills the goal of a low-cost, easy-to-use system.

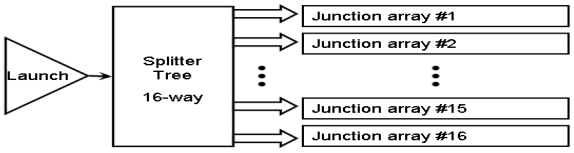

Fig. 2. On-chip microwave schematic for the NIST 10V PJVS. The microwave signal is divided 16 ways with a binary network of splitters and isolators. Each array is driven in parallel by the microwaves and connected in series for the dc output voltage (not shown).

The arrays are series connected through superconducting taps that use low-pass inductive filters. These filters are not part of the microwave path and allow dc bias currents to be applied and dc voltages to be measured. Because the taps are superconducting, no voltage errors arise from bias currents.

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[7] This commercial instrument is identified in this paper only in order to adequately specify the experimental procedure. Such identification implies no recommendation or endorsement by the National Institute of Standards and Technology, nor that the equipment identified are necessarily the best available for the purpose.

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