

SYSTEMATIC ERROR ANALYSIS OF STEPWISE APPROXIMATED AC WAVEFORMS GENERATED BY A PROGRAMMABLE JOSEPHSON VOLTAGE STANDARD

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Abstract

We have measured stepwise-approximated sinewaves generated by a Programmable Josephson Voltage Standard with several different output configurations. These data are analyzed to characterize the dominant error mechanisms for rms applications, such as ac-dc difference measurements of a thermal voltage converter (TVC). We discuss the impact of the dominant systematic errors on the overall uncertainty and consider the implications of providing the load current required by low input impedance devices such as TVC's.

Introduction

Since the introduction of series arrays of intrinsically shunted Josephson junctions in the mid 1990's [1-3], Programmable Josephson Voltage Standards (PJVS) have been used to generate stepwise-approximated waveforms for a number of ac metrology applications including ac-dc difference measurements at frequencies up to 1 kHz [4, 5], fast reversed dc (FRDC) measurements of thermal voltage converters [6, 7], and, more recently, impedance and power metrology [8-10]. The advantage that PJVS systems have over other sources in these applications is that the generated waveforms are constructed with quantum-accurate voltages from an intrinsic Josephson voltage standard. This approach offers the promise of a fundamentally accurate ac and dc voltage source with precisely calculable rms amplitudes and spectral content.

This stepwise-synthesis method has an important limitation, however, because the output voltage from the PJVS is not precisely known during the transitions between the quantized voltages. More importantly, the generated rms voltage depends on the exact timing of the transitions, as we recently described in detail in [11]. The transition timing is affected by (1) the *chosen* values for bias-current set-points, (2) any deviations in the *actual* bias currents from those target values, and (3) the precise shape of the Josephson current-voltage characteristic of each Josephson array.

To quickly illustrate this effect, in Fig. 1 we show a simple 1 V zero-to-peak square wave that has only two transitions per period. For a 1 kHz frequency, a +0.5 mA shift in the bias set-point causes the transition edges to move apart by 2 ns, which results in a large 2 μ V/V increase in the rms voltage [11]. Even tiny bias-current changes, on the order of tenths of a milliamp, produce timing shifts of hundreds of picoseconds (in opposite directions) for the rising and falling waveform edges. Such shifts may seem insignificant, but they directly impact the rms voltage accuracy of the PJVS waveform, especially for frequencies above 500 Hz. The dependence of transition timing on bias-current set-point is an inherent systematic error for stepwise synthesis, and we have to consider its impact in all measurements because the

specific bias currents that would yield the “correct” target rms voltage cannot be predetermined. Fortunately, at low frequencies (such as 60 Hz for power applications) the error is small enough that we can reach our uncertainty objectives by determining upper and lower bounds for the error, and including it as a Type B uncertainty. At higher frequencies, reasonably low uncertainties will be achieved only by calculating and correcting for the error through careful modeling of the PJVS current-voltage transitions and the timing.

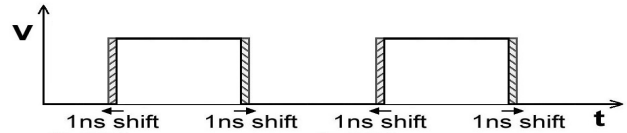


Figure 1. Diagram illustrating the shift in transition edges for a 1 V square wave. Moving the current set-point on the positive step +0.5 mA produces a timing shift of 1 ns in opposite directions on both transitions.

PJVS Output Configurations

The operational details of the PJVS have been extensively documented [12], so in this paper we will describe three methods of interfacing the output of the PJVS chip to measurement devices. These measurement configurations differ from each other in the magnitude of the error mechanisms affecting the voltage accuracy and the overall uncertainty. However, the method for evaluating potential errors is the same in each case: we vary each relevant system parameter and determine its effect on the output voltage (as in the example in Fig. 1).

In the simplest “A” configuration, the PJVS output leads are connected directly to a high-impedance measurement instrument, such as the buffer amplifier of a TVC or digital voltmeter. This has the advantage that no significant current flows in the output leads, and there is negligible voltage drop due to the output lead resistance. The disadvantage is that the output is not properly terminated, so the measured voltages, following the transitions, include some ringing which must be considered in the uncertainty analysis.

In an alternative “B” configuration, we connect the PJVS to an instrument with a relatively low input impedance (50 Ω to 200 Ω) and provide the required load current with a synchronized commercial room-temperature source. This method allows the PJVS output to be terminated by its characteristic impedance with little ringing. However, this configuration is challenging because the current-assisting source must set the voltage across the load to exactly match the PJVS voltage to better than 1 μ V to ensure that minimal current flows between the two sources. Otherwise, a voltage drop occurs across the output lead resistance, which results in a systematic error. It is difficult to ensure that this error is less than a few parts in 10^7 . This approach was used in the early days of PJVS synthesis for FRDC measurements of TVC's.

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Another, “C” configuration, that we explored during our FRDC work connects the PJVS output cable directly to a load, such as a 50 Ω TVC, and supplies the load current with the bias drivers at each end of the PJVS array. This technique has the advantage that the tolerance on the set-point for the load current is easily met, given the large current margins of SNS arrays. The penalty is that the reference plane is at the chip output pads, and the voltage drop across the output lead resistance is significant. Fortunately, this effect is both measurable and correctable for both ac and dc voltages.

Transition Considerations

The most problematic sources of systematic error for PJVS stepwise synthesis relate to the transitions between the quantized voltages. The obvious remedy is to build faster and jitter-free bias electronics so that the transition times are short and the timing is accurate. If transitions at the PJVS output could be made on the order of a nanosecond, then we could neglect their effect for frequencies below a few kilohertz. Given the 2 m cable length between the PJVS chip and the bias electronics, such a short transition time for thirteen interdependent sub-arrays is unattainable. Even the 5 ns settling time of the present bias electronics [13] is significantly increased by interaction between the sub-arrays with such long cables. Therefore, we must carefully examine the uncertainties in the different PJVS output configurations to determine which one is best suited for a given application.

In our previous investigations of PJVS transitions [11] we used configuration A. We found that the rms output voltage dependence on the bias-current set-point shift in all cells was about 0.5 $\mu\text{V/V}$ per mA for a stepwise-synthesized 50 Hz sinewave. For comparison, we recently investigated configuration B using a commercial waveform generator to provide the load current, which required close matching of the source’s amplitude and phase to the PJVS signal. The results are summarized in Table 1, where we show that for sinewaves with 32 or more samples, we measure the same 0.5 $\mu\text{V/V}$ per mA dependence as with configuration A.

Table 1 – Measured dependence of PJVS rms output voltage as a function of bias-current shift (through all cells) for a 50 Hz stepwise-approximated sinewave with various numbers of samples. The last column indicates the resulting Type B component assuming an estimated ± 0.2 mA set-point accuracy (which we emphasize is not the *entire* Type B uncertainty introduced by this systematic error).

Number of Samples	Measured change in rms voltage as a function of offset current ($\mu\text{V/V}$ per mA)	Resulting Type B uncertainty contribution with present set-point accuracy ($\mu\text{V/V}$)
32, 64, and higher	0.52 ± 0.02	0.1
16	0.41 ± 0.02	0.08
8	0.32 ± 0.02	0.06
4	0.19 ± 0.02	0.04

The identical voltage dependence on the bias-current set-point occurs for the B configuration because, regardless of whether the PJVS transitions occur slightly before or after the auxiliary source, when the two source voltage amplitudes are not matched the resulting difference current is small enough that it flows almost entirely through the Josephson array. Thus the PJVS behaves like a short in comparison to the load, and completely determines timing of each output transition (for 32 samples or larger) instead of the current-assisting

source, and the voltage-to-bias-current dependence is exactly the same as for configuration A. As we decrease the number of samples (down to 16, 8, 4), the current that flows due to the difference between the sources exceeds the current-range of the Josephson step for longer times, which allows the current-assisting source to have more influence on the timing. This reduces the measured slope in our measurement of the rms voltage as a function of PJVS bias-current.

Conclusion

We are evaluating systematic error mechanisms in PJVS stepwise-approximated waveforms in order to develop an overall system uncertainty budget for power-metrology applications at 60 Hz. In the full version of this paper, we will present uncertainty analysis illustrating that at low frequencies (below a few hundred hertz), a total uncertainty for the ac PJVS voltages of a few parts in 10^7 can be obtained. We will also discuss the audio frequency range, where we expect significant challenges in obtaining low total uncertainties (at parts in 10^6 or better), since the effects of transition-related errors increase linearly with frequency.

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