MESFETs Made From Individual GaN Nanowires

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***Abstract*—In this paper, we demonstrate novel MESFETs based on individual GaN nanowires. The Pt/Au Schottky gates exhibited excellent two-terminal Schottky diode rectification behavior. The average effective Schottky barrier height was 0.87 eV, with an average ideality factor of 1.6. In addition, the Schottky gates efficiently modulated the conduction of the nanowires. The threshold gate voltages required for complete pinch off were as small as −2.6 V, and transconductances exceeded 1.4 μS. Subthreshold swings approaching 60 mV/decade and ON/OFF current ratios of up to 5×10^8 were achieved. These results show that the Schottky gate has the potential to significantly improve the performance of GaN nanowire field-effect devices.**

***Index Terms*—GaN, MESFETs, nanowires, Schottky barriers, Schottky diodes.**

I. Introduction

IT HAS BEEN well established that GaN is an excellent material for FET devices, particularly those requiring high-frequency, high-power operation [1]. Due to their high crystalline quality [2] and unique morphology, GaN nanowires (NWs) grown by molecular beam epitaxy (MBE) offer a promising alternative to thin films in many device applications. GaN NWs have not been yet employed as FET devices on an industrial scale. Indeed, GaN-NW-based FETs are still in the early stages of development compared to thin-film devices [1], [3]–[5]. However, the defect-free nature, high surface to volume ratio, and small dimensions of MBE-grown NWs suggest that NWs could pave the way for efficient, ultrahigh density devices in the future.

A significant volume of work on the FET behavior of GaN NWs has been carried out in the past few years [6]–[15]. However, prior work on GaN NW FETs has relied upon gating through an oxide insulator that is tens or hundreds of nanometers thick, which often results in inefficient modulation of the conducting channel of the NW.

An alternative to the oxide-based FET approach is the MESFET, which uses a Schottky barrier in place of the insulating oxide. Effective Schottky gating has previously been demonstrated in MESFETs made from single CdS nanobelts and ZnO nanorods [16], [17]. However, MESFET performance depends largely upon the quality of the Schottky barrier, and high-quality Schottky barriers have been difficult to realize for individual GaN NWs. Schottky diodes based on single GaN NWs have been reported, but these devices exhibited large deviations from ideal behavior [18]–[20].

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We report novel MESFETs based on individual GaN NWs. The Schottky gates exhibited excellent two-terminal Schottky diode rectification behavior and ideality factors significantly lower than those reported previously for individual GaN NWs. In addition, the Schottky-gated MESFETs showed low threshold voltages, high transconductances, small subthreshold swings, and large ON/OFF ratios. The MESFET design shows promise for significant improvement in the performance of GaN NW field-effect devices.

II. Device Fabrication

The NWs used in this study were c-axis, n-type, Si-doped GaN grown by catalyst-free MBE on Si (1 1 1) substrates. Details of the NW growth can be found elsewhere [21], [22]. Using typical back-gated FET measurements and calculations [15], the carrier concentration in these NWs was roughly estimated to be between 4×10^{17} and 4×10^{18} cm^{-3}. In the devices described here, the NWs were 11–19 μm in length and 210–470 nm in diameter. The approximate diameter of each NW in the gated region, as estimated from field-emission SEM (FESEM) images, is listed in Table I.

Fig. 1 shows schematic cross-sectional diagrams of the NW MESFET structure. The substrate consists of 600 nm of thermally grown SiO_2 on heavily doped p-type Si. In the first step of device fabrication, conventional photolithography was used to pattern the device substrate. A 55-nm-thick layer of Ti comprising the bottom layer of the source and drain electrodes was deposited on the patterned resist by electron-beam (e-beam) evaporation, and the extraneous metal was lifted off in acetone.

Next, the NWs were removed from their growth substrate by ultrasonic agitation in isopropanol. The NWs were then aligned across the 8-μm gaps between the source and drain electrodes by the use of dielectrophoresis. Interconnects between the source contacts and between the drain contacts of multiple devices allowed a 20-V peak-to-peak, 75-kHz sine wave to be applied simultaneously across 136 device sites on the 1 cm × 1 cm sample. During voltage application, a drop of approximately 7 μL of NW/isopropanol solution was dispensed over the device sites and allowed to evaporate. Due to the presence of the electric field, NWs aligned across the gap between the source and drain electrodes of some of the device sites. It should be noted that the dielectrophoresis parameters used here have not been optimized for device yield.

After NWs were placed on device sites, the sample was patterned for the source and drain top contacts by photolithography with microscope alignment. Prior to metal deposition, the exposed tips of the NWs on top of the source and drain Ti electrodes were subjected to a reactive ion etch (RIE) using 75-sccm O_2 at 30 W for 20 s with a chamber pressure of 20 Pa (150 mtorr).

TABLE I
MEASURED AND CALCULATED PARAMETERS FROM TEN SINGLE-NW MESFET DEVICES

device	d_{NW} (nm)	R_1 (kΩ)	R_2 (kΩ)	Φ_{Beff} (eV)	n	V_{TH} (V)	g_m (μS)	S (mV/decade)	max on/off
1	470	20.3	22.7	0.83	1.75	-15.1	2.5	--	--
2	450	22.1	27.0	0.87	1.66	-14.0	2.4	--	--
3	370	29.1	34.4	0.82	1.66	-11.6	2.2	--	--
4	360	29.5	39.0	0.87	1.52	-7.0	3.2	--	--
5	290	44.3	59.0	0.90	1.42	-3.7	2.4	75	1×10^6
6	360	47.6	63.0	0.92	1.50	-2.9	3.4	74	1×10^7
7	320	48.3	76.3	0.94	1.46	-3.2	2.3	75	2×10^7
8	310	49.3	59.3	0.72	2.04	-5.5	1.4	67	5×10^8
9	440	49.7	60.6	0.91	1.47	-7.0	1.7	--	--
10	210	94.9	151	0.93	1.53	-2.6	1.7	63	1×10^8

d_{NW} is the approximate NW diameter in the gated region, R_1 is the drain–source resistance before deposition of the Schottky gate, R_2 is the drain–source resistance after deposition of the Schottky gate, Φ_{Beff} is the effective Schottky barrier height, n is the ideality factor of the Schottky barrier, V_{TH} is the gate threshold voltage at a drain–source voltage (V_{DS}) of 1 V, g_m is the maximum transconductance at V_{DS} = 1 V, S is the subthreshold swing at V_{DS} = 1 V, and max ON/OFF is the ratio of the drain–source current (I_{DS}) at a gate–source voltage (V_{GS}) of 0 V to the minimum I_{DS} at $V_{GS} < V_{TH}$ with V_{DS} = 1 V. S and max ON/OFF were measured only for those devices for which complete pinch–off was achieved ($V_{TH} > -6$ V).

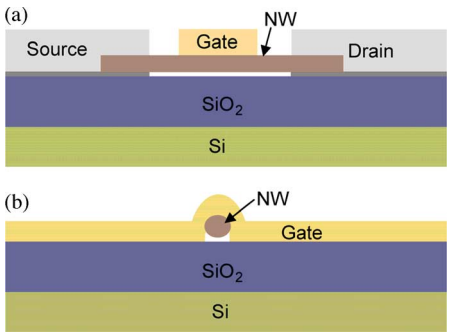

Fig. 1. (a) Schematic cross section of NW MESFET structure as seen from the side. The gap between the NW and the SiO_2 is exaggerated for clarity; in fabricated devices, the NW is effectively in contact with the SiO_2. (b) Schematic cross section of NW MESFET as seen looking down the axis of the NW, showing the omega gate structure. From FESEM inspection, the omega gate is estimated to cover one-half to two-thirds of the NW circumference.

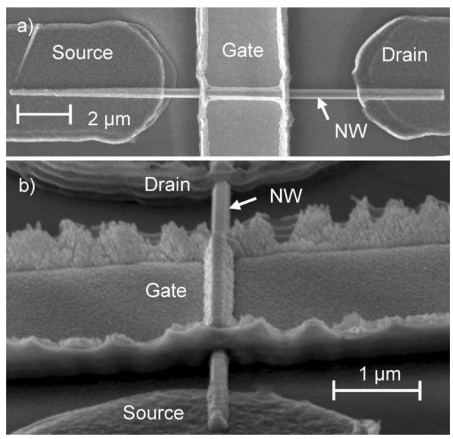

Fig. 2. (a) FESEM image of a typical NW MESFET as seen from the top. (b) FESEM image of an NW MESFET as seen from an angle looking down the length of the NW, showing the omega gate structure. The flagging metal edges are due to the lift-off process.

Twenty nanometers of Ti and 200 nm of Al were then deposited by e-beam evaporation and lifted off in acetone.

In order to electrically isolate individual devices, the Ti bottom layer interconnects were etched away by a 40-sccm CF_4, 5-sccm O_2 RIE process at 200 W and 27 Pa (200 mtorr) with a photoresist etch mask. After the etch mask was removed, the sample was annealed at 500 °C for 60 s in a 5% H_2/95% Ar ambient. Parameters similar to those used in this RIE/metallization/annealing process have been previously shown to make ohmic contacts to n-type GaN films [23]. The two-terminal source–drain current–voltage (I–V) behavior of the devices was tested after annealing.

Following the two-terminal I–V tests, the final step in fabrication was to pattern and deposit the gate electrodes. After photolithography, the sample was placed in a UV–ozone chamber for 10 min immediately prior to e-beam deposition of 30-nm Pt/300-nm Au and acetone liftoff. This Pt/Au bilayer was chosen because of the processing difficulties presented by a homogeneous top gate of either Pt or Au. The Pt acted as an adhesion layer, whereas the Au acted as an efficient filler. Due to the geometry of the NW and the nonconformal deposition method of the omega-shaped Schottky gate, it is likely that both Pt and Au were in contact with each NW. On the finished sample, there were ten single-NW devices. An FESEM image of a typical device is shown in Fig. 2.

III. CHARACTERIZATION

A. NW Resistance

The two-terminal source–drain I–V characteristics of each device were measured again after deposition of the gate electrode (with the gate floating). Both before and after gate deposition, each device exhibited a linear I–V relationship due to a source–drain bias of up to ±1 V, indicating ohmic source and drain contacts. Table I shows that device resistances before gate deposition (R_1) were between 20 and 95 kΩ. The measured

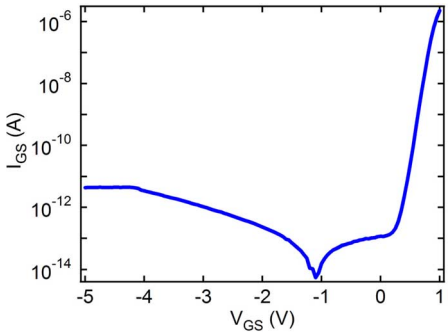

Fig. 3. Log-linear plot of the magnitude of gate–source current ($I_{\rm GS}$) versus gate–source voltage ($V_{\rm GS}$) for a typical device. The minimum at $V_{\rm GS} \approx -1.2$ V is where $I_{\rm GS}$ crosses from positive to negative. However, it is suspected that noise contributes strongly to the measurement when the magnitude of $I_{\rm GS}$ is less than approximately 100 fA (10^{-13} A).

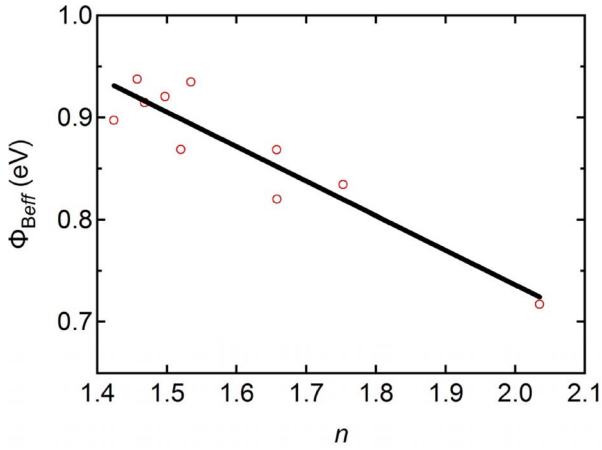

Fig. 4. Estimated values of effective Schottky barrier height ($\Phi_{B_{\rm eff}}$) versus ideality factor (n) with linear fit for ten devices. The equation of the linear fit is $\Phi_{B_{\rm eff}} = -0.34n + 1.41$ eV. From the fit, the homogeneous Schottky barrier height Φ_{B_0} was estimated to be approximately 1.1 eV.

source–drain resistance of each device after gate deposition (R_2) showed an increase of 2–56 kΩ over R_1. The increase in resistance with the addition of the Schottky gate is consistent with an increase in the width of the surface depletion layer in the gated section of the NW due to the presence of the Schottky barrier. However, other factors, such as induced strain due to bending and changes to the bare NW surface during processing for gate fabrication, may also play a role.

B. Schottky Diode Characteristics

In order to characterize the Schottky barrier between the Pt/Au gate electrode and the NW, two-terminal Schottky diode measurements were made between the gate and each ohmic electrode (source and drain) of each device. Fig. 3 shows the I–V characteristics of a typical Schottky diode measured between the gate and source of a single-NW device. The primary direction of the current flow in the NW is along the c-axis, although there are some contributions to the current along the a-axis near each metal/NW interface.

As the plot in Fig. 3 shows, this device had a low reverse-bias leakage current. The magnitude of the gate–source current $I_{\rm GS}$ of this Schottky diode stayed below 10 pA out to a gate–source bias $V_{\rm GS}$ of -5 V. In contrast, $I_{\rm GS}$ with a forward bias of $V_{\rm GS} = 1$ V reached more than 2 μA. Among the ten devices tested, the average magnitude of the reverse-bias leakage current at -5 V was approximately 22 pA. The maximum measured reverse-bias leakage current at -5 V was 102 pA.

For a single device, the magnitude of the gate–source reverse bias was increased until breakdown occurred ($V_{\rm GS} \approx -10$ V). At this point, the magnitude of $I_{\rm GS}$ increased rapidly from less than 1 nA at $V_{\rm GS} > -10$ V to more than 1 μA at $V_{\rm GS} < -11$ V. Because reverse-bias breakdown can potentially alter the rectifying behavior of a Schottky diode [24], the other devices were tested with gate voltages greater than -6 V in order to avoid breakdown. It should be noted, however, that the device that reached breakdown displayed no significant change in its rectifying behavior with $V_{\rm GS}$ or $V_{\rm GD} > -6$ V in subsequent tests. It is possible that the device underwent a soft breakdown in which tunneling was dominant [25]. However, the breakdown behavior of these devices was not studied in sufficient detail to conduct a meaningful analysis.

In the forward-bias regime, the I–V behavior of a Schottky diode can be compared to the following thermionic emission model in order to estimate the effective zero-bias Schottky barrier height $\Phi_{B_{\rm eff}}$ and the ideality factor n [24]

$$I = AT^2A^{**}\exp\left[\frac{-\Phi_{B\rm eff}}{kT}\right]\left(\exp\left[\frac{q(V-IR_s)}{nkT}\right]-1\right). \tag{1}$$

In (1), q is the magnitude of the charge of an electron, R_s is the series resistance due to the NW and ohmic contact, k is Boltzmann's constant, T is the temperature ($\sim$293 K), A is the Schottky contact area, and A^{**} is the theoretical value of the effective Richardson constant [24] (26.4 A·cm$^{-2}\cdot$K^{-2}). V is either the gate–source voltage $V_{\rm GS}$ or the gate–drain voltage $V_{\rm GD}$. Similarly, I is either $I_{\rm GS}$ or $I_{\rm GD}$. When V, and thus I, is sufficiently small, the term IR_s in (1) can be neglected. If at the same time $V > 3kT/q$, the term -1 can also be neglected. Applying these approximations and taking the natural logarithm of (1), we have

$$\ln(I) = \ln\left(AT^2A^{**}\right) + \left(\frac{-\Phi_{B\rm eff}}{kT}\right) + \frac{qV}{nkT}. \tag{2}$$

Hence, a plot of $\ln(I)$ versus V is expected to reveal a straight-line region in which the relationship of (2) holds. The parameters of a fit to this region were used to calculate n and $\Phi_{B_{\rm eff}}$ from both the gate–source and gate–drain forward-bias Schottky diode I–V curves at room temperature. Table I lists the average calculated values of $\Phi_{B_{\rm eff}}$ and n for each of the ten devices. For a given device, the gate–source and gate–drain values of each parameter typically differed by only about 1.5%. For these ten devices, the average $\Phi_{B_{\rm eff}} \approx 0.87$ eV and the average $n \approx 1.6$.

As Fig. 4 shows, there appears to be a roughly linear correlation between $\Phi_{B_{\rm eff}}$ and n. It has been suggested that such a linear correlation can be explained by lateral nonuniformity in the Schottky barriers [26]. The origin of the apparent nonuniformities is not clear, but it may be related to NW surface

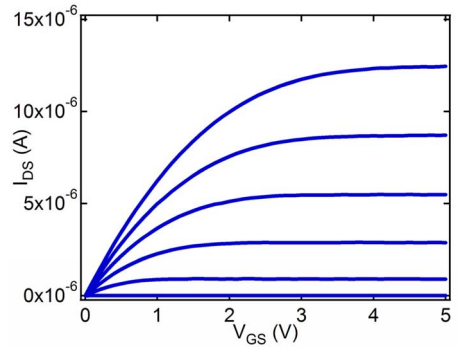

Fig. 5. Drain–source current ($I_{\rm DS}$) versus drain–source voltage ($V_{\rm DS}$) at several gate–source voltages ($V_{\rm GS}$) showing the best example of saturation observed for a single-NW MESFET. The bottommost trace corresponds to $V_{\rm GS} = -3$ V, with $\Delta V_{\rm GS} = 0.5$ V between successive traces proceeding upward.

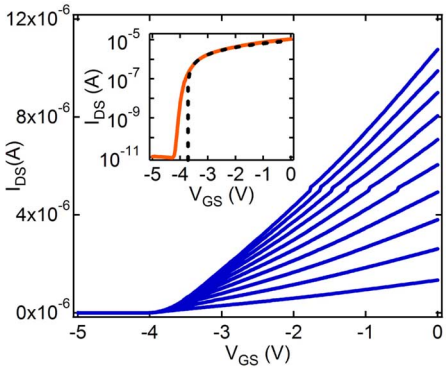

Fig. 6. Drain–source current ($I_{\rm DS}$) versus gate–source voltage ($V_{\rm GS}$) for a typical single-NW MESFET. The bottommost trace corresponds to a drain–source voltage ($V_{\rm DS}$) of 0.1 V, with $\Delta V_{\rm DS} = 0.1$ V between successive traces proceeding upward. The inset is a log-linear plot of $I_{\rm DS}$ (solid trace) and a fit to the above-threshold linear region (dashed trace) versus $V_{\rm GS}$ for $V_{\rm DS} = 1$ V. The equation of the linear fit is $I_{\rm DS} = 2.40 \times 10^{-6} V_{\rm GS} + 8.95 \times 10^{-6}$ A. The linear fit was used to estimate $V_{\rm TH} \approx -3.7$ V. The apparent kink in each of the $I_{\rm DS}$ versus $V_{\rm GS}$ curves at 5 μA is an artifact due to an automatic change in the measurement range of the ammeter.

contamination during processing or the use of an inhomogeneous Schottky metallization. Contaminants at the interface between the NW and the SiO_2 substrate may also play a role in causing deviations from ideal behavior. A rough estimate of the homogeneous barrier height Φ_{B_0} was obtained by extrapolating the linear fit of the data points to $n \approx 1$, which resulted in $\Phi_{B_0} \approx 1.1$ eV. However, it should be emphasized that the linear extrapolation method used to find Φ_{B_0} is only approximate in this range of n and $\Phi_{B_{\rm eff}}$.

The effective inhomogeneous barrier heights measured here are higher than those previously reported for individual GaN NW Schottky diodes with Pt Schottky contacts (0.2–0.62 eV) [18], [19]. As in this paper, each of these previous NW studies has assumed the theoretical value of A^{**}. However, the values of $\Phi_{B_{\rm eff}}$ reported here are on the low side of effective barrier heights reported for Pt and Au on planar GaN (0.88–1.13 eV for Pt, 0.8–1.88 eV for Au) [24]. It is worth noting that the homogeneous barrier height Φ_{B_0} ($\sim$1.1 eV) estimated for these NWs is in the middle to upper range of the reported Schottky barrier heights measured from I–V characteristics of Au and Pt on GaN films.

Although higher than the ideality factors reported for many GaN film devices, the ideality factors measured here are significantly lower than those reported previously for individual GaN NW Schottky diodes [18]–[20]. These previous reports attributed high values of n to NW surface damage during Schottky contact fabrication ($n = 18$) [18], a small Schottky contact area in which tunneling current becomes important ($n = 6.5$) [19], and an insulating interfacial layer between the NW and the Schottky metal ($n = 17.8$) [20].

C. MESFET Characteristics

After the Schottky barriers were characterized, each Schottky gate was used to modulate the conducting channel of its NW by varying the negative gate bias, thus yielding MESFET behavior. The substrate was unbiased (floating) during all MESFET tests. $I_{\rm DS}$ versus $V_{\rm DS}$ at different $V_{\rm GS}$ for one MESFET is shown in Fig. 5. This device most clearly showed saturation of $I_{\rm DS}$.

Fig. 6 shows $I_{\rm DS}$ versus $V_{\rm GS}$ at several values of $V_{\rm DS}$ for a typical device. The threshold gate voltage $V_{\rm TH}$ at which the conducting channel pinched off was estimated by fitting a line to the linear region [27] of $I_{\rm DS}$ versus $V_{\rm GS}$ at $V_{\rm DS} = 1$ V and extrapolating to $I_{\rm DS} = 0$ A. From the fit line (Fig. 6, inset), the threshold gate voltage of this device was estimated to be $V_{\rm TH} \approx -3.7$ V. The maximum transconductance g_m was estimated to be $g_m \approx 2.4$ μS at $V_{\rm DS} = 1$ V. $V_{\rm TH}$ and maximum g_m at $V_{\rm DS} = 1$ V for all ten MESFETs are listed in Table I. The average parameters from the ten devices were $V_{\rm TH} \approx -7.3$ V and $g_m \approx 2.3$ μS. Five out of the ten devices showed complete pinch off, with $V_{\rm TH} > -6$ V.

For each of the five devices for which complete channel pinch off was observed ($V_{\rm TH} > -6$ V), the subthreshold swing S and the ON/OFF ratio were also estimated for $V_{\rm DS} = 1$ V. S is the inverse of the subthreshold slope, measured in the subthreshold regime where $I_{\rm DS}$ depends exponentially on $V_{\rm GS}$. The measured values of S are listed in Table I. On average, $S \approx 70$ mV/decade, although S as low as 63 mV/decade was observed. This is close to the theoretical limit of $S \approx 60$ mV/decade at room temperature [16]. In addition to low subthreshold swing values, these MESFETs also demonstrated high ON/OFF ratios. The ON/OFF ratio reported here is the ratio of $I_{\rm DS}$ at $V_{\rm GS} = 0$ V and $V_{\rm DS} = 1$ V to the minimum measured $I_{\rm DS}$ at $V_{\rm GS} < V_{\rm TH}$ and $V_{\rm DS} = 1$ V. Table I shows that the ON/OFF ratio ranged from 1×10^6 to as high as 5×10^8 for $V_{\rm DS} = 1$ V.

A variable amount of hysteresis with respect to the gate voltage sweep was observed for all ten GaN NW MESFETs. Hysteresis and gating memory effects have been reported in previous GaN NW FET studies as well [6], [7], [13], where the effect has been attributed primarily to charge trapping in the gate oxide. An example of the hysteresis observed for one NW MESFET is shown in Fig. 7.

The source of the hysteresis is unclear. It has been suggested that charge trapping by surface-bound water molecules at the SiO_2/nanotube interface could be the primary cause of gating

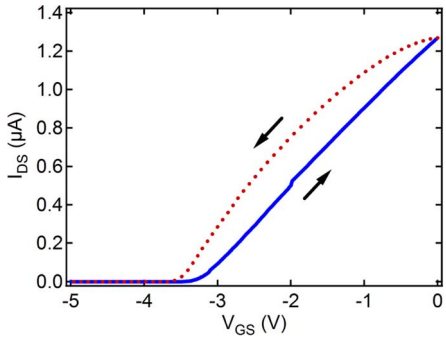

Fig. 7. Hysteresis in drain–source current ($I_{\rm DS}$) versus gate–source voltage ($V_{\rm GS}$) at drain–source voltage ($V_{\rm DS}$) of 0.1 V for a single-NW MESFET. $V_{\rm GS}$ was swept from -5 to 0 V (solid trace), and then immediately swept from 0 to -5 V (dotted trace). The maximum offset between the two sweeps is approximately 600 mV.

hysteresis in back-gated carbon nanotube FETs [28], [29]. It is possible that similar water-induced charge trapping occurred at the SiO_2/NW interface beneath these GaN NW MESFETs. NW surface states due to other contaminants may also play a role. The hysteresis in these devices is the subject of ongoing investigation.

The MESFETs reported here compare favorably with the GaN-NW-based MOSFETs that have been reported in the literature. GaN NW MOSFETs have frequently shown threshold gate voltages exceeding 20 V in magnitude [10]–[14]. Yu *et al.* reported a GaN NW MOSFET with conductance modulation better than three orders of magnitude when the gate voltage was switched between a value just below threshold ($V_{\rm TH} \approx -8$ V) and 6 V [15]. Huaqiang *et al.* showed a top-gated GaN MOSFET with $V_{\rm TH}$ as small as -4 V and an ON/OFF ratio of around 10^6 at $V_{\rm DS} = 2$ V [8]. The best GaN NW MESFET in this study showed an ON/OFF ratio of 10^8 with $V_{\rm TH} = -2.6$ V at $V_{\rm DS} = 1$ V.

MESFETs based on GaN films have shown threshold voltages similar to those reported here [1], [3]–[5]. The maximum absolute $I_{\rm DS}$ and g_m of these GaN film MESFETs are typically two or three orders of magnitude higher than those reported here; this is largely due to the much larger conducting channel in MESFETs based on thin films. When g_m is normalized by the device width, values on the order of 20–50 mS/mm have been obtained in thin-film devices. In contrast, g_m divided by the NW diameter in the GaN NW MESFETs ranges from 4 to 9 mS/mm. However, it should be noted that g_m reported here was measured at $V_{\rm DS} = 1$ V (below saturation), which is lower than the true maximum g_m at saturation.

IV. Conclusion and Future Work

Although many of the MESFETs reported here performed well compared to previously reported GaN NW FETs, the design and fabrication of GaN NW MESFETs could be optimized to further improve device performance. First of all, surface treatments and alternative metallizations could be investigated to try to increase the effective Schottky gate barrier height and reduce the ideality factor [30], [31]. Second, a cylindrically conformal Schottky gate could be used in place of the omega-shaped gate. Because a conformal gate would allow the entire circumference of the NW to be gated simultaneously and symmetrically, it would make the modulation of the conducting channel more efficient. Third, passivation techniques or alternative substrates could be explored to reduce or eliminate the gating hysteresis [28], [29]. The MESFET results presented here suggest that an optimized GaN NW MESFET device could show several orders of magnitude of conductance modulation with switching voltages on the order of 1 V or less.

In conclusion, we have demonstrated MESFETs based on individual GaN NWs. The average effective Schottky gate barrier height was 0.87 eV. The average ideality factor of 1.6 was much closer to unity than values reported previously for Schottky diodes on individual GaN NWs. We measured threshold gate voltages ranging from -15 to -2.6 V, with transconductances between 1.4 and 3.4 μS. The MESFETs also exhibited near-ideal subthreshold swings and ON/OFF drain–source current ratios from 1×10^6 up to 5×10^8. These results show that Schottky gates have the potential to significantly improve the performance of field-effect devices based on single GaN NWs.

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