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Random Telegraph Signals and 1/*f* Noise in ZnO Nanowire Field Effect Transistors

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***Abstract* — Single-crystal ZnO nanowires have been fabricated as field effect transistors (FETs). The low frequency noise in the drain current of n-type ZnO FETs has been investigated through random telegraph signals (RTSs) at 4.2 K and 1/*f* noise at room temperature. At room temperature, the noise power spectra have a classic 1/*f* dependence with a Hooge parameter that is ~ 5 × 10^{-3}. ZnO FETs measured in a dry O_2 environment displayed elevated noise levels that can be attributed to increased fluctuations associated with O_2^- on the nanowire surfaces. At 4.2 K, the device's noise spectra change from 1/*f* to Lorentzian type, and the current traces as a function of time show random telegraph signals (RTSs). The channel current RTSs are attributed to correlated carrier number and mobility fluctuation due to the trapping and emission of carriers by discrete border traps. At certain bias conditions, the current in the channel shows three-level switching events with amplitudes as high as 40 %, from which two individual defects with energies close to the Fermi level in the ZnO channel can be distinguished.**

Keywords —***1/f noise, nanowire, oxide trap, random Telegraph Signal, ZnO***

I. INTRODUCTION

For submicron CMOS and nanowire/nanotube field effect transistor (FET) structures, one fundamental factor limiting their performance is the conduction fluctuation or signal-to-noise ratio. Because of the large surface-to-volume ratio of nanowire/nanotube FETs and unpassivated nature of their surfaces, the low frequency current noise fluctuations can be more pronounced in such devices due to the enhanced scattering from surface states. As a result, it is critical to reduce the noise and fluctuations in these devices, at least to a level comparable to traditional MOSFETs, before nanowires/nanotubes can be used in integrated circuits. Low frequency 1/*f* noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices. [1-3] The use of noise as a defect characterization method has become even more popular in recent years for deeply scaled Si MOSFETs [4-8] and nano-scale devices [9-12], because the sensitivity of this technique improves as the size of the devices is reduced, as opposed to capacitance-voltage and charge pumping measurement methods which become less accurate as the device size decreases and require a substrate contact. 1/*f* noise was modeled by McWhorter in 1957 as carrier number fluctuations caused by the tunneling of electrons in and out of surface states [13]. In large area transistors, the large number of trapping/detrapping processes with a broad range of time constants lead to 1/*f* type spectra, by the superposition of Lorentzians [3]. For submicron silicon MOSFETs and nanowire/nanotube FETs, the fluctuating occupancy of individual electron traps in the gate dielectric close to the semiconductor/insulator interface generates discrete switching events in the drain current, resulting in two or more current levels in the current time trace, which are referred to as random telegraph signals (RTSs). The fluctuation of the current amplitude in the confined channel can be as high as 60-70 % for both planar submicron MOSFETs and carbon nanotube FETs [14-15], posing a significant threat to the stability of scaled CMOS and nano-structures. At the same time, the study of RTS can provide a novel technique to probe a single trap and allows one to understand the fundamental physics behind the carrier transport and current fluctuations in nano-scale devices [16-20]. To our knowledge, using RTSs to study individual defects in ZnO nanowires has not been reported. In this work, n-type ZnO nanowire FETs were fabricated. Their low frequency noise and RTS properties were characterized and analyzed at both room temperature and 4.2 K as a function of gate bias. The noise spectra change from 1/*f* type at room temperature to Lorentzian at 4.2 K, due to the reduction of the channel carrier numbers and the shrinking of the trap energy range accessible to channel carriers. The physical nature of the traps responsible for the two- and three-level RTSs is also analyzed.

II. EXPERIMENTAL

ZnO nanowires were synthesized by thermally vaporizing a mixed source of commercially available ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1:1 in a tube furnace. A c-plane sapphire was used as the substrate for the ZnO nanowire growth. After an initial cleaning, a 3 nm Au thin film was deposited on the sapphire substrate. Then the substrate and the source materials were loaded into a quartz tube and the ZnO NWs were grown on the substrate surface at a temperature of 920 ºC for 20 min under the flow of a gas mixture of O_2 and Ar (0.2 % O_2 in Ar) with a flow rate of 50 sccm.

Figure 1(a) shows the field emission scanning electron microscopy (FE-SEM) image (tilted view) of vertically and uniformly grown ZnO NWs on the entire sapphire substrate. Figure 1(b) shows a high-resolution transmission electron

microscopy (HR-TEM) image and a selected-area electron diffraction pattern (inset) of the ZnO NWs. The discrete diffraction spots indicate that the ZnO nanowires is hexagonal wurtzite single-crystalline. The X-ray diffraction spectrum in Figure 1(c) further shows that the as-synthesized ZnO NWs have the hexagonal wurtzite structure with lattice parameters of a = 0.33 nm and c = 0.52 nm. A single peak at approximately 378 nm is observed in the photoluminescence (PL) spectrum (Figure 1(d)) of the ZnO NWs. This peak is attributed to near the band-edge recombination of free excitons. These results confirmed that these are high quality single crystalline ZnO NWs and the preferred growth direction is [0001].

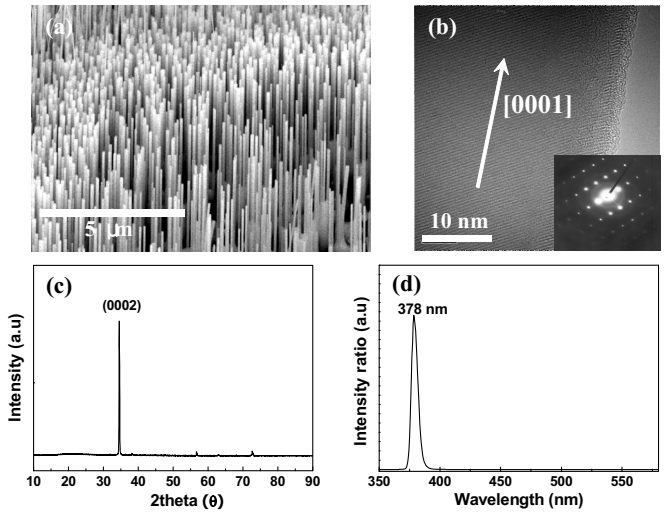

Figure 1. (a) FE-SEM image of ZnO NWs grown on a sapphire substrate (tilt view). (b) HR-TEM image of an individual ZnO nanowire showing its [0001] preferred growth direction. The inset shows a selected-area electron diffraction pattern. (c) X-ray diffraction spectrum of the ZnO NWs. (d) PL emission spectrum showing a strong emission at ~378 nm.

The grown ZnO NWs were removed from the substrate by a brief sonication in ethanol (30 - 60 sec). The nanowires in solution are then dropped onto a 100 nm thick, thermally grown, oxide on a highly doped p-type silicon substrate that can be used as a gate electrode. Ti/Au (30 nm/200 nm) contacts were deposited by using an electron beam evaporator and defined by standard photolithography and a lift-off process to form the source and drain electrodes. The distance between source and drain electrodes is approximately 4 μm. Current-voltage characteristics of the ZnO NW FETs were measured by using a semiconductor parameter analyzer. The low frequency noise characterization for these devices was performed by using a typical noise measurement setup composed of a low noise DC biasing source, a low noise current amplifier, and a dynamic spectrum analyzer. All of the measurements were carried out at room temperature and under high vacuum (<1.5x10^{-6} Torr) unless otherwise mentioned.

III. RESULTS AND DISCUSSION

The DC electrical measurements were conducted at high vacuum (<1.5x10^{-6} Torr). Figure 2(a) and the inset show the I_{ds}-V_{ds} and I_{ds}-V_g characteristics of a ZnO transistor at room temperature. The modulation of the channel conductance indicates n-channel depletion mode of device operation with a threshold voltage ~ –0.5 V. The hysteresis of the I_{ds}-V_g characteristic is considerably smaller than that in air because

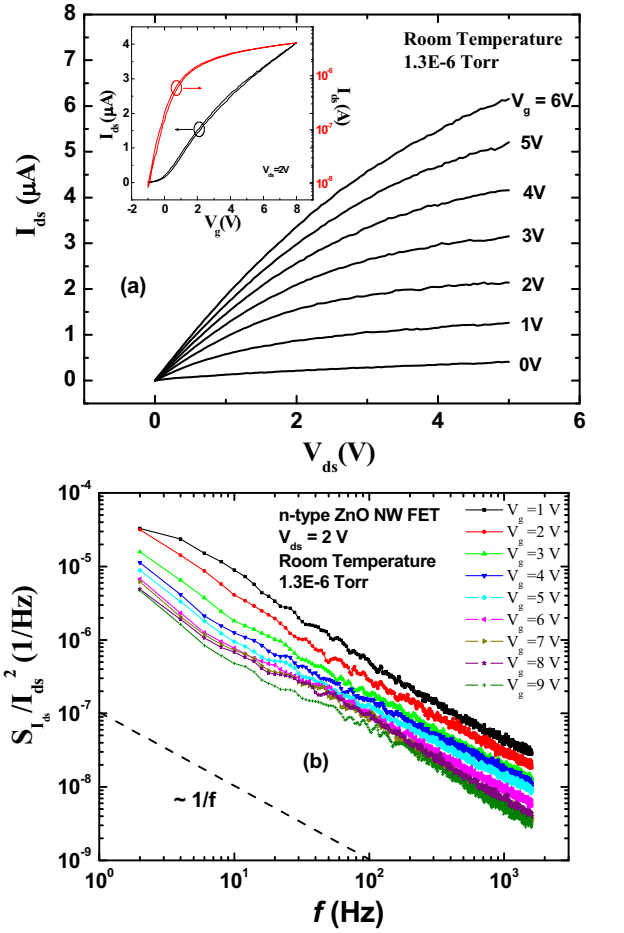

Figure 2. (a) I_{ds} versus I_{ds} characteristics for an n-type NW FET device at room temperature at 1.3 x 10^{-6} torr. The inset shows the I_{ds} versus V_g curve in both linear and log scales, showing good n-type transistor characteristics with small hysteresis; (b) normalized drain current noise power spectrum density as a function of the gate bias in the frequency range 1 Hz – 1.6 kHz at room temperature. V_{ds} is constant at 2 V.

surface absorption effects are minimized. Typical normalized drain current noise spectra are plotted in Figure 2(b) with the device biased at V_{ds} = 2 V and the gate bias varying from 1 V to 9 V. The frequency range is from 1 Hz to 1.6 kHz. The low frequency noise spectra are predominantly $1/f^{\alpha}$, with the frequency exponent α close to 1. Further analysis shows the normalized current noise S_{Ids}/I_{ds}^2 varies with $1/I_{ds}$ over the whole current range studied, indicating either a mobility fluctuation origin for the noise in the ZnO nanowire at room temperature [21], or number fluctuation noise, with an increase in defect density as the defect energy levels approach the band edge [22]. For 1/*f*-type fluctuations, the noise behavior can be described by

$$S_{I_{ds}} = \frac{AI_{ds}^{2}}{f^{\alpha}}, \qquad (1)$$

where A is the noise amplitude, f is the frequency, and $S_{I_{ds}}$ is the power spectrum density of the drain current.

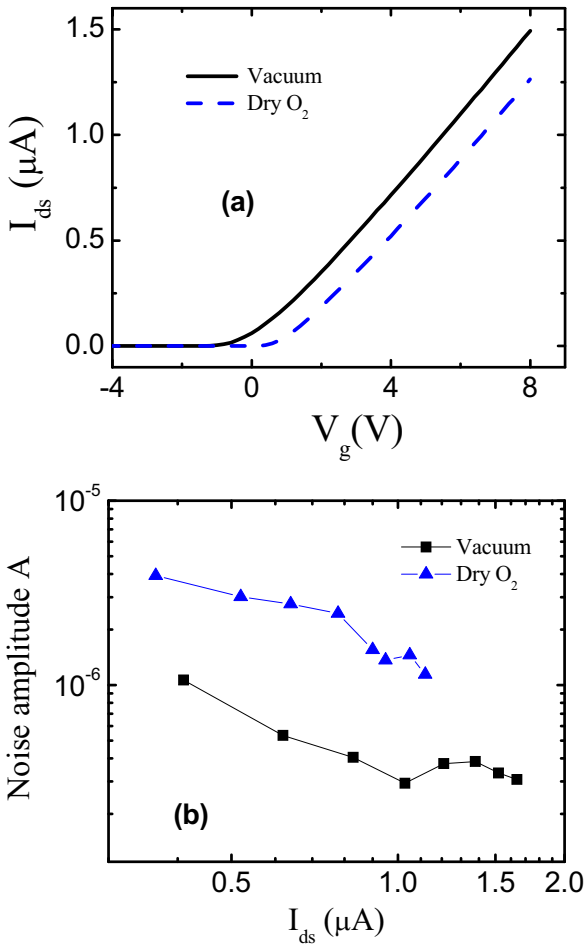

Figure 3. (a) I_d–V_g characteristics of the ZnO NW FET device in vacuum and dry oxygen environments. V_d = 1 V. (b) Noise amplitude as a function of drain current under different gate biases in vacuum and the oxygen environments. V_d = 1 V.

Several groups have previously reported the oxygen sensing properties of ZnO NWs [23-25]. We also performed noise measurements in a dry oxygen environment on a different device with similar dimension. The device was tested in vacuum at first and then left in dry oxygen under a pressure of 900 Torr for 2 days before the measurements to ensure that oxygen molecules occupy the majority of the surface vacancy sites of the ZnO NW. Figure 3(a) shows typical device I_{ds}–V_g characteristics before and after the introduction of the dry O_2. Compared to the vacuum data, the threshold voltage shifted from 0.05 to 0.87 V under the oxygen environment. This observation agrees with previously published reports that showed ZnO NW FETs' oxygen sensing properties [24-25]. It has been proposed that O_2 molecules can be absorbed at surface vacancy sites of the metal-oxide nanowires and then accept electrons to form O_2^- [24]. These chemisorbed O_2^- lead to the observed threshold voltage shift and deplete surface electron states; thus, at a given voltage, the channel carrier concentration is reduced and there is an accompanying decrease of the conductivity. Due to the threshold voltage shift, the carrier concentration in the channel has been reduced from 5.2×10^7 cm^{-1} (under vacuum) to 4.5×10^7 cm^{-1} (in dry O_2) at a gate bias of 6 V if we assume that the average dielectric constant is the same for both cases. The mobility has also slightly decreased by ~ 6%. Figure 3(b) shows the device noise amplitude as a function of drain current at various gate biases under different environments. As it reveals, the device noise level in the dry oxygen environment is nearly an order of a magnitude larger than that in vacuum. Measurements of the ZnO NW FETs in dry nitrogen environment did not show significant noise amplitude change compared to the vacuum data. The higher noise level in the oxygen environment can be elucidated by considering Hooge's empirical law $A = \frac{\alpha_H}{N}$ where α_H is the Hooge's constant and N is the total carrier number in the system [26]. The Hooge's constant is ~ 4×10^{-2} for the ZnO NW FET under the oxygen environment, compared to the observed α_H of 5×10^{-3} in vacuum. We propose that the microscopically dynamic impact of the surface bound O_2^- species on the charge transport significantly increased the carrier number fluctuations related to electron trapping/detrapping events and accompanied scattering fluctuations in the device channel, which was reflected as an increased Hooge's constant under the oxygen environment. This is similar to the situation in traditional planar MOSFET devices, where the increase of fixed charges by, for example, bias stressing or ionizing irradiation results in a shift of threshold voltage and an elevated noise level [27-28]. The interactions between the O_2^- species and carriers increased both number fluctuations and mobility fluctuations in the channel, and therefore generated a larger noise amplitude for the ZnO NW FETs in the oxygen environment.

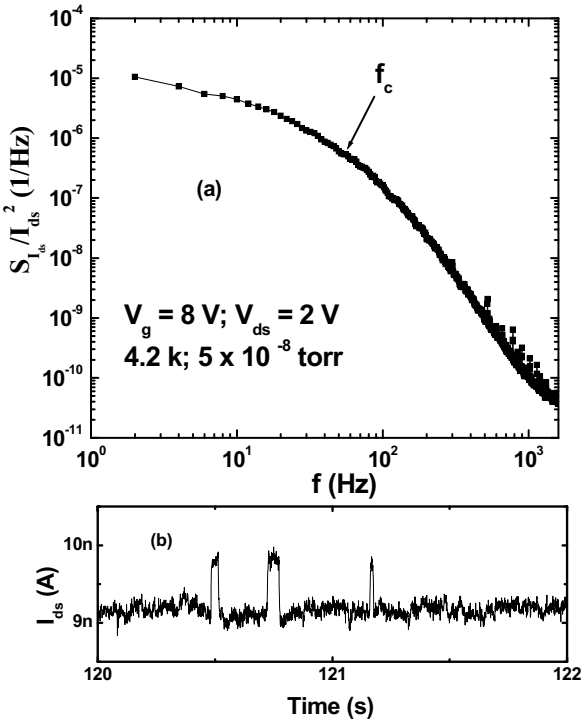

Figure 4. (a) Typical Lorentzian spectrum with corner frequency at ~ 18 Hz when the device is biased at V_g = 8 V and V_{ds} = 2 V; (b) the corresponding time domain RTS.

When the temperature is lowered to 4.2 K, the low frequency noise in the device from Figure 2 changes from 1/*f* to a Lorentzian spectrum. Figure 4(a) shows the noise spectrum of the ZnO nanowire FET biased at V_{ds} = 2 V and V_g = 8 V at 4.2 K, which can be described by

$$\frac{S_{I_{ds}}}{I_{ds}} = \frac{K}{(1+f/f_c)^2}, \qquad (2)$$

where K is a constant independent of frequency and f_c is the corner frequency of the Lorentzian. The Lorentzian spectrum is caused by the trapping and detrapping of a single defect in the dielectric. The signature of this single trap state is also shown in the RTS of the drain current time trace of Figure 4(b), where the channel current switches between two discrete values. The change of temperature to 4.2 K primarily decreases the number of defects in the dielectric accessible to the carriers in the wire and responsible for the fluctuations to a few single traps due to the shrinking of the activated energy window (~ 4 k_BT, where k_B is the Boltzmann constant) in the dielectric bandgap. In addition, it is accentuated by reduced carriers as indicated by a three orders of magnitude decrease of current at 4.2 K compared to room temperature. As a result, the trapping/detrapping of carriers from the traps causes more dramatic fluctuations of the channel current. The RTS trace in Figure 4(b) is a small portion of the curve in Figure 5(a) (where V_g = 8 V). The corner frequency f_c can be estimated to be ~ 18 Hz by locating the peak of S_{Ids}*f vs f plot. This is consistent with the calculation from mean time at high current τ_{on} and low current τ_{off} from the current time trace in Figure 4(b), where $f_c = 1/2\pi\tau_0$ and $1/\tau_0 = 1/\tau_{on} + 1/\tau_{off}$.

In Figure 5(a), 300 s drain current traces were recorded at V_{ds} = 2 V as a function of gate bias; the corresponding histograms of the drain current data are plotted in Figure 5(b) for more detailed analysis. For the case of two discrete levels at V_g = 8 V, the corresponding histogram plot in Figure 5(b) shows two distinct peaks with a background Gaussian distribution, indicating only one near interface oxide (border) trap, A, interacting with the carriers through tunneling. At this bias condition, only one trap in the dielectric resides in the band gap within ~2 kT of the channel Fermi level, and is within a favorable distance from the channel to be able to be electrically active in the reversible capture and emission processes with the channel carriers.

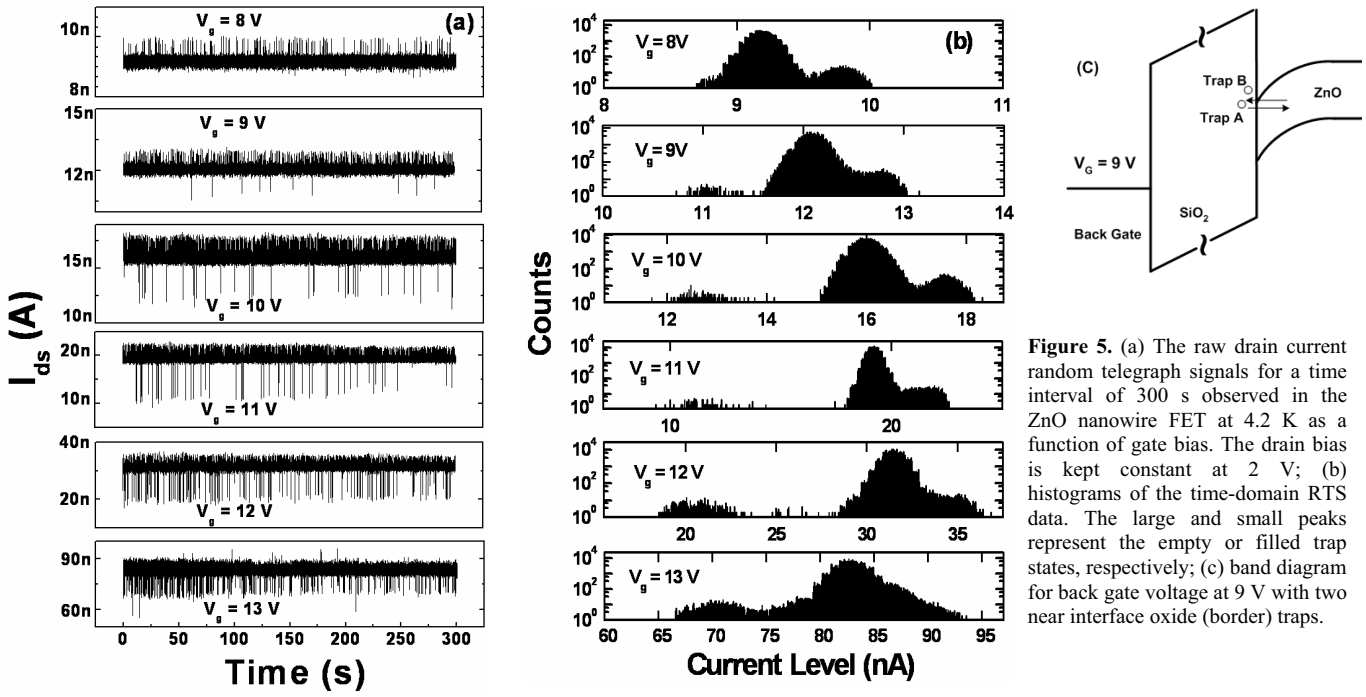

Figure 5. (a) The raw drain current random telegraph signals for a time interval of 300 s observed in the ZnO nanowire FET at 4.2 K as a function of gate bias. The drain bias is kept constant at 2 V; (b) histograms of the time-domain RTS data. The large and small peaks represent the empty or filled trap states, respectively; (c) band diagram for back gate voltage at 9 V with two near interface oxide (border) traps.

The low current level corresponds to the state that one electron is captured by the trap A while the high current level corresponds to the empty state. As the gate bias increases, the trap occupancy increases. When V_g is increased to 9 V, negative peaks appear and the current trace shows three levels, confirmed by the three distinctive peaks in the corresponding histogram. It has been argued that this could be due to multiple electron trapping at one defect site [2], which is highly unlikely due to the repulsive force between a electron and a negatively charged trapping center. The most likely scenario is that there is a second border trap [29], B, with a slightly higher energy than trap A, located within ~ 2 k_BT of the Fermi level in the ZnO nanowire when the bias on the gate is increased, which causes more band bending. Here the high current value corresponds to the state where both traps are unoccupied, the middle current level is observed when trap A is charged while trap B is empty, and the low current level likely corresponds to the state where both traps are filled. The band structure of the measured device with two traps can be illustrated in Figure 5 (c). As the gate voltage increases to ~ 13 V, only trap B aligns with the Fermi level so simple two level RTS is again observed. Trap B gives much larger RTS amplitude compared to trap A,

presumably due to a closer proximity to the channel. The number fluctuation caused by a single electron trapping/detrapping cannot account for the significantly large RTS amplitude ΔI_{ds} (~40 %). The combination of number and mobility fluctuations caused by coulomb scattering is dominant in our case.

IV. CONCLUSIONS

In summary, measurements of the devices in dry O_2 environment exhibited a higher noise level, which could be attributed to the increased channel fluctuations associated with O_2^- bound at the ZnO surface. This study also suggests that the changes of the noise characteristics under different environments could be utilized as a new sensitive method for sensing applications. We have observed anomalous RTSs in the drain current of ZnO nanowire FETs for the first time. 1/f noise is dominant at room temperature and the spectra change to Lorentizians at 4.2 K. The defects responsible for the RTSs are not visible by using conventional techniques which only measure average properties and miss the transient events. The channel current RTSs are attributed to the correlated carrier number and mobility fluctuation due to the trapping and detrapping of the carriers by discrete border traps in the SiO_2. At certain bias conditions, the current in the channel shows three-level switching events with amplitudes as high as 40 % of the drain current, from which two individual defects with energies close to the Fermi level in the ZnO channel can be distinguished. The fast switching RTSs at 4.2 K suggest the effects of discrete traps on the carrier transport. The characterization of two- and three-level RTSs in these devices is a step towards the use of noise methods for the detailed characterization of the energetic and spatial position of individual defects in semiconductor nanoelectronic devices.

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