Extraction of Sheet Resistance and Line Width From All-Copper ECD Test Structures Fabricated From Silicon Preforms

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***Abstract*—Test structures have been fabricated to allow electrical critical dimensions (ECD) to be extracted from copper features with dimensions comparable to those replicated in integrated circuit (IC) interconnect systems. The implementation of these structures is such that no conductive barrier metal has been used. The advantage of this approach is that the electrical measurements provide a nondestructive and efficient method for determining critical dimension (CD) values and for enabling fundamental studies of electron transport in narrow copper features unaffected by the complications of barrier metal films. This paper reports on the results of tests which have been conducted to evaluate various extraction methods for sheet resistance and line width values from the current design.**

***Index Terms*—Copper, critical dimension (CD), electrical critical dimension (ECD), electrical test structure, line width, metrology.**

I. Introduction

THE NEED to develop a test structure capable of facilitating electrical extraction of parameters such as sheet resistance and line width from copper (Cu) interconnect features has been presented in a number of papers [1]–[3]. A detailed description of the fabrication of a Cu test structure that provides such a capability has been recently published [4]. The benefits of using this structure are that, due to the process and nature of the substrate material used, the Cu interconnect features possess a nearly rectangular cross section. This allows line width to be extracted primarily by way of electrical measurements from specially designed all-copper test structures. Although in commercial applications Cu interconnects employ barrier layers for adhesion, diffusion, and oxidation properties, the structure reported here does not include a barrier metal and allows fundamental studies of all-copper features. This work aims to further the understanding of copper interconnects both with and without barrier layers. As a means of determining the traceability of this method as well as providing necessary calibration measurements, the structure reported also allows the line width to be measured using previously demonstrated techniques including atomic force microscopy, critical dimension scanning electron microscopy, optical microscopy, and high resolution transmission electron microscopy [5]–[7]. The NIST35 design [8] was used to fabricate the all-copper test structures. Analyses of extended electrical measurements made on them are presented in this paper.

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II. Fabrication Overview

The substrate materials employed for these structures are (110) silicon wafers, chosen for their etch characteristics in anisotropic wet etch solutions. The test patterns are aligned to the $\langle 112 \rangle$ crystal-lattice vectors in the surface of the wafer and printed in a silicon oxide (SiO_2) hard mask. The pattern is then etched into the silicon with a tetramethylammonium hydroxide (TMAH) wet etch solution, which is inherently lattice plane selective. Due to the nature of the single crystal silicon and the etch solution, the sidewalls of the structures, as defined by the $\langle 111 \rangle$ crystal planes, provide a rectangular cross section with nearly atomically parallel sides [9]. This resulting silicon mesa is referred to as a "Silicon Preform" and is used as a reference for line width. The dimensions of this silicon preform are preserved with a multilayer dielectric stack of low pressure chemical vapor deposition (LPCVD) followed by plasma enhanced chemical vapor deposition (PECVD) silicon nitride (SiN). These layers are then processed in a chemical–mechanical polishing (CMP) tool to expose the top of the silicon preform while also presenting a planar surface. A portion of this silicon is isotropically removed to form a trench of which the bottom is oxidized to provide electrical isolation from the substrate. The Cu metal is deposited using physical vapor deposition (PVD), no barrier material is used in this implementation due to the requirement for an all-copper track. Following the Cu deposition, a CMP step is used to polish the wafers in a damascene manner to define the final test structure pattern. Throughout the fabrication of these devices, care has

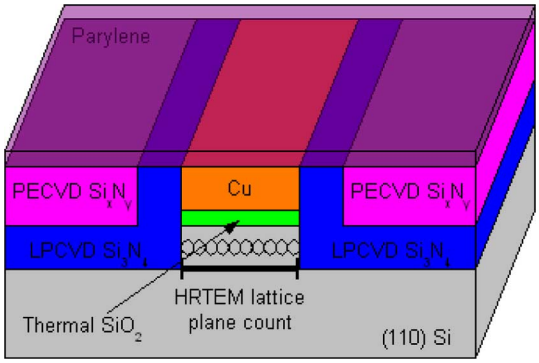

Fig. 1. Cross-sectional diagram of the test structure used [4].

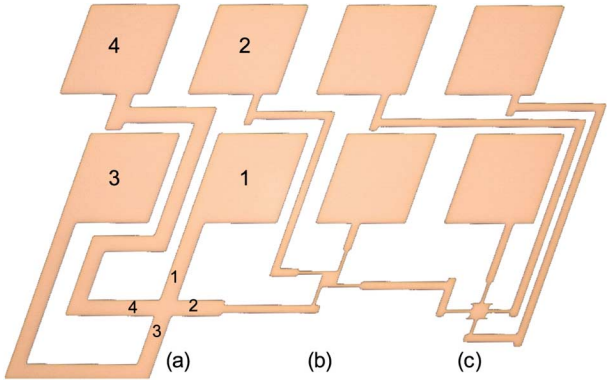

Fig. 2. Test structures used to extract sheet resistance for Cu interconnect features: (a) Greek cross; (b) corner-tapped box cross; and (c) side-tapped box cross.

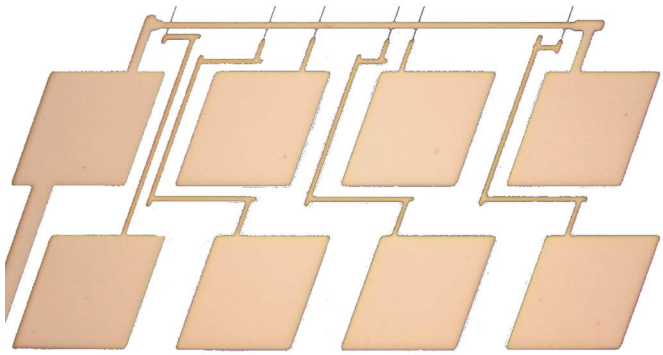

Fig. 3. Multiple-tapped Kelvin bridge resistor test structure used to extract line width for copper interconnect features.

been taken with the process steps to ensure that the Cu film does not oxidize. The final step involves the deposition of parylene to act as a passivation layer and hence prevent any oxidation of the copper features. The parylene film is removed from probe pads to allow electrical contact during testing. At this point the structure is ready for electrical measurements to extract the parameters of sheet resistance and line width (Fig. 1). Typical Cu thickness seen in the structures used for this study was 300 nm.

III. Method

The analyses of sheet resistance and line width of the copper test structures are based on work which has been reported previously [10]. Measurements are designed to be undertaken using a standard dc parametric test system comprised of a current source and a high sensitivity voltmeter[1]. Electrical contact is made to the devices using a probe station and probe card fixtures. During electrical testing, parameters were chosen to maintain the linearity of the current and voltage (*I–V*) variables and to reduce the impact of joule heating.

A. Sheet Resistance

Sheet resistance measurements reflect thickness variations in the Cu film as well as provide a useful parameter for line width extraction. *I–V* measurements were taken from three different van der Pauw sheet resistance structures located at various sites over the entire die. The three structures are the Greek cross, corner-tapped box cross, and the side-tapped box cross (Fig. 2).

Fig. 2(a) is used to explain the measurement strategy for sheet resistance measurements. Forcing a set current from arm 4 to 1 and measuring the voltage drop across arms 3 and 2 as well as similarly forcing current the reverse direction from 1 to 4 and measuring the voltage between 2 and 3 provides two values which can be averaged to determine the $\langle V/I\rangle_1$ value for the obtuse angle. In the same manner, the acute angle is measured by forcing current in both directions on arms 1 and 2 while measuring the voltage drops across arms 4 and 3, providing $\langle V/I\rangle_2$. The actual sheet resistance value is then calculated using the $\langle V/I\rangle$ values to solve for Rs in the generic van der Pauw (1) [11]:

$$\exp\left(\frac{-\pi\left\langle\frac{V}{I}\right\rangle_1}{Rs}\right)+\exp\left(\frac{-\pi\left\langle\frac{V}{I}\right\rangle_2}{Rs}\right)=1. \qquad (1)$$

[1]As dc electrical tests are performed to extract parameters from the Cu test structures, skin effects, which become noticeable in copper lines at high frequency applications, are not present.

TABLE I
Drawn Dimensions of Kelvin-Tapped Bridge Resistor Structures

Bridge Design Parameters		
Type	Design Widths (μm)	Design Lengths (μm)
Standard	1.00, 0.90, 0.80, 0.70, 0.60, 0.55	8, 16, 24, 32, 48
Long	10.00, 9.00, 8.00, 7.00, 6.00, 5.00, 4.00, 3.00, 2.50, 2.00, 1.50, 1.00	24, 48, 72, 96, 144

B. Line Width

The line width test structures used for these measurements are specifically designed to eliminate the need for strict design rule restrictions as seen in standard line width cells [12]. From Fig. 3 it can be observed that they consist of multiple tapped bridge resistors with a range of segment lengths having a constant line width from which *I–V* values can be extracted. The design of the bridges depends on whether the lines are narrow ($\leq 1\ \mu$m) or wide ($\geq 1\ \mu$m), with details of each provided in Table I. The NIST35 design is intended for use with the short bridge

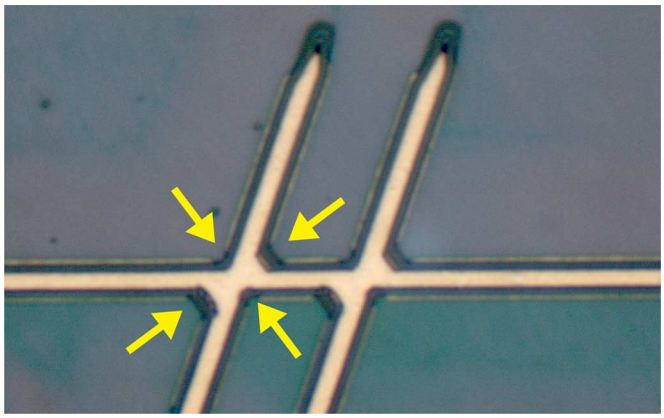

Fig. 4. Optical micrograph of the intersection of two Cu lines demonstrating the presence of facets.

technique [13] and, therefore, employs a design width of 1.0 μm for each of the voltage taps. Measurements are conducted by forcing a current along the bridge and measuring the voltage difference between adjacent taps along the structure. There are three distinct algorithms for the extraction of line width from these measurements evaluated in this work and published here.

1) Individual Segment Analysis: In this method line width is extracted using the standard formula for Kelvin type bridge resistor structures as defined in (2), where W_m is the measured line width, L_i and $\langle V/I \rangle_i$ are the segment length and $\langle V/I \rangle$ values for each segment, respectively, and R_{s_n} is the representative value for the sheet resistance of the bridge resistor:

$$W_m = \frac{R_{s_n} L_i}{\left\langle \frac{V}{I} \right\rangle_i}. \tag{2}$$

As there are multiple segments in each structure all having the same line width, extracted values for W_m can be taken and averaged to reduce measurement error.

2) Multiple Segment Analysis: Another approach to extracting ECD values from the test structures is to apply linear regression techniques to solve for line width. One point to note is that, due to the nature of photolithography and the etching of the silicon, the intersection of the line and the voltage taps produce facets of unknown dimensions as seen in Fig. 4. These facets present an electrical influence on the structure and hence introduce a source of uncertainty seen as a difference from the drawn line length. Furthermore, at small dimensions, where the tap width is of the same or larger dimension than the bridge structure, further variations in measurements due to the intersection of the taps are experienced. This value of line length variation is described by the term δL [13], [14]. Equatiion (3) better defines the formula for determining the line width (W_m) of a given structure by including the numerical effect of the facets on the line length[2]:

$$W_m = \frac{R_{s_n} (L_i - \delta L)}{\left\langle \frac{V}{I} \right\rangle_i}. \tag{3}$$

[2]Lateral current flow through single-level patterning means that transmission line model issues do not have to be provided for.

This method requires that the test structure has $n \geq 2$ line segments each having the same line width but different segment lengths. The process starts by plotting the $\langle V/I \rangle$ values against the tap separation distances of the segments from which they were measured. Then by applying least squares fit, a linear relation can be derived to relate the data points to one another as described by (4), where m is the slope of the line and b is the intercept of the line at the $L_i = 0$ axis:

$$\left(\frac{V}{I} \right)_i = mL_i + b. \tag{4}$$

The standard equation of a line becomes apparent by re-writing (3) to the form:

$$\left\langle \frac{V}{I} \right\rangle_i = \left(\frac{R_s}{W_m} \right) L_i + \left(\frac{R_{s_n}}{W_m} \right) (-\delta L). \tag{5}$$

Therefore,

$$\text{slope}(m) = \left(\frac{R_s}{W_m} \right) \tag{6}$$

and

$$\text{intercept}(b) = \left(\frac{R_s}{W_m} \right) (-\delta L). \tag{7}$$

Equation (6) defines the relationship between Rs and measured line width while the δL term is found by dividing the intercept of the line relating the segments by the slope of the same line as seen in (7). Using the slope of the line and a measured Rs value, the line width can be calculated.

3) Multiple Structure Analysis: This final technique further improves upon the values based on the data gathered from the multiple segment approach. As will be seen in the results presented later, issues arise when using the van der Pauw structures to determine values for Rs. Sheet resistance is used as a measure of resistivity of thin films that have a uniform thickness. One issue with the current van der Pauw structures is due to the facets, as explained earlier, which present a nonplanar geometry in the structure, and therefore the film in the crosses is not of uniform thickness. Furthermore, when CMP is used, process induced effects, present in small lines used for ECD extraction, result in variations in sheet resistance between the van der Pauw structures and the multiple tapped bridge resistors. The most predominant of these effects is the dishing of the copper lines which can also result in nonuniformity of Rs values within a single structure. For example, the extent of the dishing of the middle of a line may vary from the dishing at the intersection between the line and the taps, hence presenting thickness variations over the length of the structure. Therefore, the Rs term used in (2), (3), and (6) is not necessarily truly representative of the sheet resistance of the copper in the structure. As a consequence alternative means for determining sheet resistance values need to be implemented.

This is achieved by plotting slope values against the drawn line width for each device, provided there are $n \geq 3$ structures. The drawn line widths are used to provide a measure of the relation between the full set of structures without incorporating any process bias that may be present in the fabricated structures. By applying nonlinear regression with a least squares fit approach, a curve described by (8) can be used to represent the relationship between multiple structures with different drawn line widths:

$$m_n = \frac{a}{(W_m)_n^k}. \tag{8}$$

In this equation, m_n is the slope of structure n as determined from (4), a is a term primarily proportional to the sheet resistance of the measured structures, and k is proportional to the range in measured line width $(W_m)_n$ from the result of the regression fit. With values for a and k, the line width for each structure can be calculated by substituting the slope (m_n) of each line into (8) and solving for $(W_m)_n$.

IV. Results

A. Sheet Resistance

I–V values have been taken from a full array of six by three structures within a single die. Sheet resistance (Rs) values were then calculated using (1) based on averaged measurements from both the acute and obtuse angles on the upper and lower portions of the van der Pauw cross structures. A contour plot can then be generated to represent the sheet resistance over a complete die as seen in Fig. 5. These data display a similar trend in systematic variation, within a single die, for the three different types of van der Pauw structures. There are a number of process-induced effects which can be used to explain this occurrence. Firstly, CMP can result in similar systematic variations over a wafer or die due to the effects of dishing. Another possibility is the variations introduced from the trench etch stage of the fabrication process.

To fully understand the range in extracted Rs values, a comprehensive analysis was conducted on the Greek cross structure. The range in measured Rs values from this structure ($49\ \mathrm{m}\Omega/\square$ to $52\ \mathrm{m}\Omega/\square$)[3] translates to an equivalent thickness range from 296 nm to 314 nm[4]. This 18 nm range in thickness could easily be the result of CMP dishing variation over the die. AFM scans were taken of the Greek cross in die $\{1, 3\}$ and compared to another scan taken from die $\{6, 3\}$. The Rs values for these die vary by $1.9\ \mathrm{m}\Omega/\square$, which has the equivalent thickness variation of approximately 12 nm. Profiles extracted from the AFM scans agree with these predictions by demonstrating a difference in dishing value between the two structures of 18 nm. The deviation in equivalent thickness difference and measured thickness difference can be attributed to factors such as accuracy of measurement equipment as well as the true bulk resistivity value of the deposited and patterned Cu feature that can vary from the nominal value reported in literature.

[3] Rs values are represented in terms of ohms per square ($\Omega/\square$).

[4] The values reported here, and elsewhere, for equivalent thickness are based on the assumption that the copper has a bulk resistivity of $1.539\ 10^{-8}\ \Omega\mathrm{m}$ [15].

One important factor to note is that the mask set used to define these structures was intended for use on doped SOI structures which would not have undergone a CMP step and therefore would be more likely to have a uniform distribution of sheet resistance over a single die. For this reason, the NIST35 design includes large ($20\ \mu\mathrm{m}$) crosses/boxes on each of the van der Pauw structures to allow for more accurate measurements of sheet resistance. However these large features pose a problem for the Cu CMP stage as larger line widths are known to dish to a greater extent than smaller line widths [3]. This leads to the need to use smaller dimensions to reduce the dishing of the Cu and provide more appropriate measurements of sheet resistance with minimal variation.

By observing the contour plots in Fig. 5, it can be noted that, while there is a general agreement in the variation over the whole die, there is no specific agreed value between the three structures for each location. The Rs values obtained from the Greek cross test structures are consistently lower than the other two structures. This is made apparent by an average Rs of 50 m $\Omega/\square$ (implying a Cu thickness of 336 nm) for the Greek cross, while the values for the corner-tapped and side-tapped box average at 59 m $\Omega/\square$ (implying a Cu thickness of 284 nm). This suggests that the thickness varies between the Greek cross and the other two structures by roughly 50 nm. The one observation that can be made by comparing the physical layout of these three structures is that the Greek cross employs larger arms to make contact with the central cross/box area. This is supported in the design with the Greek cross having $20\ \mu\mathrm{m}$ arms while the two box cross structures have $5\ \mu\mathrm{m}$ arm widths. In order to determine whether this Rs difference is the result of dishing variations during the Cu CMP stage, atomic force microscope (AFM) scans were taken of all three van der Pauw structures within a single cell. Results of the AFM measurement demonstrate that while there is a slight variation in the degree of dishing (roughly 5-nm difference between the three structures within a single cell), this does not account for the 50 nm equivalent thickness variation observed in the electrical measurements. The next possibility is that the trench etch stage could have produced varying depths between the Greek cross and the box cross structures, which in turn denotes the final Cu thickness in the trenches. To test this theory, the Cu was etched from the wafers and an AFM used to measure the height profile of the resulting trenches, as shown in the cross-section plot in Fig. 6. Results from this test show that the Greek cross structure has trench depth of $\sim 405\ \mathrm{nm}$ while both box structures have a trench depth of $\sim 360\ \mathrm{nm}$. The difference in trench depth $(\sim 45\ \mathrm{nm})$ coupled with the variation in Cu dishing $(\sim 5\ \mathrm{nm})$ could account for the 50 nm equivalent Cu thickness variation observed in the ECD analysis. The exact cause for this step height variation is currently unknown, but believed to be related to the larger open area of the Greek cross structure due to the $20\ \mu\mathrm{m}$ arm widths and the effect thereof during the trench etch stage of fabrication. It is also worth noting that the Cu thickness as determined from ECD measurements differs from the AFM measurements of the trenches by approximatley 70 nm. While Cu dishing is measured at roughly 30 nm on these structures, it is believed that the remaining difference is due to the resistivity

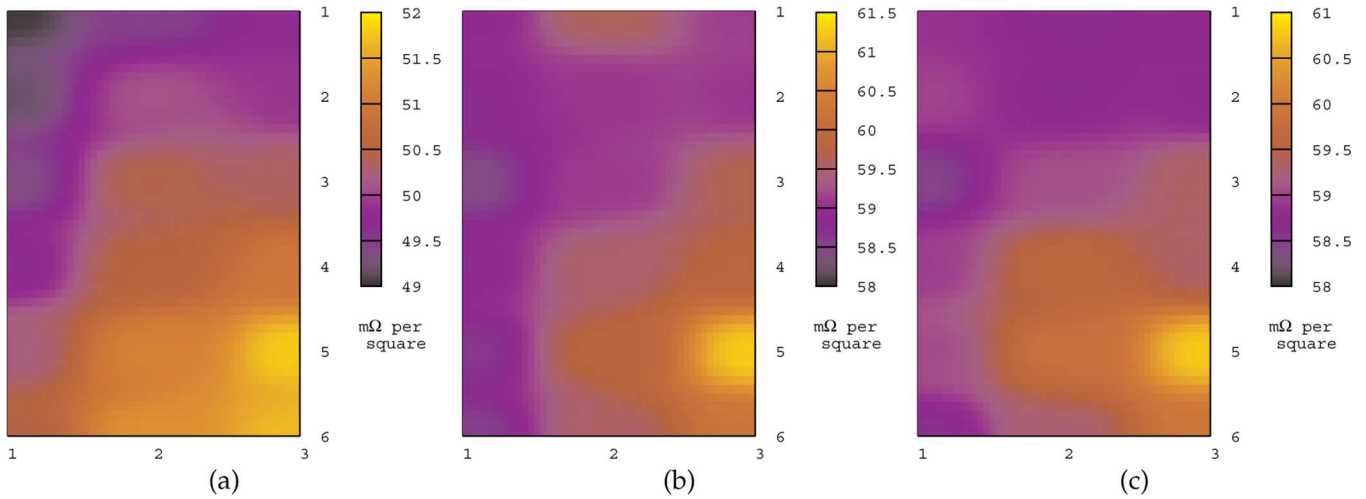

Fig. 5. Contour plot of Rs values over a single die taken from the three van der Pauw structures shown in Fig. 2: (a) Greek cross; (b) corner-tapped box cross; and (c) side-tapped box cross.

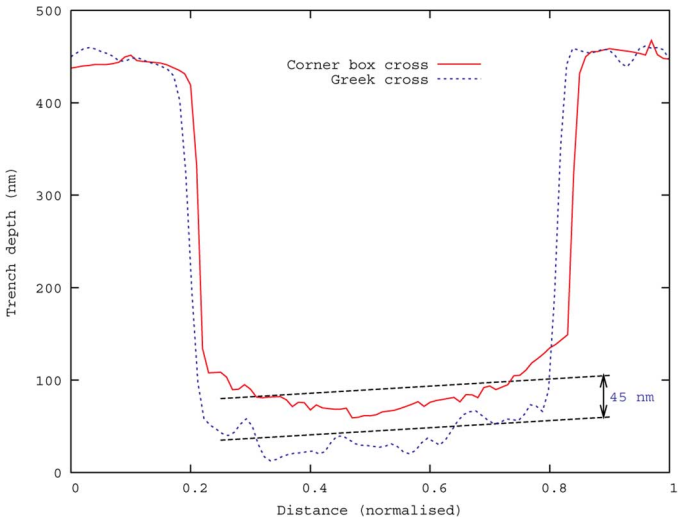

Fig. 6. AFM cross-section plots from the centers of van der Pauw structures after the Cu metal has been etched away.

of the patterned Cu structures differing from the bulk resistivity values reported in literature.

B. Line Width

Line widths have been extracted from electrical measurements from the same six by three array as the sheet resistance measurements, to fully assess the capabilities of the current design on Cu ECD extraction. Results are presented for each of the analysis approaches described in Section III-B. As a means for comparison, scanning electron microscope (SEM) images have been used to provide a value for line width, which in this case is defined by the width of the copper on the surface of the wafer. Each line scan from the SEM was taken at the midpoint of the longest bridge segment of each structure (the 144 μm segment for the long design and the 48 μm segment for the standard design). While the SEM measurements do not produce results to the degree of accuracy required for CD metrology, they do provide a baseline for comparing the analysis methods. For situations where Rs values are required to calculate line width, the average of estimates produced by the two box-cross van der Pauw structures for each location on the die are used. This is because AFM scans reveal that these structures closely match the trench depth of the line width structures. Data from the analysis methods is presented as a graph of drawn line width minus the measured line width versus the drawn line width. This applies for both ECD values as well as SEM line width values. To quantify the degree in which the ECD values agree with the SEM line width values, the sum of the absolute difference between SEM and ECD values for each drawn line width data set has been calculated. This value will be referred to as the *agreement factor*. The ideal instance where the line widths extracted from both methods agree exactly for all drawn line widths would result in an agreement factor of "0".

1) Individual Segment Analysis: The individual segment analysis was conducted as described previously. A plot of the results gathered from the average of five segments of the bridge resistor for the array of 18 structures is presented in Fig. 7. The error bars on the individual data points represent the range of line widths extracted from each segment of the multiple tapped bridge resistor. These errors are proportional to the line width, so, as the line width decreases, the range in extracted values also decreases. The agreement factor for this method was calculated at 5.53. This is justified by the separation between the plotted data sets, especially in the central region of the graph. One source for the difference between the ECD values and the SEM measurements is the use of the sheet resistance structures which are physically separate from the line width structures and subject to dishing effects caused by locality. Furthermore, the van der Pauw structures are 20 μm wide while the line width structures range from 10 μm to 0.55 μm. This introduces further effects of dishing during CMP which are related to feature size.

2) Multiple Segment Analysis: Using the linear regression technique, slope values (m) were determined for each line width structure. With the average measured Rs value from the box

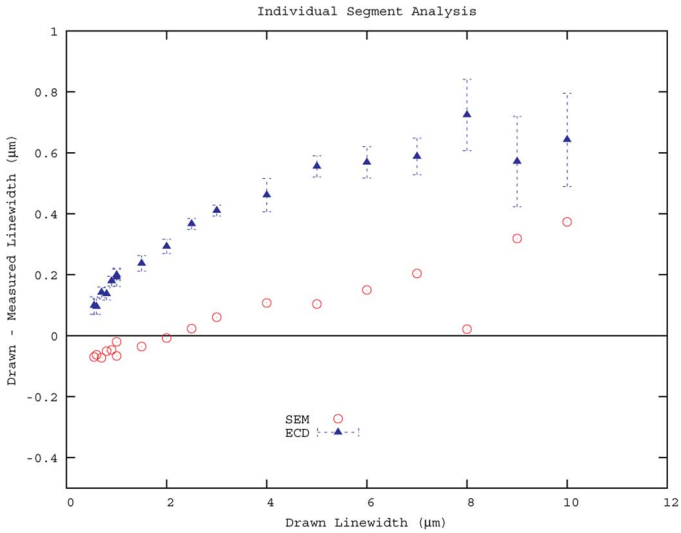

Fig. 7. Plot of drawn line width—measured line width for individual segment analysis.

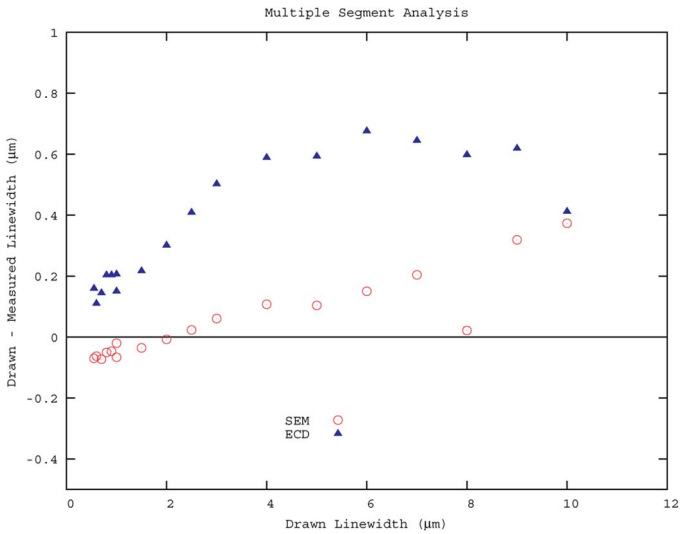

Fig. 8. Plot of drawn line width—measured line width for linear regression analysis.

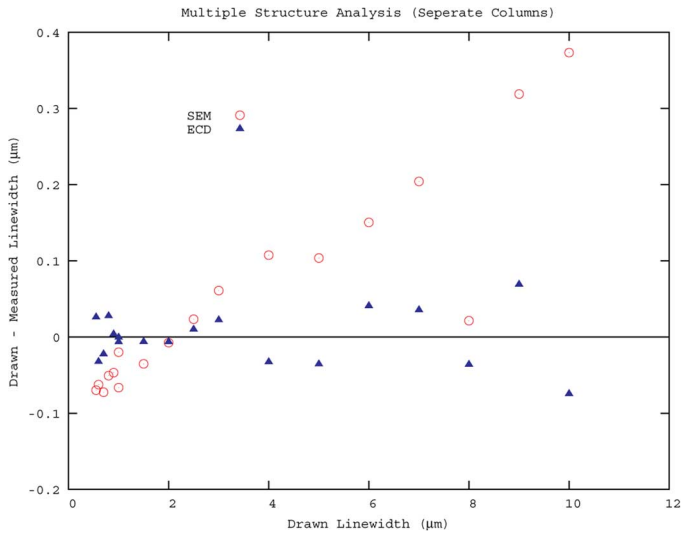

Fig. 9. Plot of drawn line width—measured line width for multiple structure analysis of separate columns.

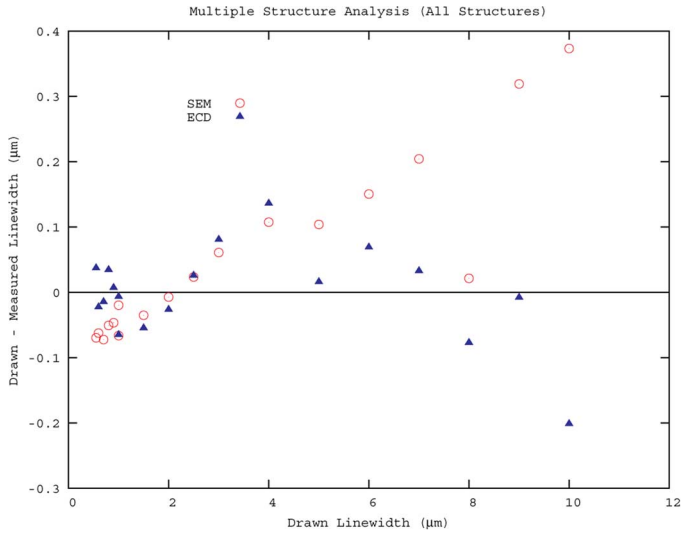

Fig. 10. Plot of drawn line width—measured line width for multiple structure analysis with all structures.

cross structures in closest proximity, the line width was calculated using (6). A plot of the results using this method for all 18 structures is presented in Fig. 8. These values unfortunately do not provide better agreement with the SEM values in comparison to those derived using the individual segment analysis. The agreement factor for this approach is 5.80. Repeating the individual segment analysis with the δL correction makes no improvement with the current set of data.

3) Multiple Structure Analysis: Equation (8) is applied to determine the relationship between the slopes and drawn line widths of the structures in the six by three array. The first approach for this technique was to analyze each column individually and apply the nonlinear regression technique. From Fig. 9 it can be seen that the values extracted for ECD measurements are in better agreement with the drawn line width values. The agreement factor of 1.78 further exemplifies the improvement in values using this method.

The second approach uses data from the entire array to determine the nonlinear relationship and hence can be used as a smoothing for any abnormalities in individual structures. Results from this method are presented in Fig. 10. Once again these data are in agreement with the drawn line widths, providing an agreement factor of 1.79. Observing the graph for this method demonstrates that the closest agreement between SEM and ECD values is seen for drawn line widths ranging from 1 μm to 4 μm. These values correspond to the column of structures that are physically located in the center of the array of the test cell.

In order to comprehend this occurrence, an investigation was conducted to measure the trench depth of the tracks in which the copper was deposited. A select number of the Kelvin bridge

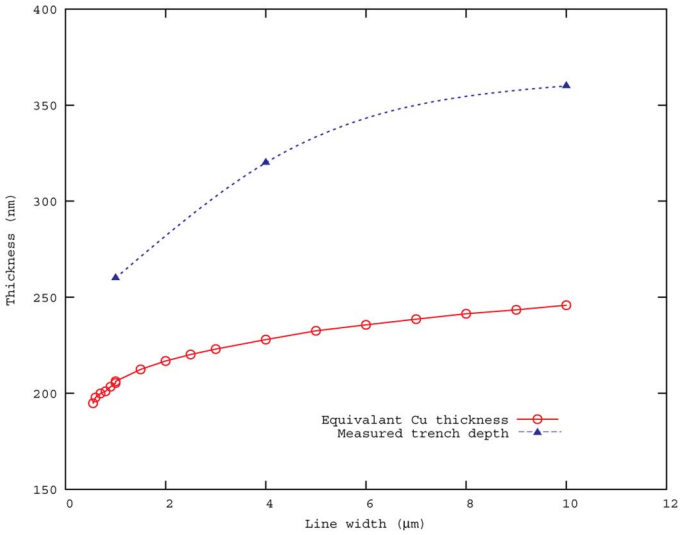

Fig. 11. Plot comparing Cu thickness, as calculated from extracted Rs data (multiple structure analysis), with measured trench depth from the AFM.

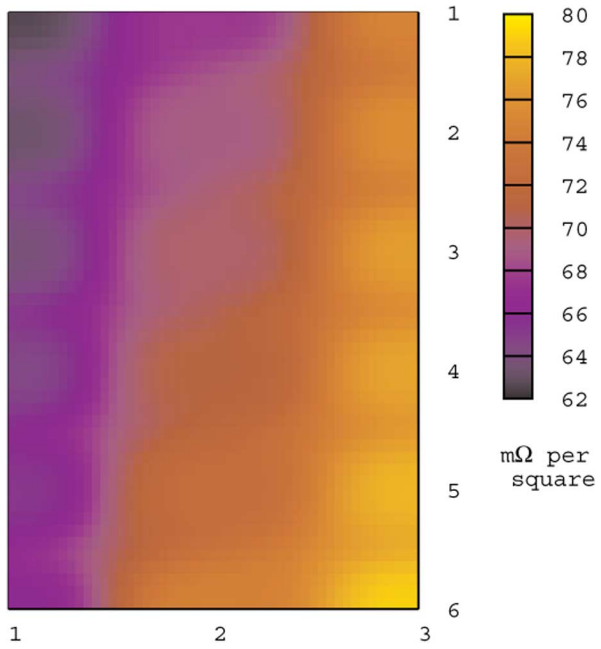

Fig. 12. Contour plot of equivalent Rs values extracted using the multiple structure analysis.

structures were measured with the use of the AFM, after the Cu was etched away. The results highlighted the fact that the depth of the etched trench was dependant on the line width of the initial silicon preform, where wider line widths result in deeper trenches, as demonstrated in Fig. 11. These deeper trenches translate to lower sheet resistance when filled with the Cu metal. In this graph, the difference between equivalent and measured values is believed to be due to the resistivity value of the deposited Cu differing from the reported bulk resistivity values combined with Cu dishing, which varies according to line width.

This explains why using all the columns in the multiple structure analysis provides the set of results which best agrees with the SEM measured data. Column 2 (central column) contains structures which posess line widths in the middle of the measured range. Column 1 contains line widths greater than the central column, and column 3 contains those structures with line widths less than column 2. Furthermore, the rows are arranged such that drawn line widths of the structures decrease from top to bottom (row 1 to 6). As the multiple structure analysis method calculates the effective sheet resistance value based on the relationship of the measured slope (m) values for the full set of structures, the most accurate values for Rs will be found in the center of the measured range due to the influence of the extreme data points. Therefore, it can be deduced that the outer columns (1 and 3) provide an averaging effect which results in the central column having the most accurate extracted line widths.

To understand the effect of line width on the Rs values as determined by the multiple structure analysis and provide a means for comparison to Rs values extracted from the van der Pauw structures, the equivalent Rs values for the full array are presented in Fig. 12. They are calculated by substituting the measured ECD values from this last analysis approach into (6). These data suggest a more smooth gradient in the variation of sheet resistance across the die. This supports the earlier conclusion that the line width directly affects the trench depth of the structures, where the decreasing line width translates to increasing sheet resistance of the Cu track.

V. Conclusion

Structures have been fabricated using a novel process to produce all-copper ECD test structures. Electrical measurements have been taken to extract values for sheet resistance and line width. Based on data gathered from extensive electrical measurements of the Cu interconnect features, issues with the current design as well as the fabrication process have been highlighted. In light of the diverse range of values for sheet resistance, the need to control the dishing of the Cu has become much more critical. This can be achieved with the combination of different CMP slurries and polishing pads, as well as improvements to the process recipes. Dishing of Cu lines is a well-known phenomenon amongst the semiconductor community, and much work is ongoing to improve this aspect of copper CMP. The more predominant factor affecting measured values is the trench depth as a result of the trench etch stage. The Greek cross structure was found to have a consistently deeper trench than the box cross structures. Furthermore, a correlation between line width and trench depth has been found. Future work is required to optimize the trench etch stage of the fabrication process to produce more consistent results.

The work conducted for the purposes of this paper has highlighted an approach to analysing the data from all-copper test structures which yields the best results. Future process improvements can be closely monitored to observe their effect on the extraction of ECD values. Ongoing work will involve the use of more precise CD measurement tools to determine the line width of the copper interconnects and serve as calibration/reference values for more in depth analysis of the presented techniques. For the purpose of this exploratory work, g-line lithography was

used to define the pattern. However more advanced technologies, such as i-line, e-beam, and deep UV (DUV) lithography, can be employed to print much smaller features. Analysis of these smaller features will bring the work in line with current roadmap predictions for Cu ECD values.

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REFERENCES

[1] M. W. Cresswell, N. Arora, R. A. Allen, C. E. Murabito, C. Richter, A. Gupta, L. W. Linholm, D. Pachura, and P. Bendix, "Test chip for electrical linewidth of copper-interconnect features and related parameters," in *Proc. IEEE Int. Conf. Microelectronic Test Structures (ICMTS'01)*, Mar. 2001, vol. 14, pp. 183–188.

[2] T. Turner, "Requirements for dual-damascene Cu-linewidth resistivity measurements," *Solid State Technol.*, vol. 43, no. 4, pp. 89–94, Apr. 2000.

[3] S. Smith, A. J. Walton, A. W. S. Ross, G. K. H. Bodammer, and J. T. M. Stevenson, "Evaluation of sheet resistance and electrical linewidth measurement techniques for copper damascene interonnect," *Solid State Technol.*, vol. 15, no. 2, pp. 214–222, May 2002.

[4] B. J. R. Shulver, A. S. Bunting, A. M. Gundlach, L. I. Haworth, A. W. S. Ross, A. J. Snell, J. T. M. Stevenson, A. J. Walton, R. A. Allen, and M. W. Cresswell, "Design and fabrication of a copper test structure for use as an electrical critical dimension reference," in *Proc. IEEE Int. Conf. Microelectronic Test Structures (ICMTS'06)*, Mar. 6–9, 2006, pp. 124–129.

[5] R. A. Allen, B. A. Ende, M. W. Cresswell, C. E. Murabito, T. J. Headley, W. F. Gutherie, L. W. Linholm, C. H. Ellenwood, and E. H. Bogardus, "Test structures for referencing electrical linewidth measurements to silicon lattice parameters using hrtem," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 2, pp. 239–248, May 2003.

[6] R. A. Allen, T. J. Headley, S. C. Everist, R. Ghoshtagore, M. W. Cresswell, and L. W. Linholm, "High-resolution transmission electron microscopy calibration of critical dimension (CD) reference materials," *IEEE Trans. Semicond. Manuf.*, vol. 14, no. 1, pp. 26–31, Feb. 2001.

[7] T. Hatsuzawa and K. Toyoda, "Critical dimension measurements by electron and optical beams for the establishment of linewidth standards," in *Proc. IEEE 1992 Int. Microelectronic Test Structures*, Mar. 1992, vol. 5, pp. 180–184.

[8] R. A. Allen, M. W. Cresswell, and L. W. Linholm, "Junction-isolated electrical test structures for critical dimension calibration standards," *IEEE Trans. Semicond. Manuf.*, vol. 17, no. 2, pp. 79–83, May 2004.

[9] M. W. Cresswell, W. F. Guthrie, R. G. Dixson, R. A. Allen, C. E. Murabito, and J. V. Martinez, "Rm 8111: development of a prototype linewidth standard," *J. Res. Nat. Inst. Standards and Technol.*, vol. 111, pp. 187–203, 2006.

[10] M. W. Cresswell and R. A. Allen, *Handbook of Silicon Semiconductor Metrology*. New York: Marcel Dekker, 2001, pp. 377–410.

[11] L. J. Van Der Pauw, "A method of measuring specific resistivity and hall effects of discs of arbitrary shape," *Phillips Res. Rep.*, vol. 13, pp. 1–9, 1958.

[12] M. W. Cresswell, J. J. Sniegowski, R. N. Ghoshtagore, R. A. Allen, W. F. Guthrie, A. Gurnell, L. W. Linholm, R. G. Dixson, and E. C. Teague, "Recent developments in electrical linewidth and overlay metrology for integrated circuit fabrication processes," *Jpn. J. Appl. Phys.*, vol. 35, pp. 6597–6609, 1996.

[13] R. A. Allen, M. W. Cresswell, and L. M. Buck, "A new test structure for the electrical measurement of the width of short features with arbitrarily wide voltage taps," *IEEE Electron Device Lett.*, vol. 13, no. 6, pp. 322–324, Jun. 1992.

[14] M. W. Cresswell, R. A. Allen, and L. W. Linholm, "Linewidth Micro-Bridge Test Structure," , 1993.

[15] , D. Lide, Ed., *Handbook of Chemistry and Physics*, 80th ed. Boca Raton, FL: CRC, 1999.

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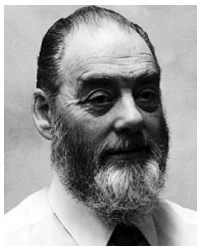

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