Internal Photoemission Spectroscopy of Metal Gate / High-*k* / Semiconductor Interfaces

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Abstract. Internal photoemission (IPE) spectroscopy is a powerful technique for investigating electronic properties of inhomogeneous interfaces of hetero-structures. Two of the most important aspects of IPE measurements involve threshold spectroscopy and photoelectron yield spectroscopy. In the first measurement type, IPE is used to determine the barrier heights at the interfaces while the second deals with photoemission of carriers (electrons and holes) with the energies above and below the barrier. We will present a brief description of the IPE principle upon which the extraction of the interfacial energy thresholds or barrier heights is based. The details of our IPE experiment setup will be also presented. For applications, in this report we will focus mainly on the first aspect of IPE where we determine the barrier heights of a technologically important class of materials which includes various metal-high-k insulator-semiconductor structures.

Keywords: Internal photoemission, high-k dielectric, metal oxide semiconductor
PACS: 73.40.Qv, 73.40.-c, 73.43.Fj, 73.90

INTRODUCTION

Electrical and electronic properties at solid/solid interfaces have always been of great interest to the device physics and integrated circuit design communities. One of the more important parameters that needs to be known and/or controlled in order to design high performance electronic devices is the electron and hole barrier heights at the interfaces. In particular for the field of complementary metal oxide semiconductor (CMOS), there has been very active investigation and research to find new materials to replace the traditional poly-Si gate / SiO_2 / Si structure of the basic MOS for the next generations of CMOS. As the gate lengths of the metal-oxide-semiconductor field-effect transistor (MOSFET) are reduced to 50 nm and below, a number of performance issues such as high leakage current and *poly*-Si electrode depletion are encountered. To circumvent these problems, both SiO_2 and *poly*-Si gate needs to be replaced with appropriate high-k dielectrics and metal gates. To select the right materials, one of the crucial electronic parameters is the band offsets at their interfaces which greatly affect electrical performance. For instance, in an extensive study, Schaeffer *et al.*[1] have shown that the optimal gate work functions (which relate to the barrier heights or band offsets) for the sub 50 nm channel lengths should be 0.2 eV below (above) the conduction band edged of silicon for n-type MOSETs (p-type MOSFETs).

Internal photoemission is a simple yet powerful technique for characterizing electronic properties of solid-solid interfaces, in particular those of insulator/semiconductor and a metal/insulator. It involves photo-excitation of electrons or holes over the interface barrier. The onset of the conduction of these photoemission carriers under an electric field determines the barrier heights as well as electronic characteristics at the interface. For a MOS structure, the barrier heights are shown schematically in the energy band diagram in Figure 1. Φ_e^{metal} and Φ_e^{semi} are the barrier heights for electrons making transition from the metal Fermi level and the top valence band of the semiconductor to the bottom conduction band of the insulator, respectively. For the hole carriers, Φ_h^{metal} and Φ_h^{semi} are the barrier height from the metal Fermi level and the bottom conduction band of semiconductor to the top conduction band of the insulator, respectively. In all, IPE may provide band offsets and alignments which are very important parameters to determine the performance of the corresponding devices.

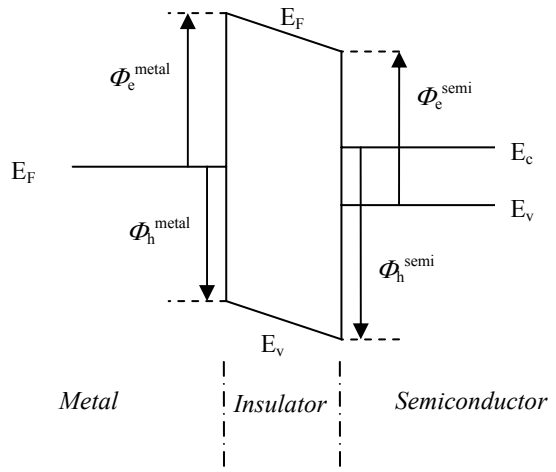

FIGURE 1. Band offset and barrier heights of a metal oxide semiconductor (MOS) device.

In this report, we briefly describe the principle as well as the experiment setup of IPE used in our study. Measurements and analysis performed on a variety of technologically relevant materials will be presented.

INTERNAL PHOTOEMISSION

Internal photoemission is defined as a process where photon-stimulated charge carriers (electron or hole) make a transition from one component of hetero-structure to another over the barrier height at their interface. In effect, the process involves a photogenerating carriers in the solid, transporting them to the interface, and supplying efficient energy for them to escape over the barriers to become carriers in the second solid.[2] To accomplish the described process, the structure is illuminated through a semitransparent thin metal deposited on the insulator, and an external bias (V) is applied between the electrode and the semiconductor substrate. The photocurrent (I) is measured as shown in Figure 2. In order for the photoemission current yield to be correctly measured, the carrier trap density should be sufficiently small as to not distort the electric field. In other words, the insulator thickness should be comparable to or less than the mean free path length of the carriers.

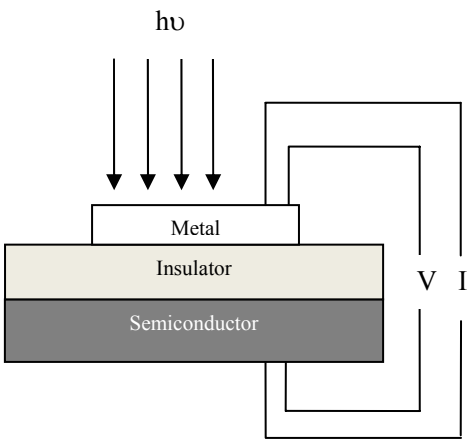

FIGURE 2. IPE experimental setup

To model the photoemission process, the optical excitation and transport processes are characterized by the energy distribution function of the photoemission carriers *N(E)* where *E* the carrier energy. The escape over the barrier can be represented by the probability *P(E)* established by the well-known Fowler conditions which expresse *P(E)* in terms of the excited carrier momentum.[3] Since, near the interface, the translation symmetry is broken, the momentum and energy relation cannot be given. However, in experiments, the photon excitation is specified by the photon energy; therefore it is more desirable to express it in terms of energy. Fowler has shown that under the relaxation of the momentum conservation condition, $P(E_n)$ at the interface can be expressed as:

$$\begin{aligned} P(E_n) &= 1 \quad \text{if} \quad E_n > \Phi \\ &= 0 \quad \text{if} \quad E_n < \Phi \end{aligned} \qquad (1)$$

where Φ is the barrier height or threshold energy and E_n is the electron energy. The momentum conservation requirement can be excluded since the insulator used in MOS devices is commonly an amorphous material. In terms of the total electron energy E, the escape probability is the following:

$$\begin{aligned} P(E) &= D(E-\Phi)\alpha \quad \text{if } E > \Phi \\ &= 0 \quad \text{if } E < \Phi \end{aligned} \qquad (2)$$

where D is a constant and α is related to the carrier distribution function. In IPE, the measured quantity is the quantum yield Y which is an integration of the product of carrier escape probability and energy distribution for all carriers having energies above the unexcited level to the excitation photon energy hυ:

$$Y(h\upsilon) = \int_0^{h\upsilon} N(E)P(E)dE. \qquad (3)$$

In the vicinity of the photoemission threshold Φ, $N(E)$ can be written as:

$$N(E) = A\,(h\upsilon - E)^b \qquad (4)$$

where the exponential b is related to the energy distribution of empty and filled states, the optical transition type, and the scattering of the excited carriers. For the simplest case of a = 1, from (2) and (4) the quantum yield (3) can be written in the following simple form:[4]

$$Y(h\upsilon) = A(h\upsilon)\,[h\upsilon - \Phi]^p. \qquad (5)$$

As it turns out, for the metal/insulator interface, for excitation photon energy near and above Φ, Y has been found to have cubic dependency i. e., $p = 2$, whereas for the semiconductor/insulator interface, $p = 3$. Thus, Φ can be experimentally determined by linear extrapolation of the measured $Y^{1/2}$ and $Y^{1/3}$ to zero yield.[4]

An electric field exists in the insulator due to the work function difference of the metal and semiconductor and the external field applied between the metal and the semiconductor under a bias. Such electric field lowers the barrier height. This is known as the Schottky effect, which is the image-force induced lowering of the potential energy for charge carrier emission when an electric field is applied. Consider the metal/insulator interface as shown in Figure 3. The zero-field energy for the electron to escape into the insulator is the energy distance, i.e. Φ_0, from the Fermi level of the metal to the bottom of the insulator conduction band bottom. When an electron is at a distance x from the metal, a positive charge will be induced on the metal surface. The attraction force is equivalent to the force that would exist between the electron and an equal positive charge located at –x, which is referred to as the image charge.[5] The attractive force (i.e., the image force) gives rise to a simple potential energy given by

$$\phi_{image} = -q^2 / 8\pi\varepsilon_0\varepsilon_i x \qquad (6)$$

where ε_0 and ε_i are the permittivity of free space and the relative optical permittivity of the insulator, respectively. With an externally applied field, the total potential energy is given by the sum of image potential energy Φ_{image} (curve b) and the potential energy of an externally applied field (curve a). It can be shown that the barrier height is written in terms of the electric field F in the insulator as:[2]

$$\phi(F) = \phi_0 - q\sqrt{\frac{qF}{4\pi\varepsilon_0\varepsilon_i}}\ . \qquad (7)$$

It is obvious from equation (6) that the barrier height decreases when the electric field F increases. Therefore, the zero-field barrier height Φ_0 is determined from the relation F vs. $\sqrt{F}$ plot when F =0.

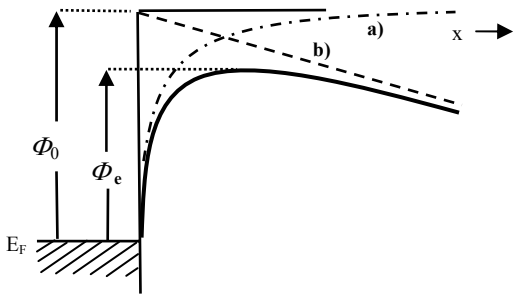

FIGURE 3. Field effects on the barrier height.

Experimental Setup

The IPE experimental setup used in this study is schematically displayed in Figure 4.

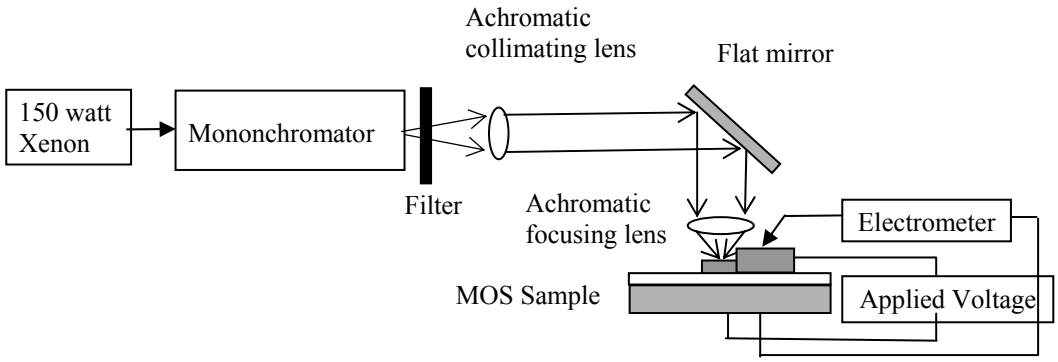

FIGURE 4. Schematic setup of an internal photoemission system.

A 150 watt broadband Xenon light source is used in junction with a grating monochromator to provide a spectral range from 1.5 eV to 6.0 eV. High order dispersion is filtered out with two long pass filters. Light from the monochromator is collimated by an achromatic UV grade lens and then focused down to a millimeter size spot on the metal electrode surface of a MOS device by another achromatic UV lens. The bias applied across the MOS capacitor is supplied by a regulated power supply, and the current is recorded by an electrometer as the light is scanned at different photon energies. The quantum yield (Y) is obtained through the measured current *I* by

$$I = PY / h\upsilon \qquad (8)$$

where *I* is the current in amperes, *P* the absorbed light power in watts, $h\upsilon$ the photon energy in electron volts, and *Y* the yield in electrons/photon. For simplicity, the light incident at the surface is used and measured by a calibrated silicon diode right at the focal point of the second lens in Figure 4. All the measured currents are corrected for stray light incident on the sample and possible tunneling and background noise current. Normal operation is usually done by measuring photocurrent as function of the incident photon at an applied bias, then repeated for wide range of biases where the tunnel currents are minimal.

INTERNAL PHOTOEMISSION APPLICATIONS TO METAL GATE/HIGH-*K*/SEMICONDUCTOR INTERFACES

In the rest of this article, we will demonstrate the application of IPE to a number of material systems that have a great practical interest for the IC industry, which is in the search for the new materials to replace conventional CMOS.

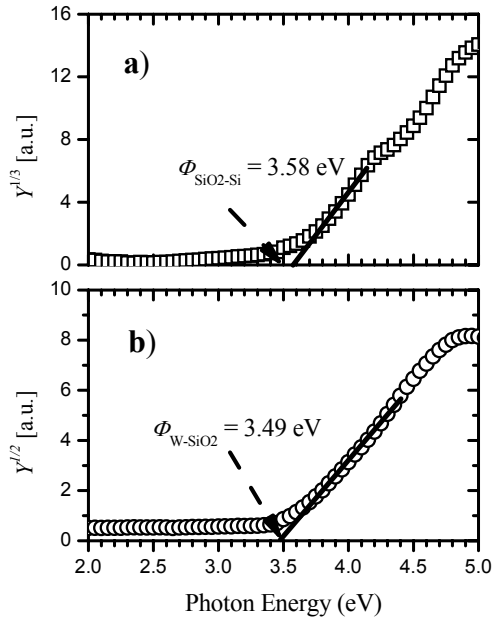

FIGURE 5. Cube root (a) and square root (b) of IPE yield as function of photon energy for W(15nm) / SiO_2 (4nm) / Si structure when Si substrate was biased at -2.0 volts and +1.0 volt, respectively.

W / SiO_2 / Si SYSTEM

To begin, as an example of metal on traditional SiO_2 insulator of an MOS structure, Figures 5a and 5b show IPE yield from a capacitor consisting of a stack of thin (15 nm) tungsten deposited on top of a 4 nm SiO_2 on Si substrate. Photoemission displayed in Figure 5a is a result of IPE of electrons from silicon to SiO_2 when a -2.0 volt bias was applied to the silicon substrate. Since the silicon was not heavily doped,

these electrons originated from the silicon valence band and escaped over the barrier into the SiO_2 conduction band. Thus, the IPE threshold from the Si top valence band to the SiO_2 bottom conduction band was extracted by extrapolating $Y^{1/3}$ to zero yield as shown by the straight solid line, which gives a barrier of 3.58 eV. When a +1 volt bias is applied, $\Phi = 3.49$ eV corresponding to the barrier between the tungsten Fermi level and the SiO_2 bottom conduction band. The same measurement and barrier height determination were performed when the silicon substrate was biased from -3 volts to +2 volts in steps of 0.2 volt. The determined barrier heights were then plotted in the form of Schottky plot (see equation 7) as a function of the square root of the electric field in the SiO_2 layer. As seen in Figure 6, the barrier height is reduced as the electric field in the SiO_2 increases as a result of the image force discussed above. A linear fit to the Schottky plot results in zero-field barrier height when the field is set to zero. We thus obtain $\Phi_{SiO2\text{-}Si}$ = 4.33 eV and $\Phi_{W\text{-}SiO2}$ = 3.82 eV. Above 1.5 MV $^{1/2}$/cm$^{1/2}$, the Schottky plot for the Si-SiO_2 barrier height shows an additional reduction of the barrier height from the image force model at higher field. Such deviation from the linear dependency of Φ on $F^{1/2}$ (equation 7) may be due to the penetration of the electric field in SiO_2 into the silicon substrate causing an additional potential drop within the photoelectron escape depth.[2]

The barrier height at the SiO_2 and Si interface determined by our IPE measurement agrees well with the reported value of 4.25 eV. At the W and SiO_2 interface, with the known SiO_2 electron affinity of 0.91 eV, the work function of W becomes 4.71 eV which agrees with reported value of 4.6 eV to 4.7 eV from Fowler-Norheim tunneling.[5]

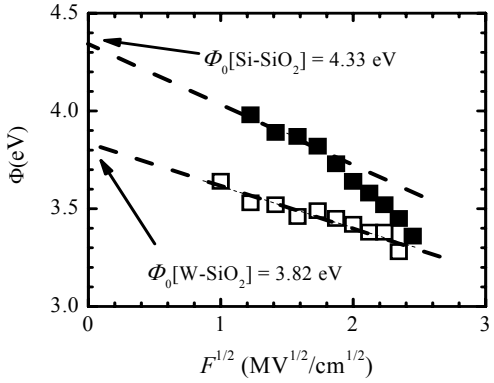

FIGURE 6. Schottky plot of barrier height as a function of square root of electric field in the SiO_2 insulator of W(15nm) / SiO_2 (4nm) / Si structure.

Al / HfO_2 / Si SYSTEM

High-k HfO_2 dielectric has been a focus of extensive research for a SiO_2 replacement. The barrier heights between metal gate and HfO_2 need to be known and tuned to an optimal value. In the following, IPE was performed on a MOS structure consisting of a 12 nm Al gate deposited on a 20 nm HfO_2 insulator, and a silicon substrate. HfO_2 was grown by atomic layer deposition. Figures 7a and 7b depict the IPE yield measured when the silicon was biased at +1.8 volts and -1.4 volts, respectively. The spectral curve in Figure 7a indicates the spectral threshold of 2.4 eV for an electron transition from the aluminum Fermi level to the conduction band of HfO_2 at 1.8 V. An increase in yield at 5.6 eV is a result of optical excitation of electrons in bulk HfO_2 from the valence band to conduction band corresponding to the HfO_2 band gap as indicated by E_g (HfO_2) in the figure.

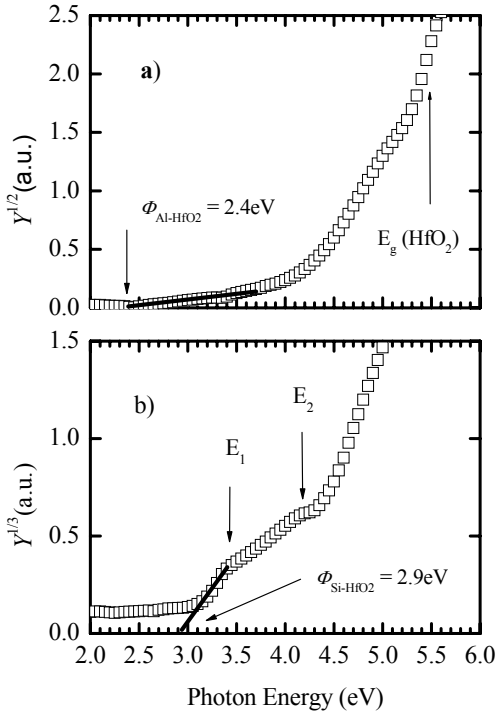

FIGURE 7. Cube root (a) and square root (b) of IPE yield as function of photon energy for Al(15nm) / HfO_2 (20nm) / Si structure when Si substrate was biased at 1.8 volts and -1.4 volt, respectively.

When the silicon substrate was negatively biased at 1.4 volt, the cube root yield shown in Figure 7b indicates a spectral threshold of 2.9 eV for electrons making the transition from the top silicon valence band to the bottom conduction band of HfO_2. In

addition, the spectral slope changes seen at 3.4 eV and 4.2 eV are due to the excitation of interband transitions E_1 and E_2 in silicon, respectively. The Schottky plots are shown in Figure 8 as a function of electric field in the HfO_2 layer. The zero-field barrier heights obtained from a linear fitting are 3.11 eV and 2.56 eV for the Al-HfO_2 and Si-HfO_2 interfaces, respectively. Both values are in a good agreement with the literature.[7] The field dependence of the Al-HfO_2 barrier height appears to be relatively weak compared with that of the same metal on SiO_2. This is because the barrier height reduction due to the image force is inversely proportional to the square root of the insulator permittivity as indicated in equation (7), and HfO_2 has a higher permittivity than that of SiO_2.

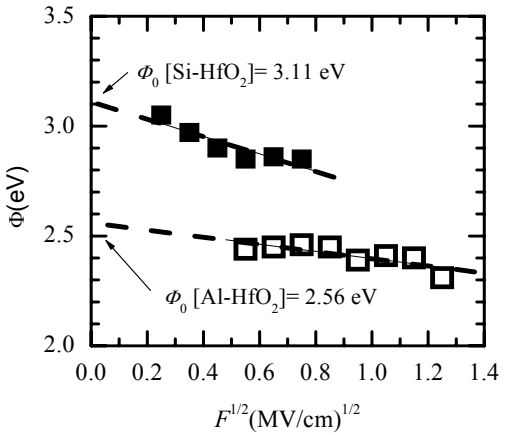

FIGURE 8. Schottky plot of barrier height as a function of square root of electric field in the SiO_2 insulator of an Al(12nm) / HfO_2 (20nm) / Si structure.

Al / Al_2O_3 / GaAs SYSTEM

Recently a new interest has shifted to high-k dielectrics on III-V compound semiconductors. Figure 9a displays a cube root IPE yield obtained from a capacitor consisting of 12 nm Al on a 10 nm Al_2O_3 on a GaAs substrate (biased at -1.0 V). A spectral threshold of 3.2 eV was extracted when the GaAs substrate was negatively biased at 1 vold. Similar to the case of silicon substrate, the E_2 optical excitation in the GaAs substrate is observed at ~ 4.5 eV as indicated in Figure 9. The zero-field barrier height from the GaAs top valence band to the Al_2O_3 bottom conduction band was determined to be 4.5 eV from the Schottky plots shown in Figure 10.

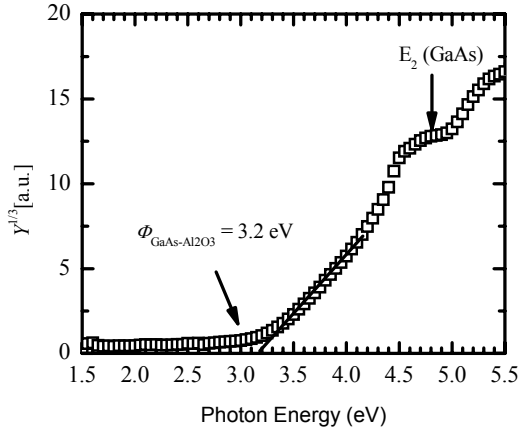

FIGURE 9. Cube root of IPE yield as function of photon energy for an Al (12nm) / Al_2O_3 (10nm) / GaAs structure when the GaAs substrate was biased at -1.0 volt.

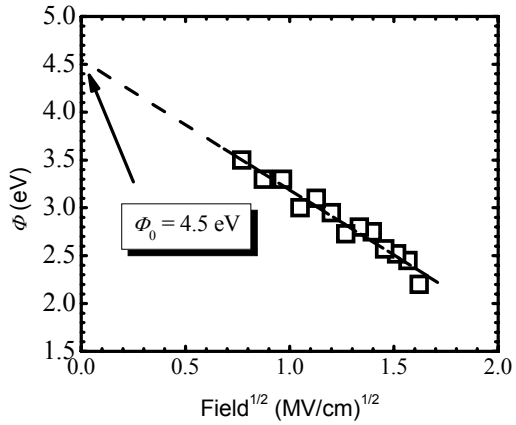

FIGURE 10. Schottky plot of barrier height as a function of square root of electric field in the Al_2O_3 insulator of an Al (12nm) / Al_2O_3 (10nm) / GaAs structure.

SUMMARY AND CONCLUSIONS

We have described the principle of the internal photoemission (IPE) technique and the experimental setup, and illustrated the applications of this technique to a few technologically important metal oxide semiconductor structures. We have shown how the barrier heights at metal/oxide and oxide/semiconductor interfaces were experimentally determined. Special photoexcitation features in IPE spectra were also uncovered and discussed. For the demonstration of the IPEs applications, IPE measurements were performed on an important material system of high-k dielectrics as insulators and both silicon and gallium arsenide as substrates.

In this report, the internal photoemission (IPE) was applied mainly as an interface threshold spectroscopy technique. Other IPE capabilities have been demonstrated in the past, which were based on the barrier distortion by defects (fixed charges, carrier scattering, charge trapping) in the insulator layer.[2] Therefore, as a simple and straightforward technique without much modeling involved, IPE should be a unique and useful tool for electronic interface characterization. Especially, as the electronic devices are being scaled down to nanometer dimension, the interface properties become an immense factor in determining their performance. It is thus expected that IPE will be an indispensable metrology tool for characterizing nanometer structures and devices for the semiconductor industry.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the NIST Office of Microelectronics Programs for their support and the following collaborators: James Maslar and William Kimes, of NIST, and Niti Goel and Kwan-Woo Choi, of INTEL, for providing the materials and useful discussions.

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