Experimental Evaluation of SiC PiN Diode Forward Bias Degradation and Long Term Stability*

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Abstract- **New automated measurement systems and test procedures are presented that enable the evaluation of long-term stability of SiC PiN diodes. Long-term stability results are presented for 10 kV SiC PiN diodes that are made using a new fabrication technology developed to eliminate the source of the degradation. The major objectives of the long-term stability test procedures are to monitor the forward on-state voltage degradation and current area reduction for different forward bias stress levels. Three experimental systems have been used to perform the long-term stability study. Results show that it is possible for SiC diodes to perform acceptably after over 2000 hours of forward bias stress time.**

I. INTRODUCTION

The silicon carbide (SiC) industry is developing SiC power devices that are better suited than silicon (Si) power devices to operate at voltages over 10 kV. For high-voltages, minority carrier device types such as PiN diodes, BJTs, IGBTs, and GTOs have the best performance. Nonetheless, SiC minority carrier device types have been shown to be susceptible to degradation of the on-state voltage (V_f) when subjected to forward conduction stress. In general, the V_f degradation is caused by SiC crystal stacking fault propagation, which has been studied in more detail in [1].

Recently, a new fabrication process has been introduced that promises to eliminate this degradation mechanism [2] by producing high voltage blocking layers that are free of the nucleation sites that result in stacking fault propagation. The purpose of this work is to present new test systems and procedures to assess the long-term stability of SiC PiN diodes made using this new fabrication process, including V_f and conduction area reduction monitoring at various levels of forward bias stress. The test systems and procedures discussed in this work can also be used to evaluate other minority carrier device types such as BJTs, IGBTs, and GTOs.

II. FULL DEGRADATION SYSTEM

In this study, three experimental setups are used to evaluate forward bias degradation and long term stability of SiC PiN diodes: 1) a pulsed degradation and monitoring system, 2) a multi-channel continuous long-term degradation system, and 3) a pulsed high-speed transient thermal current uniformity measurement system.

A. Pulsed Degradation and Monitoring System

The procedure used to evaluate the forward bias stability begins by characterizing the devices for the initial value of V_f. This is done by using a pulsed degradation and monitoring system [1]. Fig. 1 shows the test system configuration for this measurement system, including the LabWindows/CVI[1] front panel user interface needed to control the hardware from the computer. The V_f characterization is performed under pulsed conditions to minimize stress and enable precise control of the chip surface temperature. This temperature is maintained using a temperature-controlled test fixture at the package case (or base-plate), and the forward bias pulse width is kept low enough so that self-heating of the device does not occur.

After the initial V_f measurement is made, an initial current uniformity image is obtained using a pulsed high-speed thermal imaging system, described below. Because the thermal imaging technique itself results in some stress on the device, the device is again characterized for V_f using the pulse forward bias monitoring system described earlier. The device is then subjected to various levels of forward bias stress and periodically monitored for V_f and conduction area degradation.

The test procedure requires degradation times to vary initially from a few seconds up to several hours or even months, as necessary. The criterion used to increase the stress time as the test progresses is to monitor the level of V_f and area reduction stability for close-to-steady behavior. When these monitored quantities do not change appreciably (typically less than 20 mV), the stress interval is increased (typically doubled).

B. Multi-Channel Long-Term Degradation System

The pulsed degradation system described above is used for the initial short periods of time where the temperature is maintained relatively constant using a short pulse (0.1 s) with low duty cycle (1 %). In order to test higher levels of stress, maintaining the 1 % duty cycle significantly increases the time required to impose the stress on the device. Therefore, the continuous current long-term degradation system is instead used for the higher levels of stress.

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[1] LabWindows/CVI is a trademark of National Instruments. Certain commercial products have been identified in order to describe the subject matter of this paper adequately; this does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products are the best for the purpose.

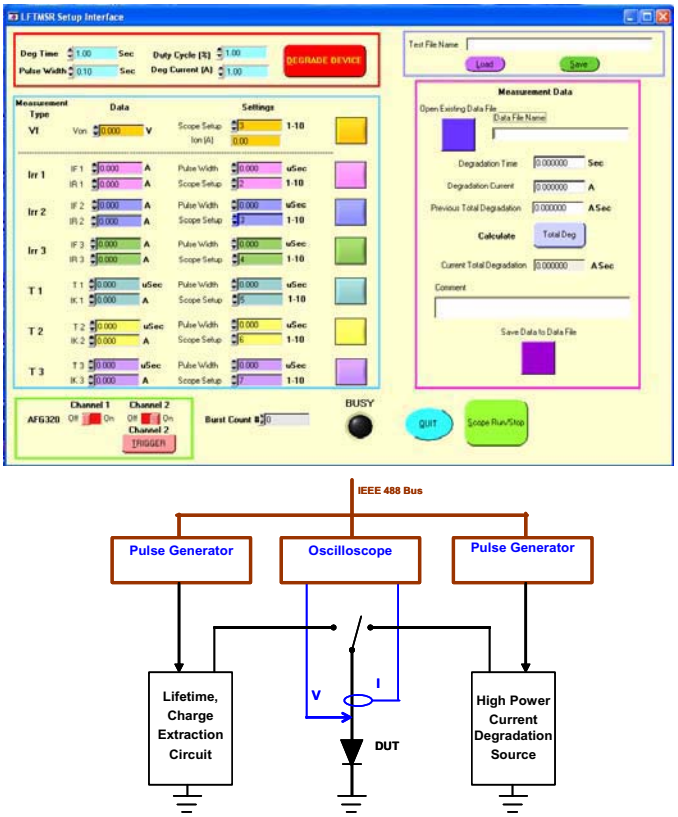

Figure 1. Pulsed Degradation and Monitoring System.

Fig. 2 shows the (a) hardware configuration and (b) computer user interface for the multi-channel, long-term degradation system. In this system, the header (or base-plate) of the package is maintained at a fixed temperature using a water-chilled heat sink arrangement. The chip surface is initially heated to a higher temperature due to its own package thermal resistance. The self-heating occurs in less than a minute, and then the device stabilizes at a relatively constant temperature.

The hardware of Fig. 2a includes a multi-channel temperature measurement system to monitor the heatsink and chilled water supply temperatures, and multiple programmable source-measurement power supplies to provide constant current to each device under test (DUT). The LabWindows/CVI user interface in Fig. 2b is used to input the stress current level, and to display the monitored quantities for each DUT. The program records the monitored quantities and degradation time for each DUT in a log file at intervals determined by the user specified time, voltage, and temperature increments.

C. Pulsed High-Speed Transient Thermal Current Uniformity Measurement System

The current uniformity measurements are obtained using the high-speed transient thermal imaging system described in [3]. Fig. 3 shows the computer user interface and hardware configuration for this system.

Each image is taken at 398 µs after the heating pulse is applied. To do this, a 1 ms heating current pulse is applied to

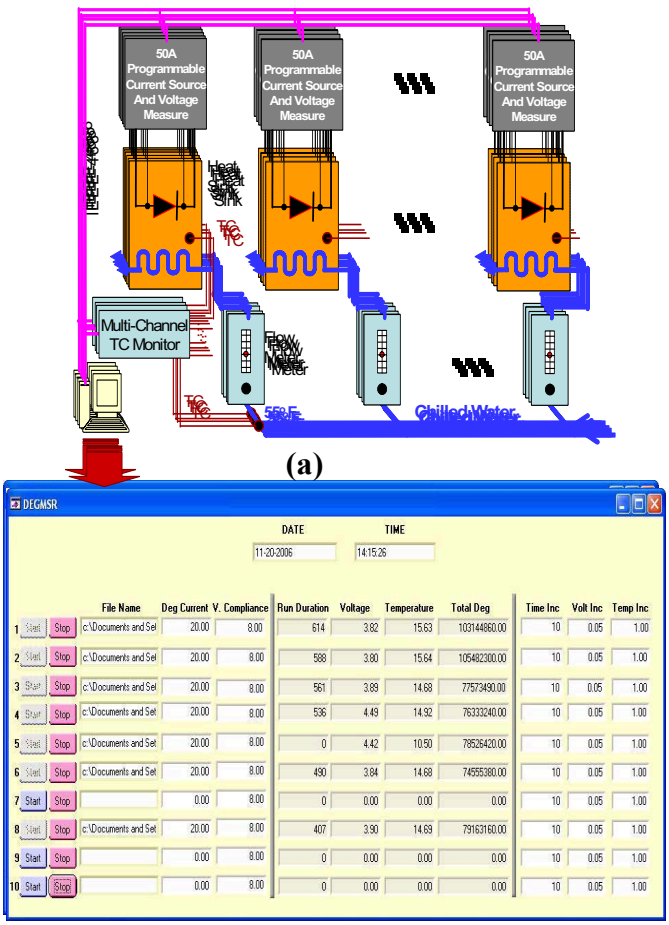

Figure 2. Multi-Channel Long Term Degradation System: (a) experimental setup, (b) front panel user interface.

the device under test at a frequency of 10 Hz (duty cycle of 1 %) with an amplitude of 20 A. The device is mounted on a temperature-controlled heat sink and held at an elevated temperature of 75 ºC to increase the infrared signal level. The devices are also coated with a thin, black, high-electrical-resistance film to improve emissivity. In general, areas showing the lower temperatures at 398 µs after the heating pulse is applied are equivalent to areas of no current conduction, except where an obstruction such as a wire bond exists.

III. Degradation Evaluation Summary

Fig. 4 shows the current voltage characteristics of a PiN diode indicating that the forward voltage at a given current increases with time as the device degrades. For the following degradation monitoring, V_f is recorded at 100 A/cm^2 which is near the normal current density range for 10 kV SiC PiN diodes. For the results presented in this paper, long-term degradation experiments were performed on numerous diodes where approximately twelve current uniformity images were taken at logarithmically spaced time intervals as the device degraded.

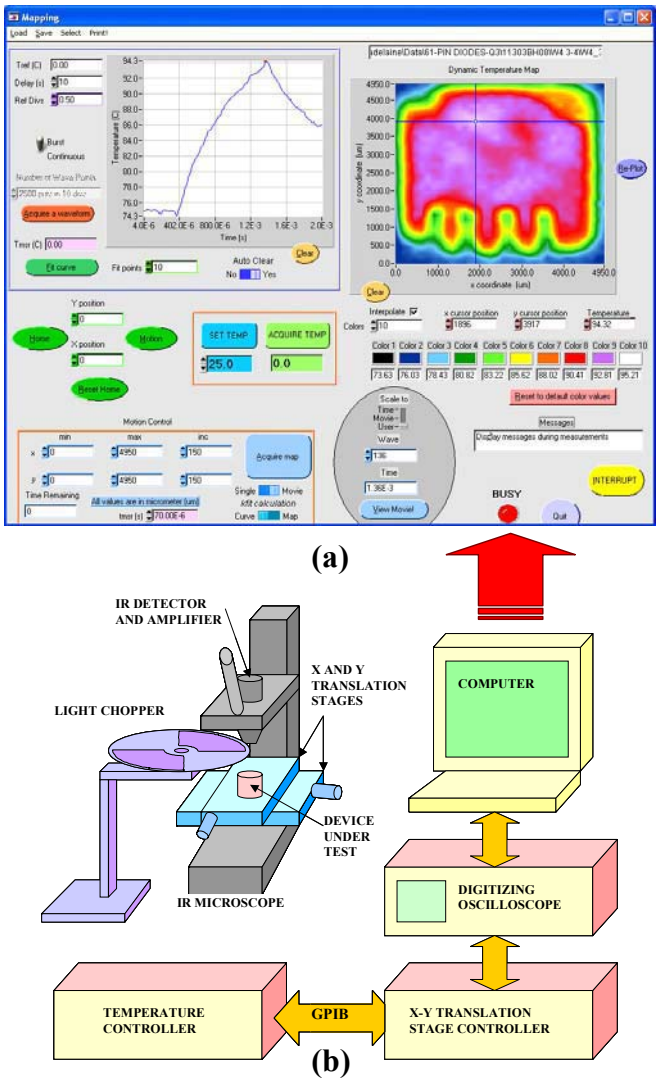

Figure 3. Transient Thermal Current Uniformity Degradation System: (a) front panel user interface, (b) experimental setup.

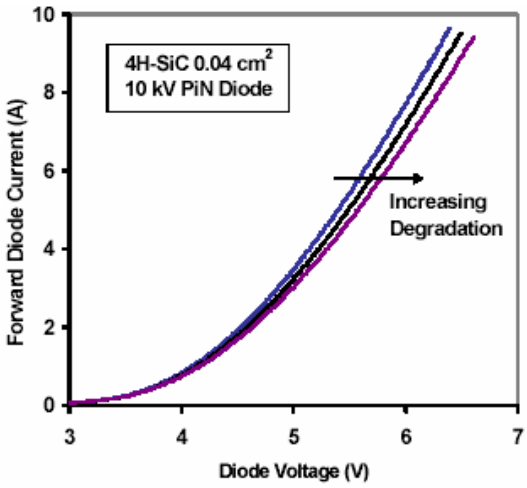

Figure 4. On-state characteristics of a high-voltage SiC PiN diode after various levels of forward bias stress.

Table 1 summarizes the results of the diode degradation measurements and provides the relationship between changes in the forward voltage (ΔV_f) and an estimation of the percentage of non-conducting area (ΔA) caused by the degradation process. The results given in the table are for the approximate degradation times of 1 h, 10 h, 100 h, and 1000 h. The non-conducting area percentages are qualitative estimates from the pulsed high-speed transient thermal images. In some cases wire bonds and bond wedges on the samples complicate the conduction area estimates.

In Fig. 5, V_f is plotted versus the current-time product for Diode 2, where (a) shows V_f on a linear scale and (b) shows V_f on a logarithmic. The current-time product is used to quantify the applied stress because V_f degradation is generally observed to be a function of this product although there is often an independent current dependence as well. In many cases, the degradation rate exhibits some sporadic behavior due to initiation and termination of individual stacking fault propagations within the material [1].

Fig. 6(a) shows the first thermal images for Diode 2, after it has been characterized for V_f, and Fig. 6(b) shows the last thermal image taken after 1000 h, giving an indication of the device current uniformity performance.

In Table 1, Diode 2 shows substantial degradation after 100 h with 20 % of non-conducting area and a ΔV_f greater than that seen in Diode 4 after 1000 h. On the other hand, Diode 4 exhibits the best least degradation with an on-state voltage change of 0.12 V and zero area reduction after 1000 h of stress (see Fig. 7 and Fig. 8). Presently, a number of devices have completed 2000 hr of stress and exhibit behavior similar to Diode 4.

IV. Conclusions

A procedure is introduced and utilized to evaluate the long term stability of SiC PiN diodes through continuous forward bias stress applied in variable time periods ranging from a few seconds to several hours and months, with V_f and conduction area monitored at various time interval. In general, devices with substantial degradation usually show a considerable ΔV_f considerable conducting area reduction after short degradation time periods. In contrast, devices with low degradation have moderately small ΔV_f combined with 0 % area reduction after thousands of hours of degradation. This new long-term stability monitoring procedure can be extended to other bipolar-type SiC devices, BJTs, IGBTs, and GTOs.

References

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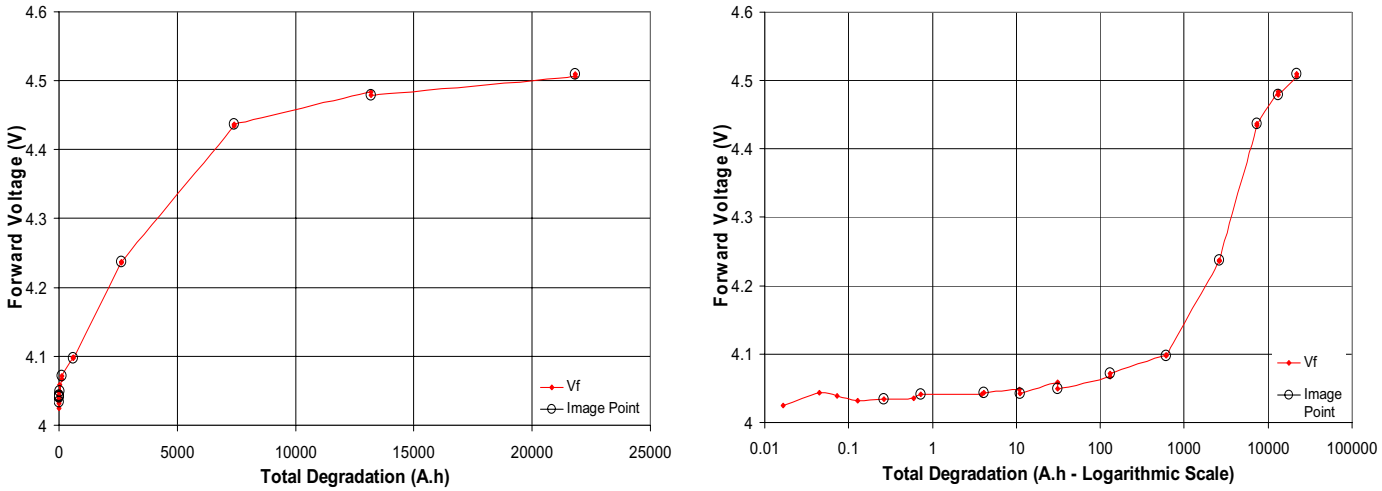
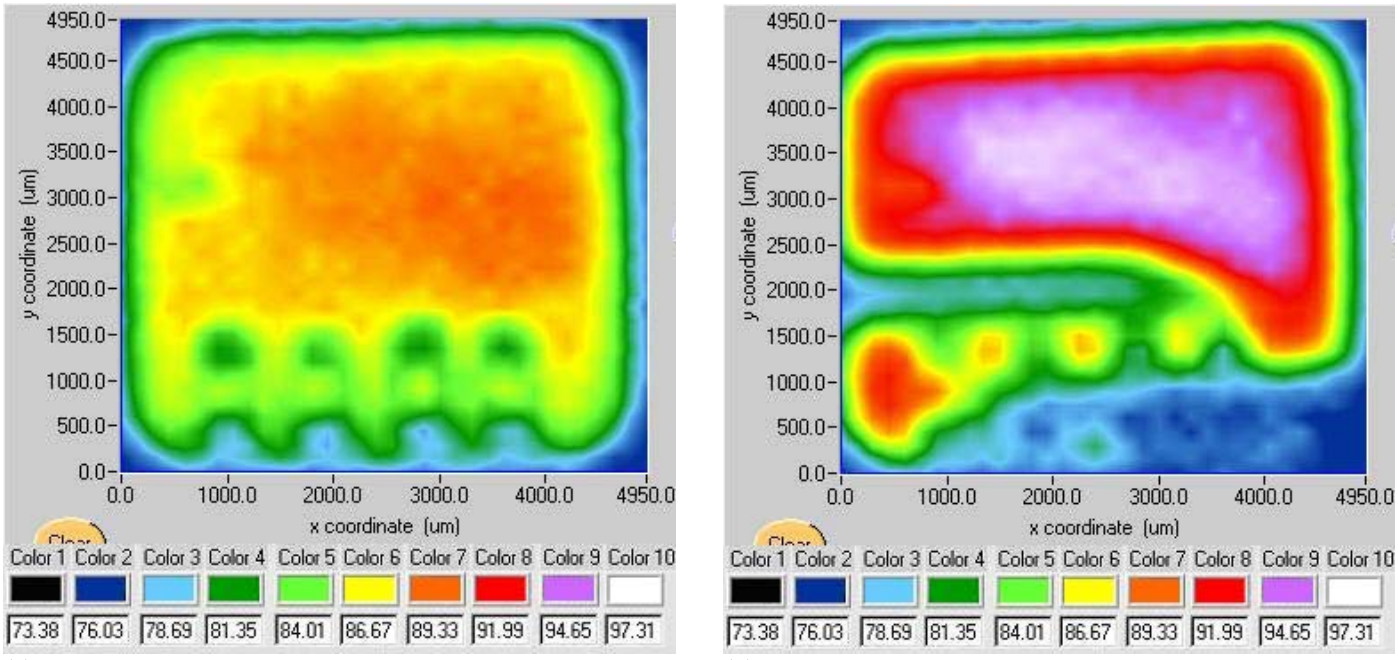
TABLE I
RELATIONSHIP BETWEEN CHANGES IN FORWARD VOLTAGE AND NON-CONDUCTING AREA PERCENTAGE

	0 h	1 h		10 h		100 h		1000 h		
	V_f Initial	ΔV_f (V)	$\Delta\%A_{lost}$	ΔV_f (V)	$\Delta\%A_{lost}$	ΔV_f (V)	$\Delta\%A_{lost}$	ΔV_f (V)	$\Delta\%A_{lost}$	V_f Final
Diode 1	4.25	0.08	20 %	0.12	40 %	0.15	40 %	0.22	40 %	4.47
Diode 2	4.04	0.02	0 %	0.05	0 %	0.20	20 %	0.47	40 %	4.51
Diode 3	3.80	0.01	20 %	0.02	20 %	0.08	20 %	0.13	20 %	3.92
Diode 4	3.72	0.01	0 %	0.01	0 %	0.06	0 %	0.12	0 %	3.93



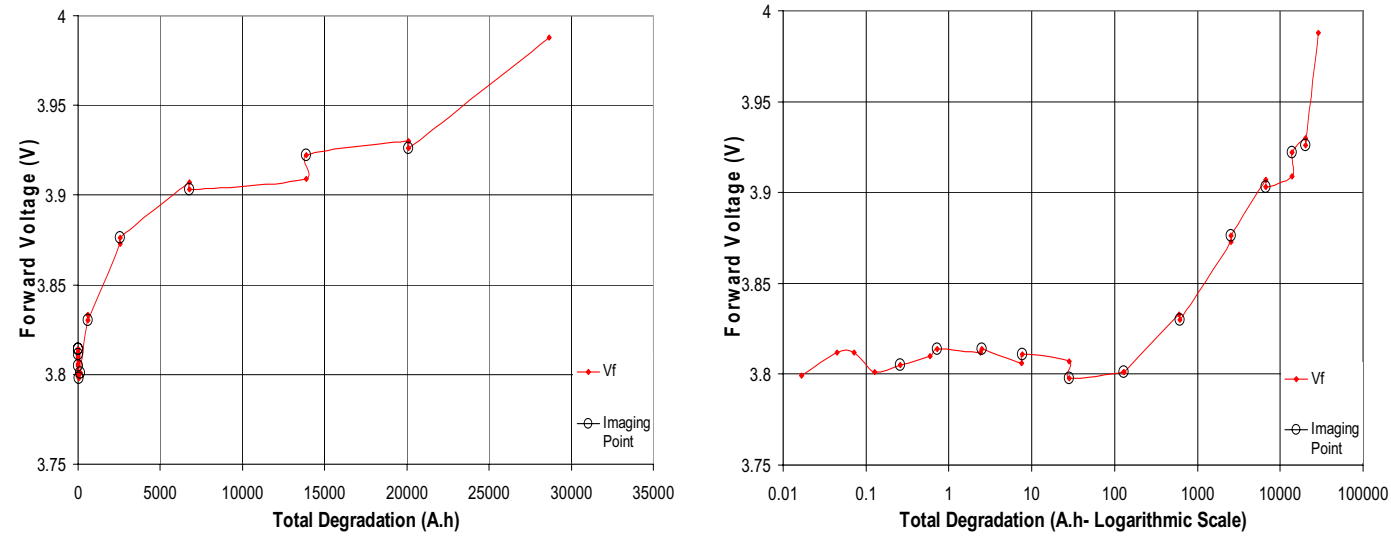
(a) (b)

Figure 5. On-state voltage, V_f, degradation as a function of total degradation (forward stress current-stress time product) for Diode 2: (a) regular scale, (b) logarithmic scale.



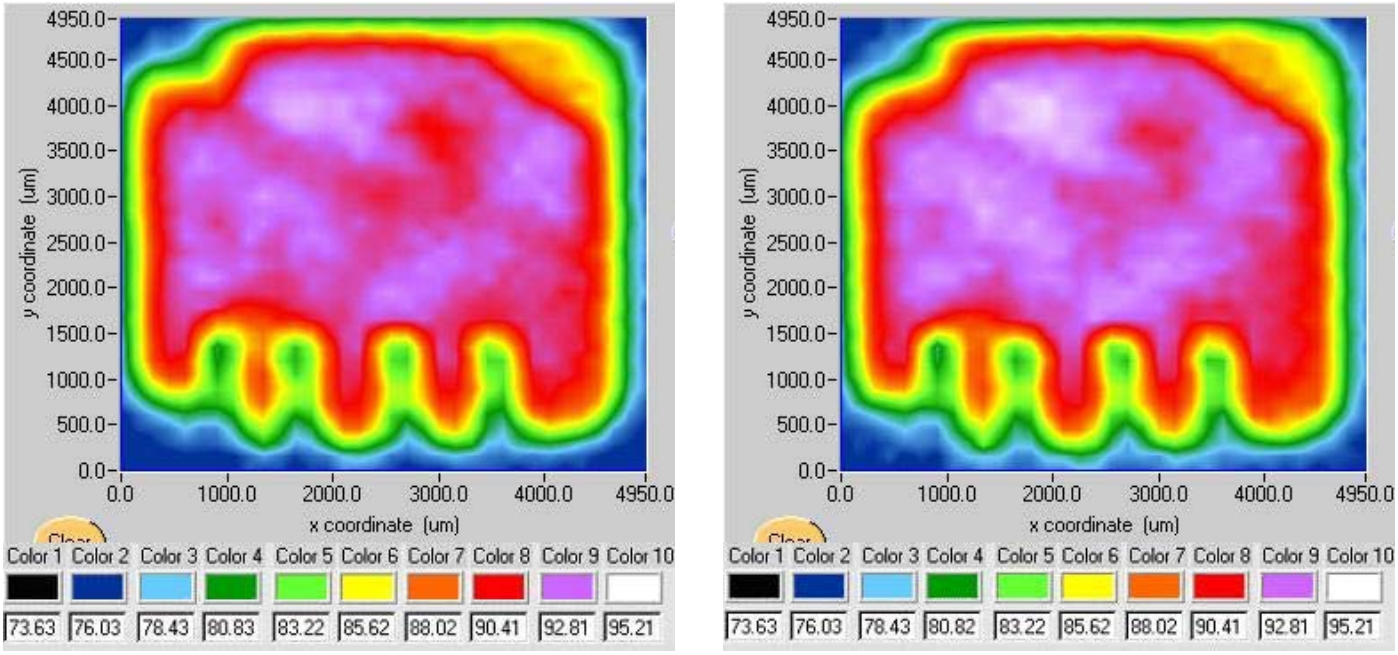
(a) (b)

Figure 6. Thermal images for Diode 2: (a) first image before any degradation, (b) last image after 1000 degradation hours.



(a) **(b)**

Figure 7. On-state voltage, V_f, degradation as a function of total degradation (forward stress current-stress time product) for Diode 4: (a) regular scale, (b) logarithmic scale.



(a) **(b)**

Figure 8. Thermal images for Diode 4: (a) first image before any degradation, (b) last image after 1000 degradation hours.