Random telegraph signals in *n*-type ZnO nanowire field effect transistors at low temperature

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Single-crystal zinc oxide (ZnO) nanowires have been fabricated as field effect transistors (FETs). The characteristics of low frequency noise in the drain current of *n*-type ZnO FETs have been investigated through random telegraph signals (RTSs) at 4.2 K. At room temperature, the noise power spectra have a classic $1/f$ dependence with a Hooge parameter that is $\sim 5 \times 10^{-3}$. At 4.2 K, the device's noise spectra change from $1/f$ to Lorentzian type, and the current traces as a function of time show RTSs. The channel current RTSs are attributed to correlated carrier number and mobility fluctuation due to the trapping and emission of carriers by discrete border traps. At certain bias conditions, the current in the channel shows three-level switching events with amplitudes as high as 40%, from which two individual defects with energies close to the Fermi level in the ZnO channel can be distinguished. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2761254]

For submicron complementary metal-oxide-semiconductor (CMOS) and nanowire/nanotube field effect transistor (FET) structures, one fundamental factor limiting their performance is the conduction fluctuation or signal-to-noise ratio. Because of the large surface-to-volume ratio of nanowire/nanotube FETs and unpassivated nature of their surfaces, the low frequency current noise fluctuations can be more pronounced in such devices due to the enhanced scattering from surface states. As a result, it is critical to reduce the noise and fluctuations in these devices, at least to a level comparable to traditional metal-oxide-semiconductor field effect transistors (MOSFETs), before nanowires/nanotubes can be used in integrated circuits. Low frequency $1/f$ noise has traditionally been utilized as a quality and reliability indicator for semiconductor devices.[1–3] The use of noise as a defect characterization method has become even more popular in recent years for deeply scaled Si MOSFETs[4–8] and nanoscale devices,[9–12] because the sensitivity of this technique improves as the size of the devices is reduced, as opposed to capacitance-voltage and charge pumping measurement methods which become less accurate as the device size decreases and require a substrate contact. $1/f$ noise was modeled by McWhorter in 1957 as carrier number fluctuations caused by the tunneling of electrons in and out of the surface states.[13] In large area transistors, the large number of trapping/detrapping processes with a broad range of time constants lead to $1/f$-type spectra by the superposition of Lorentzians.[3] For submicron silicon MOSFETs and nanowire/nanotube FETs, the fluctuating occupancy of individual electron traps in the gate dielectric close to the semiconductor/insulator interface generates discrete switching events in the drain current, resulting in two or more current levels in the current time trace, which are referred to as random telegraph signals (RTSs). The fluctuation of the current amplitude in the confined channel can be as high as 60%–70% for both planar submicron MOSFETs and carbon nanotube FETs,[14,15] posing a significant threat to the stability of scaled CMOS and nanostructures. At the same time, the study of RTS can provide a promising technique to probe a single trap and allows one to understand the fundamental physics behind the carrier transport and current fluctuations in nanoscale devices.[16–20] Using RTSs to study individual defects in ZnO nanowires has not been reported. In this work, *n*-type ZnO nanowire FETs were fabricated. Their low frequency noise and RTS properties were characterized and analyzed at both room temperature and 4.2 K as a function of gate bias. The noise spectra change from $1/f$ type at room temperature to Lorentzian at 4.2 K, due to the reduction of the channel carrier numbers and the shrinking of the trap energy range accessible to channel carriers. The physical nature of the traps responsible for the two- and three-level RTSs is also analyzed.

ZnO nanowires were synthesized by thermally vaporizing a mixed source of commercially available ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1:1 in a tube furnace. The nanowires in solution are then dropped onto a 100 nm thick, thermally grown, oxide on a highly doped *p*-type silicon substrate that can be used as a gate electrode. Ti/Au (100/100 nm) contacts were deposited by using an electron beam evaporator and defined by standard photolithography and a lift-off process to form the source and drain electrodes. The drain current noise is characterized with a dynamic signal analyzer and a digital oscilloscope

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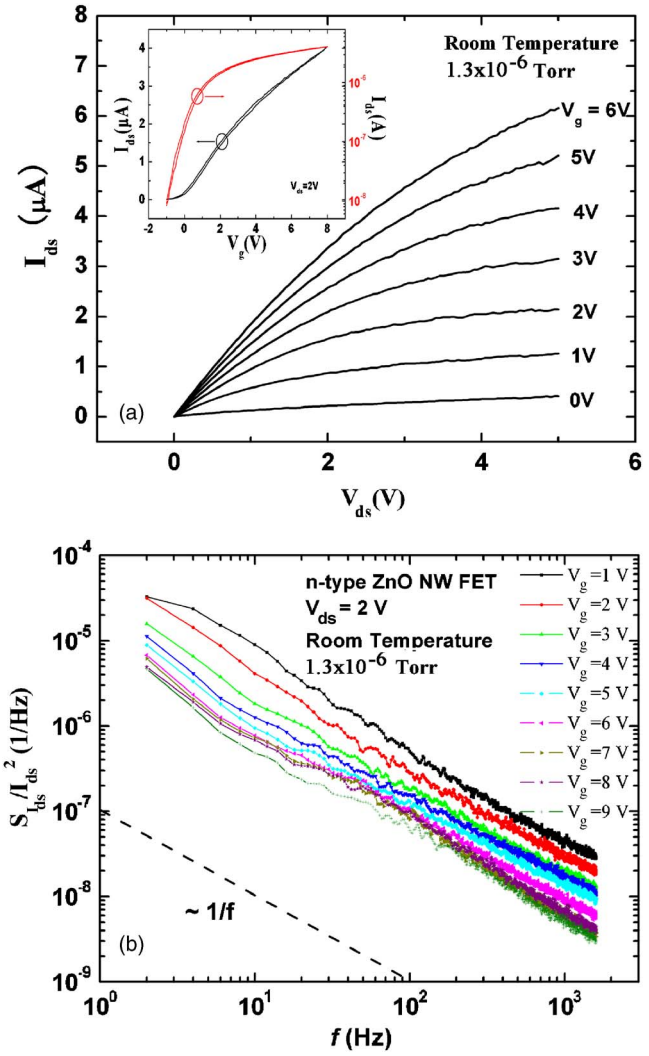

FIG. 1. (Color online) (a) I_{ds} vs I_{ds} characteristics for a *n*-type ZnO nanowire FET device at room temperature at 1.3×10^{-6} torr. The inset shows the I_{ds} vs V_g curve in both linear and log scales, showing good *n*-type transistor characteristics with small hysteresis. (b) Normalized drain current noise power spectrum density as a function of the gate bias in the frequency range of 1 Hz–1.6 kHz at room temperature. V_{ds} is constant at 2 V.

after the drain current signal goes through a transimpedance amplifier.

The dc electrical measurements were conducted at high vacuum ($<1.5\times10^{-6}$ Torr). Figure 1(a) and the inset show the I_{ds}-V_{ds} and I_{ds}-V_g characteristics of a ZnO transistor at room temperature. The modulation of the channel conductance indicates *n*-channel depletion mode of device operation with a threshold voltage approximately −0.5 V. The hysteresis of the I_{ds}-V_g characteristic is considerably smaller than that in air because surface absorption effects are minimized. Typical normalized drain current noise spectra are plotted in Fig. 1(b) with the device biased at $V_{ds}=2$ V and the gate bias varying from 1 to 9 V. The frequency range is from 1 Hz to 1.6 kHz. The low frequency noise spectra are predominantly $1/f^{\alpha}$, with the frequency exponent α close to 1. Further analysis shows the normalized current noise $S_{I_{ds}}/I_{ds}^2$ varies with $1/I_{ds}$ over the whole current range studied, indicating either a mobility fluctuation origin for the noise in the ZnO nanowire at room temperature[21] or number fluctuation noise, with an increase in defect density as the defect energy levels approach the band edge.[22] For $1/f$-type fluctuations, the noise behavior can be described by

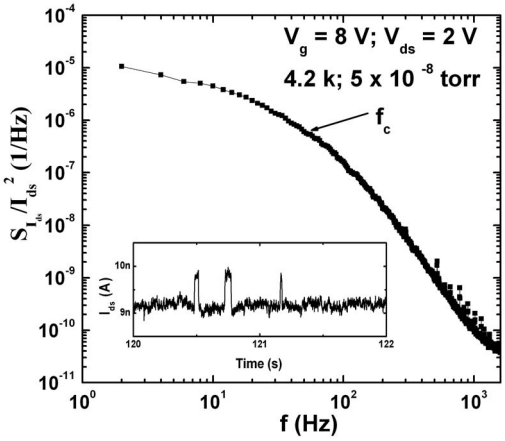

FIG. 2. Typical Lorentzian spectrum with corner frequency at ~18 Hz when the device is biased at $V_g=8$ V and $V_{ds}=2$ V; the inset shows the corresponding time domain RTS.

$$S_{I_{ds}} = \frac{AI_{ds}^2}{f^{\alpha}}, \tag{1}$$

where A is the noise amplitude, f is the frequency, and $S_{I_{ds}}$ is the power spectrum density of the drain current. The Hooge parameter is estimated to be $\sim5\times10^{-3}$ based on the procedure described in Ref. 14.

When the temperature is lowered to 4.2 K, the low frequency noise in the same device changes from $1/f$ to a Lorentzian spectrum. Figure 2 shows the noise spectrum of the ZnO nanowire FET biased at $V_{ds}=2$ V and $V_g=8$ V at 4.2 K, which can be described by

$$\frac{S_{I_{ds}}}{I_{ds}^2} = \frac{K}{(1+f/f_c)^2}, \tag{2}$$

where K is a constant independent of frequency and f_c is the corner frequency of the Lorentzian. The Lorentzian spectrum is caused by the trapping and detrapping of a single defect in the dielectric. The signature of this single trap state is also shown in the RTS of the drain current time trace of Fig. 2, where the channel current switches between two discrete values. The change of temperature to 4.2 K primarily decreases the number of defects in the dielectric accessible to the carriers in the wire and responsible for the fluctuations to a few single traps due to the shrinking of the activated energy window ($\sim4k_BT$, where k_B is the Boltzmann constant) in the dielectric band gap. In addition, it is accentuated by reduced carriers as indicated by a three orders of magnitude decrease of current at 4.2 K compared to room temperature. As a result, the trapping/detrapping of carriers from the traps causes more dramatic fluctuations of the channel current. The RTS trace in Fig. 2 is a small portion of the curve in Fig. 3(a) (where $V_g=8$ V). The corner frequency f_c can be estimated to be ~18 Hz by locating the peak of $S_{I_{ds}}^{*}f$ vs f plot. This is consistent with the calculation from mean time at high current τ_{on} and low current τ_{off} from the current time trace in Fig. 2, where $f_c=1/2\pi\tau_0$ and $1/\tau_0=1/\tau_{on}+1/\tau_{off}$.

In Fig. 3(a), 300 s drain current traces were recorded at $V_{ds}=2$ V as a function of gate bias; the corresponding histograms of the drain current data are plotted in Fig. 3(b) for more detailed analysis. For the case of two discrete levels at $V_g=8$ V, the corresponding histogram plot in Fig. 3(b) shows two distinct peaks with a background Gaussian distri-

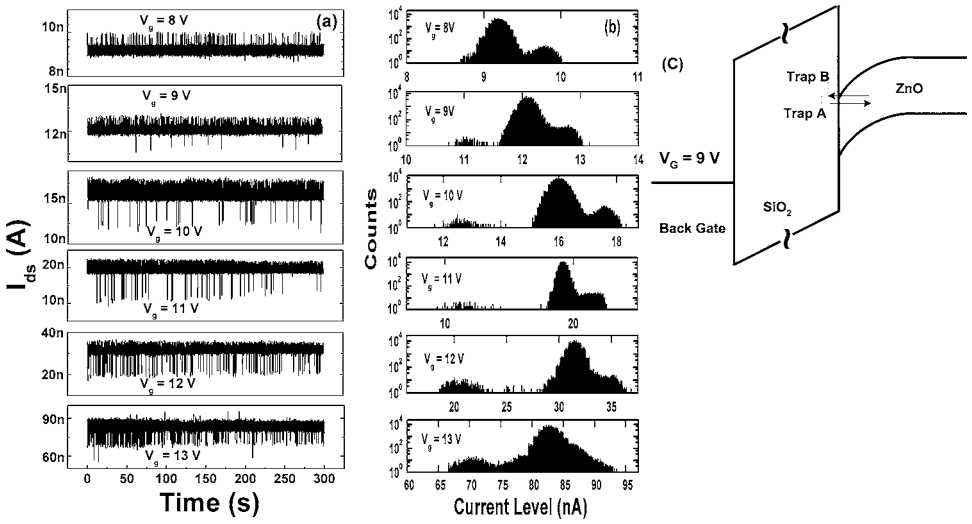

FIG. 3. (a) Raw drain current random telegraph signals for a time interval of 300 s observed in the ZnO nanowire FET at 4.2 K as a function of gate bias. The drain bias is kept constant at 2 V. (b) Histograms of the time-domain RTS data. The large and small peaks represent the empty or filled trap states, respectively. (c) Band diagram for back gate voltage at 9 V with two near interface oxide (border) traps.

bution, indicating only one near interface oxide (border) trap, A, interacting with the carriers through tunneling. At this bias condition, only one trap in the dielectric resides in the band gap within $\sim 2k_BT$ of the channel Fermi level, and is within a favorable distance from the channel to be able to be electrically active in the reversible capture and emission processes with the channel carriers. The low current level corresponds to the state that one electron is captured by trap A while the high current level corresponds to the empty state. As the gate bias increases, the trap occupancy increases. When V_g is increased to 9 V, negative peaks appear and the current trace shows three levels, confirmed by the three distinctive peaks in the corresponding histogram. It has been argued that this could be due to multiple electron trapping at one defect site,[2] which is highly unlikely due to the repulsive force between an electron and a negatively charged trapping center. The most likely scenario is that there is a second border trap,[23] B, with a slightly higher energy than trap A, located within $\sim 2k_BT$ of the Fermi level in the ZnO nanowire when the bias on the gate is increased, which causes more band bending. Here the high current value corresponds to the state where both traps are unoccupied, the middle current level is observed when trap A is charged while trap B is empty, and the low current level likely corresponds to the state where both traps are filled. The band structure of the measured device with two traps can be illustrated in Fig. 3(c). As the gate voltage increases to ~ 13 V, only trap B aligns with the Fermi level so that simple two level RTS is again observed. Trap B gives a much larger RTS amplitude compared to trap A, presumably due to a closer proximity to the channel. The number fluctuation caused by a single electron trapping/detrapping cannot account for the significantly large RTS amplitude ΔI_{ds} $(\sim 40\%)$. The combination of number and mobility fluctuations caused by coulomb scattering is dominant in our case.

In summary, we have observed anomalous RTSs in the drain current of ZnO nanowire FETs. $1/f$ noise is dominant at room temperature and the spectra change to Lorentizians at 4.2 K. The defects responsible for the RTSs are not visible by using conventional techniques which only measure average properties and miss the transient events. The channel current RTSs are attributed to the correlated carrier number and mobility fluctuation due to the trapping and detrapping of the carriers by discrete border traps in the SiO_2. At certain bias conditions, the current in the channel shows three-level switching events with amplitudes as high as 40% of the drain current, from which two individual defects with energies close to the Fermi level in the ZnO channel can be distinguished. The fast switching RTSs at 4.2 K suggest the effects of discrete traps on the carrier transport. The characterization of two- and three-level RTSs in these devices is a step towards the use of noise methods for the detailed characterization of the energetic and spatial position of individual defects in semiconductor nanoelectronic devices.

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