CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications[1]

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Abstract. Recently, prototype isolated-line, single-crystal critical dimension (CD) reference materials (SCCDRMs) with linewidths as narrow as 40 nm ± 1.5 nm have been reported. These reference materials, designated NIST Prototype Reference Material (RM) 8111, were configured as 10 mm by 11 mm silicon test chips mounted in 200 mm carrier wafers. The RM 8111 chips were fabricated using microelectromechanical (MEMS) process techniques, which assure the alignment of the sidewalls of the features to silicon (111) lattice planes, and were calibrated in a sequence involving atomic force microscopy (AFM) and high resolution transmission electron microscopy (HRTEM) metrology. This paper reports initial results on SCCDRMs fabricated on 200 mm bulk wafers; this monolithic approach would eliminate the need for carrier wafers.

Keywords: Metrology, Linewidth, Critical Dimension (CD), Reference Material (RM), Optical Critical Dimension (OCD), Scatterometry.
PACS: 61.46.-w

INTRODUCTION

In response to requests from the semiconductor industry, prototype isolated-line, single-crystal CD reference materials (SCCDRMs) with linewidths as narrow as 40 nm ± 1.5 nm (expanded uncertainty) were developed at the National Institute of Standards and Technology.[1,2] These reference materials, designated RM 8111, met the requirements for the 40 nm technology node (2011) specified in the *2006 International Technology Roadmap for Semiconductors* (ITRS).[3] In this paper we describe our research to respond to requests from industrial users of RM 8111 to provide the capabilities of RM 8111 in a different form.

RM 8111 was delivered with six features ranging from 40 nm to 250 nm to allow for use at a range of magnifications. Figure 1 is a sample of a calibration curve constructed from measurements made on two of these SCCDRMs with calibrated widths ranging from 40 nm to 250 nm.

Each of these reference materials was configured as a 10 mm by 11 mm silicon test chip mounted in a 200 mm carrier wafer. The carrier wafer was used to allow these SCCDRMs to be utilized in metrology tools that can only accept 200 mm wafers.

These prototype SCCDRMs were fabricated on (110) SIMOX (Separation by IMplantation of OXygen) wafers using the anisotropic wet etch techniques common to MEMS processes. Appropriate orientation of the lithography assures the alignment of the sidewalls of the features to silicon (111) lattice planes and allows for the AFM-HRTEM calibration procedure.[4]

Through chemistry improvements, and closer process control, a selection of features, with linewidths as low as 20 nm, have now been fabricated. They are anticipated to exhibit expanded uncertainties on the order of 1 nm. This extraordinary result is being achieved through formally designed experiments to identify factors that optimize reference-feature etching chemistry.[5]

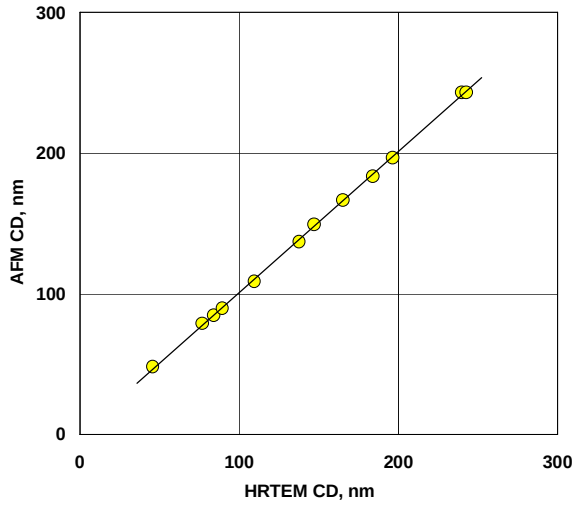

FIGURE 1. Calibration curve from recent release of prototype SCCDRMs.

Even in light of these recent improvements in linewidth and uncertainty, many in the end-user community have made it clear that the biggest enhancement that is now required is a monolithic implementation to replace the carrier-wafer assembly of individual chips. This is a major challenge because, although 200-mm wafers are considered acceptable by end users, silicon-on-insulator (SOI) having the necessary (110) orientation is unavailable in quantities commensurate with requirements. This paper thus reports progress towards fabricating a monolithic version of the CD reference materials on boron-implanted bulk (110) material. This implementation also offers a beneficial side effect over SIMOX and other SOI materials; since its features are conductive, they are much less subject to charging and hydro-carbon contamination under scanning electron microscope (SEM) inspection.

TEST STRUCTURE PROCESSING PROCEDURE

Three NIST wafers were patterned with the design NIST45A. NIST 45A is a modification of the NIST45[1] design used on RM 8111 with the following minor changes:

- Rotation of the elements of the test chip design so that the sidewalls of the feature align to the (111) planes on the 200 mm wafers
- Adjustments to allow patterning on the Nikon[2] Body 9, i-line, 0.57 NA, (8"), 5X reduction stepper with 0.45 micron resolution over a 2.2 cm square field by a lithography tool at the Scottish Microelectronics Centre at the University of Edinburgh.

Note that the first of these was required since the original NIST45 was patterned in 150 mm (110) silicon. On the 150 mm wafers, one of the (111) family of planes is parallel to a flat. In contrast, there is no flat on the 200 mm wafers; rather there is a notch. The notch is centered between the two families of (111) planes. The easiest way to understand this is to consider a v-shaped notch, with a 70.529° angle between the sides. The two families of (111) planes perpendicular to the (110) surface are parallel to the edges of the "v".

In addition, since the family of (111) planes is symmetrical relative to the notch, there is no longer the need for separate "11:00" and "1:00" designs.[1]

After patterning, one of the wafers was diced for process evaluation. Two of the chips were processed using the process flow previously optimized for use with SIMOX wafers.[5] This process was chosen as the baseline since it provided the best edge uniformity for processing the SIMOX chips.

- Acetone rinse to remove the photoresist
- Isopropyl Alcohol (IPA) rinse to remove the acetone residue
- Buffered oxide etch (BOE) for 12 s to pre-thin the hard mask
- 12 ½% Potassium Hydroxide (KOH) at 80 °C with ultrasonic agitation:
  - Chip 1: 10 s
  - Chip 2: 25 s
- BOE (20 s) for hard-mask strip.

After completion of the process, the chips were imaged by optical microscopy (Figure 2) and by SEM. The images showed the lines to have successfully patterned with provisionally acceptable uniformity. However, one concern was the surface of the field region. The KOH etch left the field region pitted and non-uniform. Since the tops of the features, as well as

[2] Certain commercial equipment is identified in this paper to describe the experimental procedure adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology or the University of Edinburgh, nor does it imply that the equipment identified is necessarily the best available for the purpose.

the surface of etched region, are bulk material, the primary contrast between the two is due to the non-uniform surface in the field region.

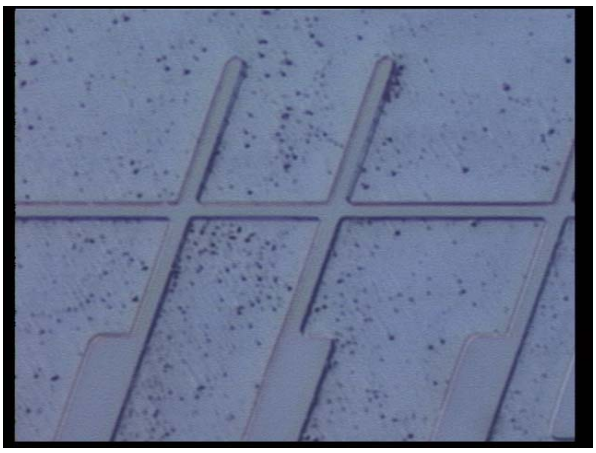

FIGURE 2. 16 µm segment of SCCDRM fabricated in bulk silicon on 200 mm wafer.

AFM CD MEASUREMENTS AND DATA ANALYSIS

Selected features from these two initial chips, including the one shown in the optical micrograph in Figure 2, were measured for CD and line uniformity using a CD-AFM (atomic force microscope) at NIST for which traceability and uncertainty budgets have been established.[6] The central 2.0 µm region of the 16 µm structure was measured. Figure 3 shows an example of the results of this measurement.

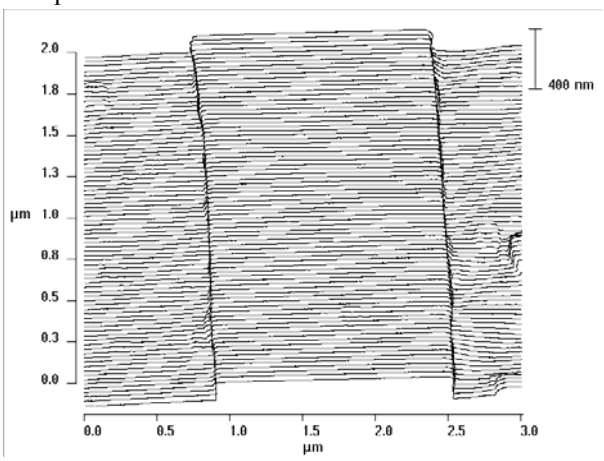

FIGURE 3. AFM scan of central region of 16 µm feature shown in Figure 2.

The first step in the analysis of the AFM data to determine the typical uncertainty of the CDs for these features was to fit a smoothing spline model[7] to the data. The smoothing spline model is a non-parametric regression model that allows us to separate the deterministic structure in the data as a function of position along the line from the noise, without having to assume a specific functional form for the relationship between CD and position. The data from one of the reference features studied as part of this work with a smoothing-spline fit through the points are shown in Figure 4.

Next a region in the center of the line of approximately 0.5 µm in length was identified as the portion of the line over which the non-uniformity of the CD would be determined. This length, which can be tailored to match different levels of navigational capability when the reference feature is used, was chosen to match the lengths used in the earlier development, calibration, and optimization of these types of reference features in single-crystal silicon[1] to facilitate comparisons between the different materials. The portion of the spline fit in the target region is surrounded by a box in Figure 4 to differentiate the target area. The approximate CD over the target length of line was then estimated using the mean of the predicted values from the smoothing spline model at the positions along the line where data was taken.

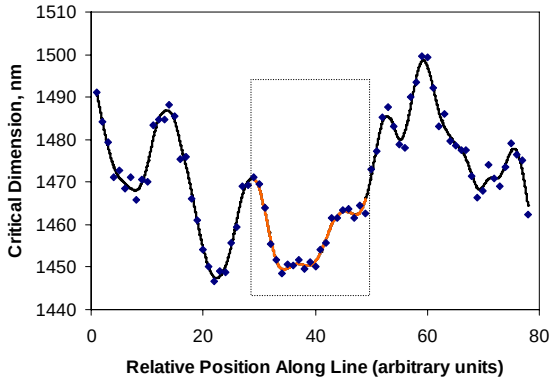

FIGURE 4. A smoothing spline model fit to AFM data on the CD of a reference line fabricated in bulk Si as a function of the position along the line.

The standard uncertainty in the CD due to non-uniformity of the reference feature was determined by a Type B evaluation[8,9] with assumption of a triangular probability distribution over the range of CD values over the target area of the line, as shown in Figure 5. Under this model, which is a simplified version of the uncertainty assessment used in the development of similar reference features using single-crystal silicon[1], the standard uncertainty due to the non-uniformity of the reference feature is given by $u_n = r_n/(2/\sqrt{6})$, where u_n is the standard uncertainty due to reference

feature non-uniformity and r_n is the range of the non-uniformity. By using this approach, the standard uncertainties due to non-uniformity for the reference features shown in Figures 4 and 5 were determined to be $u_n = 4.4\,\text{nm}$ and $u_n = 3.7\,\text{nm}$, respectively.

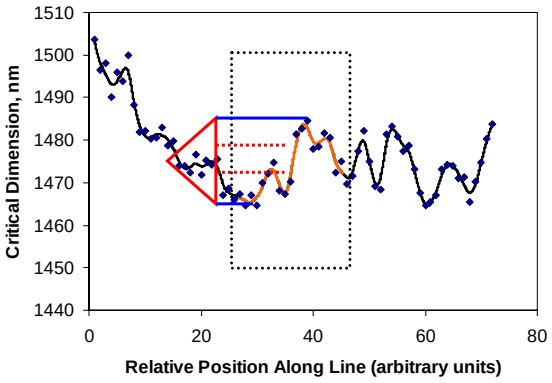

FIGURE 5. Illustration of triangular probability distribution used to obtain standard uncertainty due to feature non-uniformity.

To compare the uncertainties for the bulk Si reference features being reported here with our previously developed materials, a lower bound on the expanded uncertainty of the CDs determined for these two features were also determined. This was done by first determining a lower bound on the combined standard uncertainty, u_c for each feature and then computing an expanded uncertainty, U, from the formula $U = ku_c$, where k is a coverage factor used to control the approximate level of confidence associated with the expanded uncertainty. The sources of uncertainty included in the combined standard uncertainty, in addition to the standard uncertainty due to non-uniformity, were the standard uncertainty for the reproducibility of the AFM measurements (0.5 nm) and the standard uncertainty for the correction of the AFM offset (0.29 nm). To compute the expanded uncertainty, a coverage factor of $k = 2$ was used which corresponds to an approximate confidence level of 95 %. Some other minor potential sources of uncertainty from the estimation of the CD were not included, and so the results obtained from these computations are lower bounds for the expanded uncertainties for the CDs for each feature, which were $U \geq 8.8\,\text{nm}$ and $U \geq 7.5\,\text{nm}$, respectively.

CONCLUSIONS

In this paper we have described work to extend the successful NIST Prototype Reference Material RM 8111 to a monolithic implementation to meet the needs of the semiconductor industry. The initial results presented here are promising, but do not yet meet the uniformity and dimension requirements achieved in RM 8111. One potential advantage of using bulk silicon is that the feature height is no longer limited to the depth of the SIMOX device layer – typically 150 nm for SIMOX – but is completely a function of etch time. In this example, the KOH etch provided features 130 nm deep and 550 nm deep for 10 s and 25 s etches, respectively.

The initial results of patterning prototype SCCDRMs on 200 mm bulk silicon wafers have shown promise. However, it appears that we will not be able to use the optimized SIMOX process to reach our width and uniformity goals; rather, a new process must be developed.

These data do not yet show that the bulk material is capable of providing the same level of sidewall flatness and CD uniformity that are responsible for the previously achieved CDs of about 50 nm ± 2 nm observed for SCCDRMs fabricated in SOI material.

This work highlights an issue that may need to be addressed before acceptance of bulk silicon SCCRMs. This issue is the condition of the field area. Although the surface roughness of the field area does not affect the uniformity of either the top surface of the features or, more importantly, the sidewalls, its presence may serve to inhibit acceptance of such reference materials.

In future work, we plan to continue a two-prong development of monolithic SCCDRM on 200 mm wafers, continuing to investigate bulk silicon as well as continuing to procure 200 mm SOI wafers.

ACKNOWLEDGEMENTS

The authors would like to thank Heather Patrick and Curt Richter of NIST for technical discussions.

The authors would like to acknowledge the financial support of the NIST Office of Microelectronics Programs, the Engineering and Physical Sciences Research Council (EPSRC), and Edinburgh Research Partnership (ERP).

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