Methods to Characterize the Electrical and Mechanical Properties of Si Nanowires

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Abstract. We report metrology methods to characterize nanowires. In this work, representative devices and test structures, including nanoelectromechanical switches, non-volatile nanowire memory devices with SONOS structure, and both transfer-length-method and Kelvin test structures, have been developed to investigate the electrical and mechanical properties of the silicon nanowires. These methods and test structures can be readily applied to other (non-Si) semiconductor nanowires/nanotubes.

Keywords: Nanowire; Transfer Length Method; Nanoelectromechanical System; Non-volatile memory.
PACS: 81.07.-b; 81.16.-c; 85.40.Hp.

I. INTRODUCTION

Nanowires and nanotubes have been intensively investigated as the active medium for applications in various nanoelectronic devices. [1] However, there are very few metrology methods reported on the precise measurement of the properties of nanowires and nanotubes. This lack is because it is very difficult to manipulate and align such small materials for the fabrication of test devices; and there are not many readily available metrologies and physical models to extract the intrinsic information out of nanowires/nanotubes based systems. In this work, we have developed: (1) Kelvin method and Transfer Length Method (**TLM**) test structures to extract the conductance and contact resistance of Silicon Nanowire (**SiNW**), (2) nanoelectromechanical system (**NEMS**) to study the mechanical properties of SiNWs, and (3) non-volatile memory with SiNW on oxide/nitride/oxide (**SiNW ONO**) to study the charge retention and dynamics of the charge tunneling of the SiNW ONO system. These SiNW based test structures and methods can be applied to characterize other nanowires and nanotubes.

II. PREPARATION AND INTEGRATION OF SILICON NANOWIRES

The SiNWs were grown on Si (100) wafers by using chemical-vapor-deposition (CVD) with thin Au films (~ 1 nm to 2 nm) as the catalyst at 450 ^{o}C via a vapor-liquid-solid mechanism. [2] Diluted SiH_4 (10 % in N_2) at a pressure of 350 mTorr was used to grow the SiNW. Nanowires of 20 nm to 300 nm in diameter and 2 μm to 150 μm in length were obtained. Figure 1 shows a scanning electron microscopy (SEM) image of SiNWs grown on a Si wafer from a patterned gold catalyst.

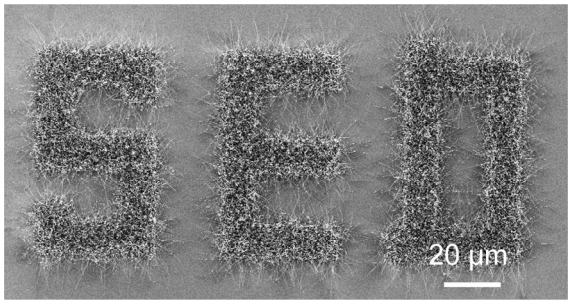

FIGURE 1. Scanning electron microscopy image of SiNWs grown from a patterned gold catalyst (in characters: SED).

In this work, we have used two methods to fabricate SiNW based test structures. Method A: For the fabrication of NEMS, Kelvin method and TLM test structures, the SiNWs were manipulated and aligned by using a single nanowire manipulation system (SNMS) and compatible photolithographic processes. [3] Method B: For the fabrication of SiNW ONO memory test structures, the SiNWs were grown from pre-defined locations and metal contacts were aligned via photolithography. [4]

III. CHARACTERIZATION OF RESISTANCE AND CONTACT RESISTANCE OF SILICON NANOWIRES WITH TRANSFER LENGTH METHOD AND KELVIN METHOD TEST STRUCTURES

In order to characterize the intrinsic conduction properties of semiconductor nanowires, it is necessary to separately determine the contact resistance. Primarily the four-terminal method has been used to investigate contact resistance and conductance in nanowires. [5, 6] Better methods are needed to improve the characterization of these electrical properties. The TLM test structure has been widely used as a precise technique for extracting contact and sheet resistance in microelectronics. [7] As shown in the SEM image in Figure 2 (a), a SiNW-based TLM test structure was fabricated by using method A followed by annealing with N_2 at 420 ^oC for 60 s to

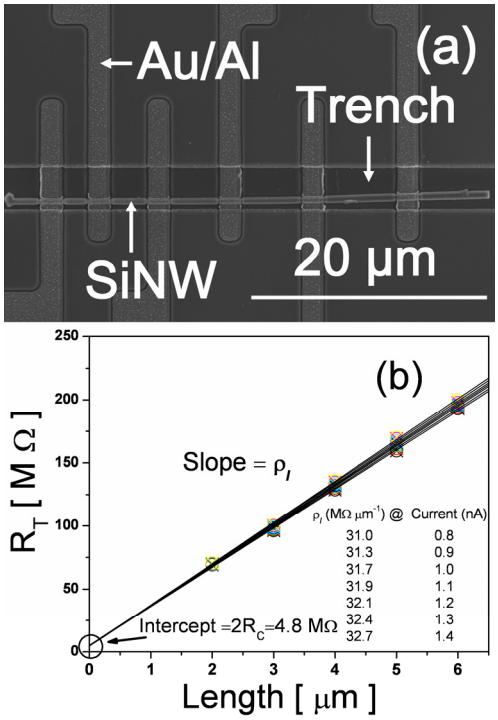

FIGURE 2. (a) SEM image of a transfer length method test structure for characterization of metal/nanowire contact resistance. (b) A plot of total resistance (R_T) as a function of contact spacing, length 2 μm to 6μm.

improve the Al/Si contact. For this TLM test structure, the total resistance (R_T) of any two contacts is

$$R_T = 2R_C + \rho_l L \quad (1),$$

where R_C is the contact resistance, ρ_l is the resistance per unit length of the SiNW (~165 nm in diameter), and L the contact spacing. The total resistance as a function of contact spacing L is plotted in Figure 2 (b) for a range of current levels with an inset showing the SEM image of the metal/SiNW contact. From a linear least square fit (LLSF), for this particular SiNW, the intercept $2R_C$ ranges from 4.5 MΩ to 5.1 MΩ, and the slope of each curve is ρ_l, which ranges from 31.0 $M\Omega\cdot\mu m^{-1}$ to 32.7 $M\Omega\cdot\mu m^{-1}$ (with uncertainty of 1.6%) for currents of 0.8 nA to 1.4 nA (Fig. 2b).

The Kelvin test structure is another semiconductor characterization technique widely used to measure contact resistance [7]. As shown in the SEM image of Figure 3 (a), a nanowire-based Kelvin method test

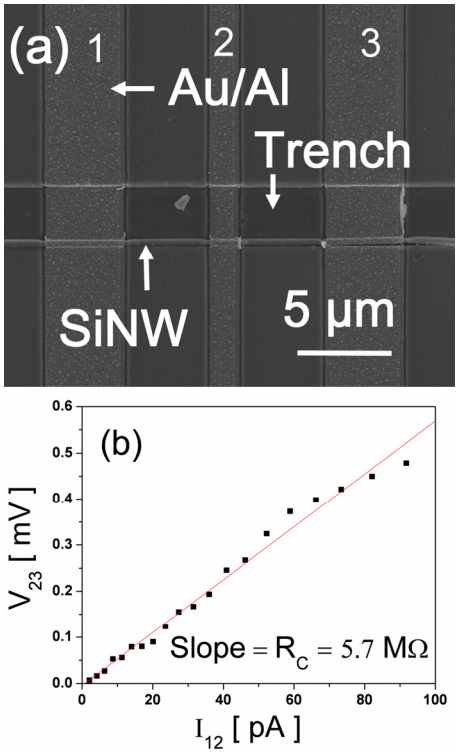

FIGURE 3. (a) SEM image of a Kelvin method test structure for characterization of metal/nanowire contact resistance. (b) A plot of voltage across metal/SiNW contact (V_{23}) as a function of current through electrode 1 and 2 (I_{12}). The slope is the contact resistance (≈5.7 MΩ) of the SiNW (~ 78 nm in diameter).

structure was fabricated by using method A and annealed with N_2 at 420 ^oC for 60 s to form good Al/Si contacts. With current flowing from contact 1 to contact 2, the contact resistance is

$$R_C = \frac{V_{23}}{I_{12}} \quad (2),$$

where V_{23} is the voltage drop measured between contact 2 and contact 3. The plot of V_{23} as a function of I_{12} is shown in Figure 3 (b). The contact resistance (≈ 5.7 MΩ for this ~ 78 nm diameter SiNW) is the slope of the plot by using a LLSF.

The specific contact resistivity (ρ_C) is defined as $\rho_C = R_C A$, where A is the contact area (estimated from πDd by assuming a cylindrical feature for SiNW with D as the diameter of the SiNW and d as the contact width, 2 μm for both test structures in Figure 2a and 3a). The specific contact resistivity of Al and SiNW is found to be ≈ 2.3×10^{-2} Ω·cm^2 and ≈ 2.8×10^{-2} Ω·cm^2 from the TLM and Kelvin structures, respectively. We attribute the relatively high specific contact resistivity to the undoped SiNW; however, further studies are in progress to understand the effect of SiNW doping and annealing condition on the contact resistance.

IV. CHARACTERIZATION OF YOUNG'S MODULUS OF SILICON NANOWIRES WITH ELECTROMECHANICAL SWITCHING SYSTEM

In addition to their possible use in electrical switching and logic applications, electromechanical switches formed from suspended nanowires can be

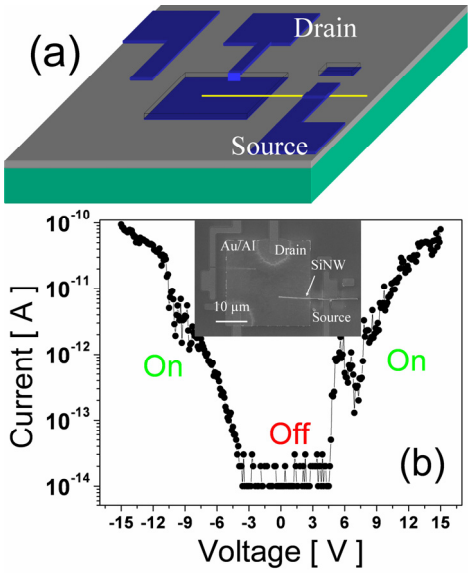

FIGURE 4. (a) Schematic drawing image of a 2-T SiNW electromechanical switch. (b) A plot of typical current-voltage characteristics with an inset showing the SEM image of the switch.

used to determine the mechanical properties (such as Young's modulus) of semiconductor nanowires. A schematic drawing and SEM images of a two terminal (2-T) SiNW electromechanical switch (EMS) are shown in Figure 4 (a) and the inset of Figure 4 (b), respectively.

The suspended gap was obtained by dry-etching 400 nm of the 600-nm thermal SiO_2 followed by Au/Al (10 nm / 10 nm) deposition and lift-off to form the bottom electrode of the switch. After the alignment of a SiNW (110 nm in diameter) with SNMS, a second-level metal (20 nm / 60 nm of Au/Al) was patterned on the part of the SiNW lying on the 600-nm oxide to clamp the nanowire in place and form the top electrode. The bottom and top electrodes are assigned as the drain and source of the 2-T EMS as shown in the images. Both levels of patterns were obtained by using regular photolithographic and metal lift-off processes with an Au layer on the top of the Al layer.

The typical switching current-voltage characteristics of a 2-T EMS are shown in Figure 4 (b) with an inset showing the SEM image of the switch. The 2-T EMS stays off until the applied voltage between the source and drain electrodes is raised above the threshold voltage, Vt, (Vt = 3.8 V for the example shown in Figures 4 (b)) and a significant increase in current is observed. During the operation, the suspended part of SiNW was bent down to touch the bottom electrode by the electrostatic force as it reached a snap-down point at Vt. The On/Off ratio of current measured at 9 V and 3.8 V is about 1000. Such reversible current-voltage switching is observed at both negative and positive applied voltages.

The threshold voltage for these EMS to "close" the switch and turn on the current is determined by the SiNW's diameter (R), suspending length (L), suspending height (h) and mechanical properties (e.g., Young's modulus: E) of the SiNW. When the maximum moment due to electrostatic force (M_e) is greater than the bending moment (M_m) of the SiNW, the SiNW will be bent down and in contact with the bottom electrode: the EMS will be closed. A simple estimate of Vt can be made by assuming the initial "snap-down" of the SiNW occurs when $M_e = M_m$. The bending moment (M_m) [8] due to the stress of SiNW, system capacitance C, and Me [9] can be expressed as

$$M_m = EI/\rho \tag{3},$$

$$C \approx 2\pi\varepsilon_0 L \Big/ \cosh^{-1}\left(2h/R\right) \tag{4},$$

$$M_e = \left(C^2 V_t^{\,2} h / 4\pi^2 \varepsilon_0 L^2\right) \int_a^b \int_0^L \int_0^L \partial x \partial z \partial l \cdot h \cdot l / \left(x^2 + h^2\right)\left[x^2 + h^2 + (z-l)^2\right]^{3/2} \tag{5},$$

$$E = M_e \cdot \rho / I \tag{6},$$

where I is the moment of inertia of the SiNW; **ρ** is the radius of curvature; a and b are the distance from the SiNW to the left and right borders of the bottom electrode, which are -10 µm and 15 µm, respectively. For the switch shown in Figure 4 (R = 110 nm, L = 10 µm, and h = 0.4 µm), E extracted by this method is ~ 118 G Pa, which is slightly larger than values reported for SiNW [10, 11] and that of bulk silicon (~ 107 G Pa). It should be noted that the accuracy of the extracted Young's modulus depends on how well C represents the specific geometry of the SiNWs and the electrode.

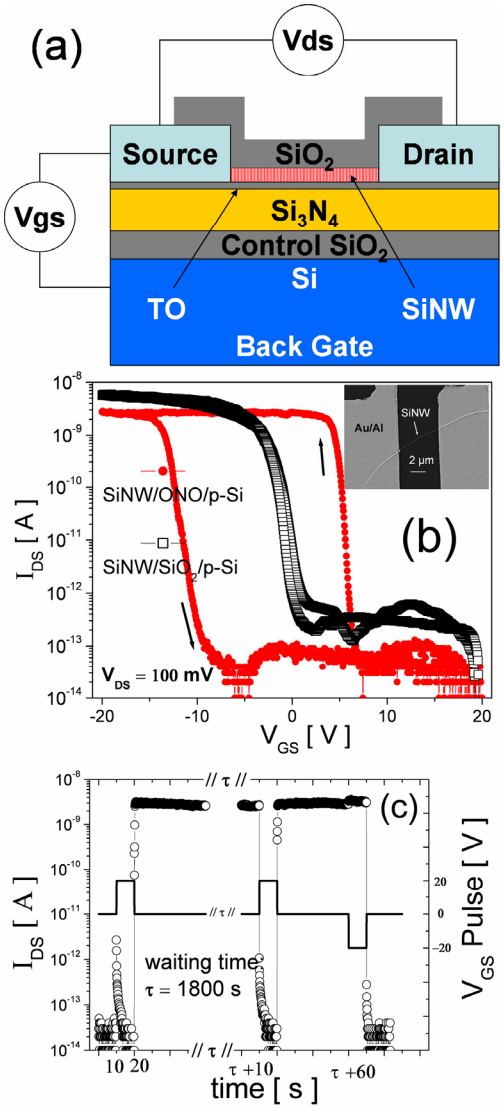

FIGURE 5. (a) Schematic drawing of a SiNW ONO memory device with measurement set-up. (b) Plots of I_{DS} vs. V_{GS} for the SiNW ONO (shown in the inset) and regular SiNW FET devices. (c) Simple Write/Read/Erase memory operations of the SiNW ONO devices.

V. SILICON NANOWIRE ON OXIDE/NITRIDE/OXIDE MEMORY TEST STRUCTURE

Non-volatile memory devices with SiNW on oxide/nitride/oxide (**SiNW ONO**) have been integrated to study the charge retention and dynamics of the charge tunneling of the SiNW ONO system. SiNW ONO devices were fabricated by using method B. The schematic drawing of the device cross-section and measurement set-up is shown in Figure 5 (a). The thickness for the tunneling oxide (TO), nitride and control oxide (CO) indicated on Figure 5 (a) is 1 nm, 60 nm and 30 nm, respectively. Regular back gate SiNW FETs with a conventional SiO_2 (~ 30 nm in thickness) gate dielectric were prepared as control devices for comparison.

The typical electrical characterization: source-drain (I_{DS}) current vs. gate voltage (V_{GS}) of a SiNW ONO device (shown in the inset of Figure 5 (b)) and a regular SiNW FET control device at 100 mV source-drain voltage (V_{DS}) is shown in Figure 5 (b). The SiNWs are about 25 nm in diameter and 3 µm in length. A large hysteresis (i.e. memory window) was observed from the SiNW ONO device while there was no significant hysteresis observed from the control device. These results can be explained as followed: At a high positive back gate voltage (e.g., 20 V), the negative charges (i.e. electrons) tunnel from the nanowire, through the TO into the nitride and oxide/nitride interface. [12] These stored negative charges act as a compensating negative gate voltage and induce a positive threshold voltage (V_{th}) shift. Hence the SiNW ONO device can be turned on at a higher positive gate voltage than the regular SiNW FET. As the back gate voltage switches to negative, the stored negative charges tunnel out of the ONO stacked layers and the positive charges are injected into the ONO stacked layers at higher negative gate voltages (e.g., - 20 V). The positive charges act as an effective compensating positive gate voltage to induce a negative V_{th} shift, and hence the device is turned off at a more negative gate voltage than the regular SiNW FET. Thus, the charge storage in the ONO stack layer leads to IV hysteresis. Undoped SiNW are very sensitive to change in nearby charges, which account for the dramatically large hysteresis and large on/off ratio observed for these SiNW devices (Fig. 5b).

As shown in Figure 5 (c), simple reversible Write, Read and Erase operations of the SiNW ONO device can be implemented by using programming voltage pulses of V_{GS} = 20, 0 and -20 V, respectively. The I_{DS} is continually monitored (i.e. reading) at V_{DS} = 100 mV. The device is first measured at V_{GS} = 0 V with

very low off-state I_{DS} current since no charges are stored in the nitride. At time, t, = 10 s, a 10 s pulse of 20 V is applied on the gate to drive negative charges to tunnel from the SiNW and store into the ONO layers. Low I_{DS} was observed during this Write operation at V_{GS} = 20 V. These stored negative charges shift the V_{th} to positive 7.5 V according to the I_{DS} - V_{GS} curve in Figure 5b. From t = 20 to 60 s, the devices is read at V_{GS} = 0 V with high on-state I_{DS}. During the continuous 1000 time reading operation for totally 40 s, the on-state current decays ~ 8% resulted from the small loss of certain charge from the nitride layer. The loss of charge is due to the thin TO between the SiNW and the nitride, and the read-disturb mechanism. [13] The device was then placed in an open circuit and re-measured after a waiting time (τ = 1800 s). The current is almost equal to that measured before waiting. This indicates that memory retention is disturbed more significantly during the reading operation than in an open circuit. The Write and Read operations have been repeated from τ + 10 s to τ + 60 s and the same behaviors have been observed. From τ + 60 s, a 10 s pulse of -20 V is applied on the gate to drive the positive charges (i.e. holes) to tunnel from the SiNW and stored into the ONO layers. High I_{DS} is obtained during the Erase operation due to the high negative gate voltage; however, the V_{th} is shifted to -5.0 V by the stored holes according to the I_{DS} - V_{GS} curve in Figure 5b. From τ + 70 s (after the Erase pulse), low off-state current is read at V_{GS} = 0. These Write/Read/Erase operations were repeated for more than 1000 times without degrading the devices.

VI. SUMMARY

In this work, we have successfully developed: (1) SiNW TLM and Kelvin method test structures to characterize and extract the resistance and contact resistance of SiNWs; (2) SiNW nanoelectromechanical switching system to measure the electromechanical properties of SiNWs; and (3) SiNW ONO memory system to study the charge storage and charge retention of SiNWs and nearby interface dielectrics. These device test structures can be engineered and used to characterize other nanowires and nanotubes.

ACKNOWLEDGMENTS

Contribution of the National Institute of Standards and Technology is not subject to U.S. copyright. The authors acknowledge the support of the NIST Office of Microelectronics Programs and NIST Semiconductor Electronics Division. The devices were fabricated with the support of the NIST Center for Nanoscale Science and Technology's Nanofab facility.

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