Array Based Test Structure for Optical-Electrical Overlay Calibration

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Abstract— **The novel overlay test structure reported in this paper was purposely designed to serve as an application-specific reference material. It features standard frame-in-frame optical overlay targets embedded in electrical test features and fabricated by the same process as the parts being manufactured. Optical overlay is commonly used in process control applications due to its utility for determining the relative positions of features patterned in photoresist. Electrical overlay, although it can only be measured on fully patterned test structures, is the metric of interest. Using this combined optical/electrical overlay test structure, we can derive the relationship between the routinely measured optical overlay and the electrical overlay for any specific combination of process and optical overlay tool.**

I. Introduction

An important function of manufacturing process control is assuring lateral geometrical superposition of a new additional layer onto an existing layer of patterned material on a partially fabricated wafer to within engineering-design specifications [2]. An important example is correct lateral superposition of vias in the M1-M2 (metal 1 to metal 2) inter-level dielectric relative to M1 patterned features. In this and other stages of wafer fabrication, the term overlay quantifies the degree of superposition. It is a vector which is parallel to the wafer surface and is defined at every location on a composite pattern of two layers. The magnitudes of its two components are measures of the relative lateral locations of features of the second layer with respect to corresponding ones of the first layer. The ideal value of both components of the overlay vector is zero. During wafer manufacture, the overlay at one or more locations on one or more die sites is sampled to confirm that it is within specification. The sampling is applied to the overlay between the patterned first layer and, either the developed resist of the second layer or, actual features of the second layer after completion of patterning. The test structures described in this paper apply to the second case, but their implementation can deal also with the first case. In both cases, overlay information is extracted by optical inspection with a highly specialized optical microscope, commonly known as an overlay tool. Such tools obtain local overlay values by capturing the image of a dedicated target structure, which is replicated on a die site specifically and exclusively to facilitate overlay metrology. A common target has the so-called frame-in-frame architecture shown in Fig. 1(a), which exemplifies the overlay-vector components. The key property of the target is that the outer frame is patterned in one layer and the inner frame is patterned in the material of the other. The analysis of its image, as collected by the overlay tool, is performed by well-established image-processing techniques and is rapid and economic.

The problem that this paper addresses is that the values of overlay obtained using optical means can be affected by two types of error. The first type is tool-induced shift (TIS). This factor often originates in misalignment of the optical axis of the overlay tool. The second is wafer-induced shift (WIS) which originates in any geometrical asymmetries; for example asymmetry in the vertical profiles of contact vias. The outcome is that the result of the frame-in-frame measurement typically includes elements due to either, or more likely both, TIS and/or WIS. Thus the reported optical overlay value

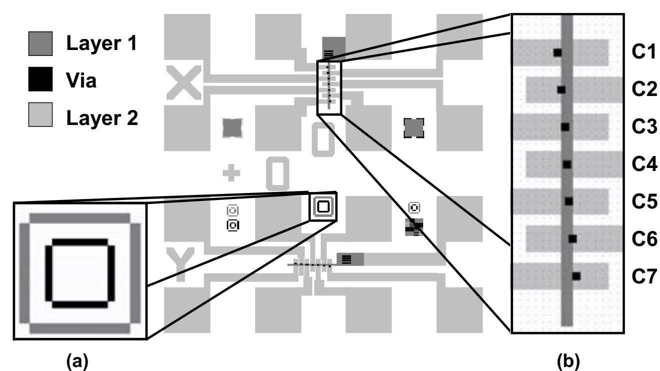

Fig. 1. Layout of single test cell of the NIST47 design with (a) frame-in-frame structure and (b) diagonal arrangement of contacts.

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[2]Subsequently we use the term first layer to refer to the uppermost existing layer and an additional layer is referred to as the second one.

generally differs by an unknown amount from a value based on optimum geometrical (and hence electrical) integrity of the conductor-via contact. We refer to the latter value as the electrical overlay. In this paper we report on a technique to determine this unknown difference. Please note that this new test structure is not designed to replace the optical overlay test structure in routine applications. This is because the box-in-box is typically applied after imaging the photoresist of the upper conductive layer. If the box-in-box shows the overlay to be out of specification, the photoresist can be removed and repatterned; if the process were continued to the point at which electrical metrology could be applied, identification of overlay errors is beyond the point at which rework could allow the salvage of the wafer.

II. Design

For demonstrating the technique, a test chip (NIST 47) has been designed [1], [2]. It consists of a regular array of similar cells that can be implemented in a three-level short-loop process . The three levels in this application are a lower conductor, a via, and an upper conductor. In this case we used a traditional metal 1 to dielectric-via to metal 2 interconnect process. Each test cell, one of which is shown in Fig. 1, has separate elements to determine the X and Y components of the local overlay of the dielectric-via level to the first metal level by electrical means as discussed below. Each of the two elements has a reference feature which is replicated in the first metal level (this is the vertical feature in the detail box in Fig 1(b)). At the completion of the fabrication, this reference feature is nominally connected to a metal 2 test pad through a group of vias as shown schematically in Fig. 1. Seven vias through the M1-M2 inter-level dielectric layer are regularly distributed along a line inclined to, and intersecting, the reference line. It is key at this point to remind the reader that the overlay is determined in this implementation of the test structure only between the first metal and the via layer. The second metal serves only to distribute the desired electrical signals to the pads.

The via pitch (p) is the component of the drawn lateral separation of adjacent vias in a direction perpendicular to the reference line, as shown in Fig 2(a). In the design used in this experiment, the pitch between adjacent vias is 0.5 μm or 1.0 μm, with the pitch between the end vias totaling 5.0 μm. In each element of the test cell, the as-fabricated mis-registration of a particular via is its center-to-center perpendicular distance from the reference line as shown in Fig. 2(b). It is equal to its as-drawn lateral displacement from the reference line plus the as-fabricated misalignment of the cell. The misalignment of the cell is the cell's programmed offset plus the overlay with which the test structure is fabricated. All cells of the test structure are fabricated with the same overlay but are replicated with their own programmed (drawn) offsets.

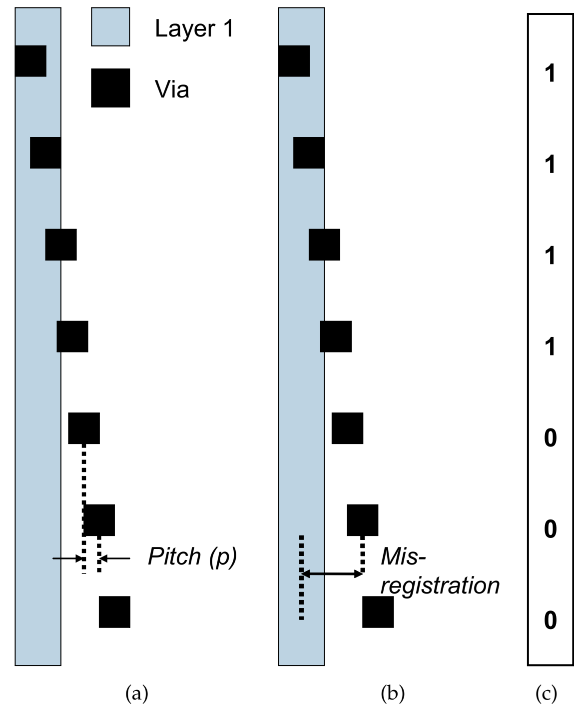


Fig. 2. Illustration of (a) pitch and (b) mis-registration of contact vias with (c) corresponding binary signature.

Electrical contact to the filled vias, some of which may be in contact, or in partial contact, with the M1 reference line, is provided by their connection to test pads on the M2 level as illustrated in Fig 1. This arrangement enables electrical continuity to be sensed between the reference line patterned on the M1 level and the contacts connected to the test pads on the M2 level. The results are recorded in binary format where a 1 represents electrical continuity and a 0 represents an electrical open. In principle, the misalignment of a cell can be determined to within a resolution of the via pitch p from the binary continuity signature (Fig. 2(c)) of the cell in a manner similar to that reported for vernier type structures [3]–[7].

Within each test cell is also a standard frame-in-frame optical overlay target. The placement of its features matches the as-fabricated misalignment of the cell, which is the cell's programmed offset plus the overlay with which the test structure is fabricated. The cell misalignment is measured optically using the same tool that is to be calibrated. In the test structure, which is a regular array of 287 cells, each cell has its own programmed offset which is a multiple of 10 nm. The complete test structure, shown in Fig. 3, enables the cross comparison of optical and electrical overlay between -1.43 μm and 1.43 μm in both the X and Y directions in steps of 10 nm for the purpose of application-specific calibration-curve

construction.

In the test structure design reported here, each cell is systematically placed in an ordered row and column format for simplifying analysis. However, the arrangement is such that the cells are effectively randomized across the complete test structure in both the X and Y directions. This ensures that any systematic change in overlay, for example increasing from left to right across the complete structure does not show up as an offset. Each column contains 16 cells, where the individual cells have sequential programmed offsets of 10 nm ordered such that the programmed offsets decrease from the top to the centre of the column in odd-number multiples of 10 nm. The programmed offsets similarly decrease in even-number multiples of 10 nm from the bottom to the centre of the column. The columns are arranged such that the leftmost column contains the set of cells offset in the extreme negative direction, while the rightmost column contain those in the extreme positive direction. Progressing towards the centre of the die sees the offset values alternate in direction (positive and negative axis) whilst decreasing in value.

III. Fabrication Overview

In order to demonstrate the design, a traditional two layer metal process fabricated on bulk silicon wafers was implemented. The wafers first undergo a thermal oxidation to provide electrical isolation from the substrate. Then a thin layer of aluminium is deposited and patterned with the M1 reference line of the electrical structure along with the external frame of the optical structure. Following this a dielectric layer of silicon

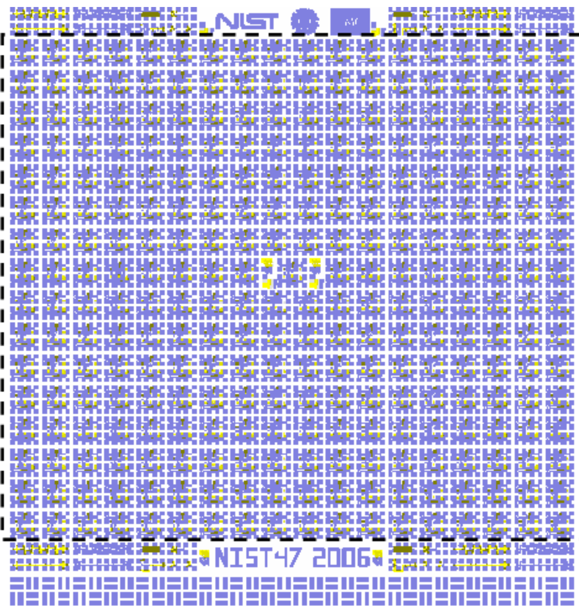


Fig. 3. Layout of entire chip for NIST 47 design; the test structure described in this paper is the 16 by 18 array of cells indicated.

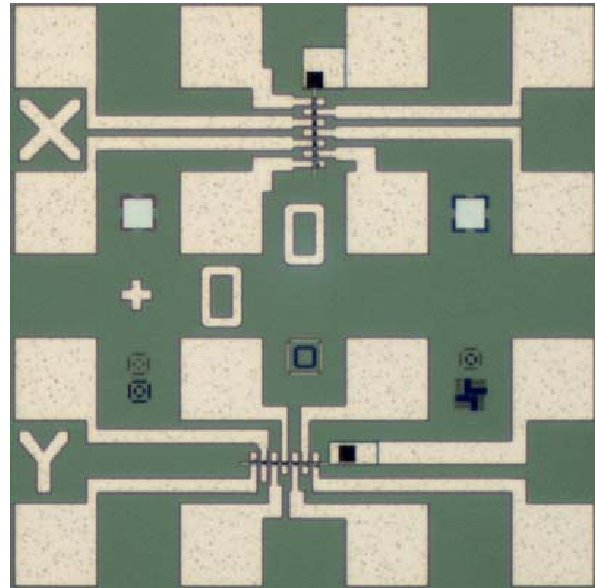


Fig. 4. Image of the as fabricated cell with zero programmed offset.

dioxide (SiO_2) is deposited over the surface of the wafer using plasma enhanced chemical vapour deposition (PECVD). The contacts, as well as the inner frame of the optical structure, are then patterned and etched into the dielectric layer until M1 is exposed under each via. Finally M2 is deposited and patterned providing the probe pads and interconnect necessary for electrical measurements. An image of one of the patterned cells is shown in Fig. 4.

Though this design is demonstrated with aluminium, it can be implemented with other interconnect matericals such as copper.

IV. Results

Complete arrays of 287 cells were measured electrically to determine the resistance between the reference line and the 7 contacts shown in Fig. 1. Electrical measurements used a standard resistance meter, as a means for determining continuity, along with a probe station and probe card fixtures to make physical contact with the probe pads. The frame-in-frame structures have also been measured using a SEM to compare with the electrical results. Table I shows some selected data extracted from the central structure along with the corresponding binary equivalents. The binary values are determined by setting a threshold resistance, where values greater than the threshold are classed as a ”0” (open) and a ”1” (short) for those below the threshold. As the difference between contacts that are conducting and those that are not is so large, a threshold of 1 kΩ is used for all measurements. The results presented in Table I indicate that the via with a pitch of 2.0 μm (C7) does not make contact and is misaligned positively with respect to the M1 reference

TABLE I
SELECTED R VALUES FROM ELECTRICAL OVERLAY STRUCTURE AND CORRESPONDING BINARY REPRESENTATIONS.

	Contact						
	C1	C2	C3	C4	C5	C6	C7
Programed Offset (μm)	-2.5	-1.5	-0.5	0	0.5	1.5	2.5
Weight Multiple (μm)	0.5	1.0	0.5	0	0.5	1.0	0.5
Resistance ($k\Omega$)	0.01	0.0092	0.0087	0.013	0.0095	0.011	17050
Binary	1	1	1	1	1	1	0

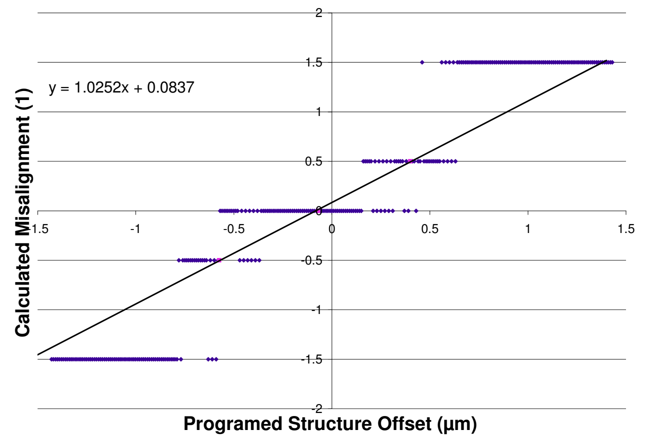
line. In order to represent the misalignment of each cell, the binary signature is weighted and summed together using equation (1), where C1 to C7 are the individual bits of the binary string.

$$((C5 \times 0.5) + (C6) + (C7 \times 0.5)) - ((C1 \times 0.5) + (C2) + (C3 \times 0.5)) \quad (1)$$

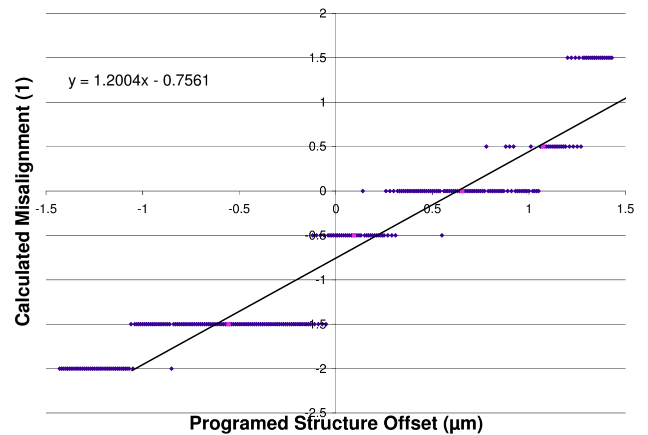
The weight multiples are determined such that the resulting calculated misalignment value provides a rough measure of the overlay for each cell. The whole test structure combines these values to provide a much better measure of overlay. The actual weight multiples employed for each via are provided in Table I. With the weighted sums for each contact calculated the leftmost 3 contacts (C1, C2, C3) are subtracted from the rightmost 3 contacts(C5, C6, C7), ignoring the centre contact as it has a 0 relative centre-to-centre distance from the reference line. The resulting value corresponds to the alignment of the contacts with respect to the centre of the reference line.

A plot of the derived values for the complete array of 287 structures, for both X and Y axis, on a single chip as determined by equation (1) is presented in Fig. 5. The electrical overlay value is then extracted from this data by calculating the median overlay value for the entire data set. For example, referring to Fig. 5(a), the set of data which lies on the calculated misalignment value of 0.5 ranges in programmed offset from 0.17 µm to 0.63 µm making the centre lie at 0.4 µm. This process is repeated for the remaining sets of data, in this case the 0 and -0.5 calculated misalignment sets. (Note: As the two data sets which extend to the limits of the programmed offset, both positive and negative, may contain data beyond those points, these sets can not be used in the calculation. In this case the $\pm$ 1.5 data sets) Linear regression is then used to determine the best fit of a line connecting the median points for the data ranging from -1.43 µm to 1.43 µm programed offset. Using the equation for the line relating the median points, the Y=0 intercept of this line provides a value for that particular chip's overlay in the X direction. The same process is then repeated for the data representing the Y axis.

Using this particular set of data a value of -81.6 nm was calculated for the overlay in X. To provide measurement assurance, SEM images (Fig. 6(a)) were taken of the frame in frame structure and measured to determine the overlay error from the optical structures. These measurements are conducted by extracting an intensity profile of the frame in frame structures along a perpendicular axis to the lines for each direction. An example of one of these profiles as used for the X direction is displayed in Fig. 6(b). With this intensity profile, the alignment can

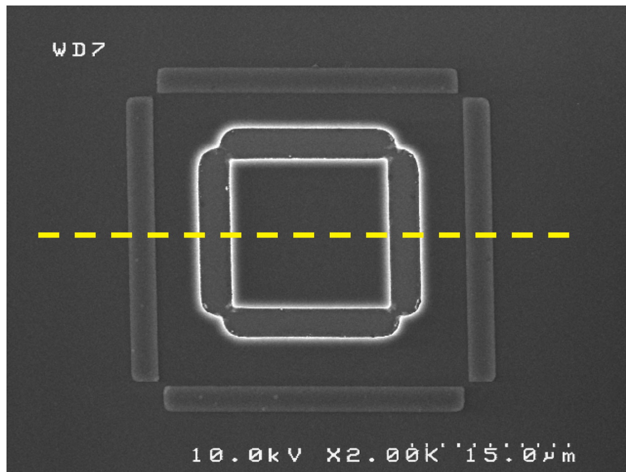


(a) Offset in X Axis

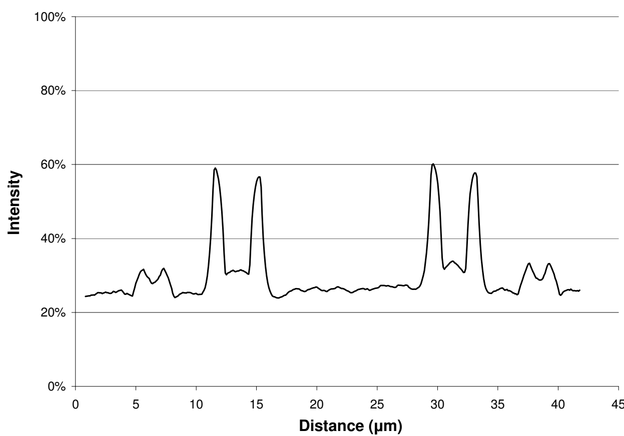


(b) Offset in Y Axis

Fig. 5. Plot of misalignment measurements calculated using equation (1) vs programmed structure offset for single die.



(a)



(b)

Fig. 6. Optical structure used for determining overlay. (a) SEM of frame in frame structure showing location of intensity profile. (b) Extracted intensity profile from above structure.

be determined by calculating the differences between the inner and outer frames, represented by the outer pair (for the outer frame) and inner pair (for the inner frame) of profiles in the intensity plot. The result of this measurement yielded a value of -80.6 nm, thereby demonstrating the functionality of this test structure.

Repeating this method for analysis of the data for the Y direction gives an electrically extracted overlay value of 629.8 nm, while the SEM intensity profile extracts the overlay as 638.4 nm. It can be observed that the values for the Y alignment differ by 9 nm. One possible explanation for this could be due to uncertainty in the measurements which result from non-uniformities in the processing. For example, if there is any fluctuation in via size caused by non-uniformity in the etch process, the cells will obviously produce different measurements depending on their location.

One observation from comparing Fig. 5(a) and Fig. 5(b) is that the slopes of the lines relating the median points differ slightly. The precise cause for this is currently being investigated.

V. Conclusions

A test structure for measuring overlay in interconnect systems has been presented which provides the necessary measurements to serve as an application-specific reference material. By incorporating a hybrid design approach, electrical structures are used to calibrate measurements taken from commercially available optical overlay tools. This is achieved by embedding optical frame-in-frame structures along side electrically testable overlay structures. This provides a straightforward method to relate optical overlay measurements with functionally relevant electrical overlay values. The NIST 47 design incorporates a large array of 287 test cells with an offset in increments of 10 nm that are used to determine overlay. An important aspect of this design is that as a standard 2 layer process is used, it is able to be fabricated by the same process as the parts being manufactured. Also, as the necessary electrical measurements are simply continuity measurements, readily available measurement tools can be used to electrically determine the overlay.

Electrical and SEM measurements have been compared and are in good agreement, providing overlay readings agreeing to within 1 nm in the X direction and 9 nm in the Y. Improving the process uniformity when fabricating these devices should help to produce much more accurate results in the future. Another source of error in this process, as with other processes utilizing lithography to define structures, is the registration of the features used in the patterning of the structures. The specific mask set used for these structures is reported to have a feature registration tolerance of ± 12 nm wafer level (based on ± 60 nm reticle tolerance using a 5x stepper for lithography).

VI. Acknowledgements

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