# On-Chip Characterization of Molecular Electronic Devices: The Design and Simulation of a Hybrid Circuit Based on Experimental Molecular Electronic Device Results

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## ABSTRACT

The focus of the field of molecular electronics primarily has been limited to the development of molecular electronic test devices and the characterization of electron transport through organic molecules. However, in order for molecular electronic technology to be realized, it is probable that these devices will have to first be integrated with traditional CMOS components and circuits. For this reason, we present the design of a molecular device/CMOS hybrid circuit that exemplifies how the two technologies can be integrated as well as how the CMOS circuitry can be used for the on-chip characterization of the molecular electronic devices. This work includes: the fabrication and characterization of silicon-based CMOS-compatible molecular electronic devices, the design of a hybrid circuit that can be used for on-chip characterization of the molecular devices, and simulations based upon the actual experimental device results that verify the effectiveness of the circuit. The components in this preliminary work have been limited to simple example devices and circuits to serve as a proof of concept, but the basic framework can be expanded in the future to include much more complex behaviors and systems.

## Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—*Advanced technologies*

## General Terms

Design, Experimentation, Measurement

## 1. INTRODUCTION

Molecular electronics is an emerging nanotechnological field based on the idea of using organic molecules with functional electrical behaviors (such as rectification, negative differential resistance or NDR, or electrical switching [1–6, 8, 11–14, 16–18, 20, 21, 27–29]) in place of traditional semiconducting materials for logic and memory components. Possible advantages of molecular electronic devices include: decreased area, lower power, increased physical flexibility, and energetic tailoribility. It is probable that if this technology is ever to be realized, the first application will be in a hybrid integrated circuit consisting of both molecular and conventional CMOS circuitry. Such a hybrid design paradigm would be able to take advantage of the best that each technology has to offer [24, 30]. Yet, most of the experimental research and development in this relatively new field has involved individual "test devices" that use processes that increase the ease and effectiveness of achieving and evaluating molecule-dependent transport [1–6,8,11–14,16–18,20,21,27–29], but in many cases disregard integration potential. Additionally, most of the device characterization that has been performed has been limited to individual external probing methods, rather than coherent characterization in a circuit environment. This is true even though the leading research in molecular electronics has shown that the devices are so environmentally sensitive that minor changes can drastically alter their electrical behaviors [4, 8, 18, 23, 26]. Thus, the development of CMOS compatible molecular electronic devices that can be characterized on-chip is essential to the realization of hybrid CMOS-molecular systems.

The first step in the realization of hybrid CMOS-molecular electronic circuits is to fabricate molecular devices using CMOS-compatible materials; however, this is rarely done. For example, gold is prevalently used in the fabrication of molecular electronic devices. A standard device configuration consists of the molecular monolayer self-assembled to a bottom gold contact with a top contact to the monolayer made by using a probing tip, metal wire, or evaporated metal. However, there are several problems with these gold-based devices including: the surface roughness of the gold traditionally used for the bottom contact (a rough bottom contact will result in a less ordered monolayer and can decrease the yield/stability of the devices), the mobile nature of gold (especially under applied bias) that can result in irregular electrical behavior, and the incompatibility of gold


*GLSVLSI'07,* March 11–13, 2007, Stresa-Lago Maggiore, Italy.

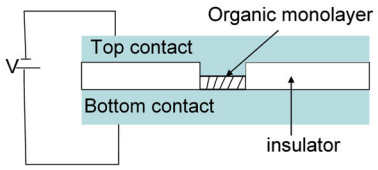


**Figure 1: Example molecular device structure.**

with traditional CMOS devices and materials (due to the potential for gold to create energy traps in silicon). Although recently more groups have realized the need to move to CMOS compatible materials [7, 10], the field is still dominated by the use of CMOS-incompatible gold.

A concurrent step in developing hybrid CMOS-molecular circuits is to design CMOS circuitry for the on-chip characterization of molecular electronic devices. Unfortunately, with few exceptions [24], molecular electronic devices are fabricated without much consideration of the possibility of integration with existing technologies in circuits [1–5, 11, 13, 14, 28]. Most devices are individually fabricated and then characterized by using one of an assortment of technologies, none of which pair them with devices required for practical logic and memory implementations.

This work investigates the potential for molecular devices that have been fabricated using CMOS-friendly materials and processes to be integrated with and characterized by traditional CMOS devices. Based on the CMOS-compatible molecular devices that we have developed and characterized, we have designed a realistic scheme for a hybrid CMOS-molecular integrated circuit. Additionally, we have designed simple CMOS circuitry to be used for detecting defective devices and determining the characteristics of working molecular devices, all to be accomplished on-chip. These circuits were simulated with Cadence tools to verify the operation of this hybrid circuit for on-chip characterization of the molecular devices. The simulation was performed by using actual experimental results from our devices to develop empirical Verilog-A models used along with standard BSIM transistor models in the Cadence Spectre environment [25].

In short, we present a blueprint for the complete fabrication of hybrid CMOS-molecular circuits to be used for on-chip characterization of molecular devices. Simulations are provided as a conceptual verification of the circuits and methods, as well as to be used in the future for the establishment of more complex devices and circuits. The remainder of this paper is divided up as follows. Section 2 describes in detail the fabrication and electrical characterization (I-V characteristics) of the molecular devices considered in this work. In section 3 the design and fabrication of the hybrid circuit is described. This is followed by section 4, which presents some CMOS circuitry that can be used to evaluate the devices for current magnitude and symmetry. We then present our conclusions in section 5.

## 2. DEVICE FABRICATION AND ELECTRICAL CHARACTERISTICS

We first fabricated and electrically characterized molecular electronic test devices. These electrical characteristics were later used in simulations evaluating the hybrid CMOS-molecular circuit configuration. The devices consisted of 10 $\mu$m wells in 200 nm of thermally grown silicon dioxide on heavily doped n-type and p-type silicon wafers ($1 \times 10^{17} \Omega \times$ cm). It is important to note that although these devices are not "nanoscale," the same device structure can be implemented on the nanoscale by using electron beam lithography instead of optical lithography. By using established assembly techniques [9], a monolayer of alcohol-terminated alkane molecules was assembled in the wells. Then, we deposited individual top contacts for the devices by thermally evaporating silver through a shadow mask. The resultant structure had a silicon bottom contact and silver top contact with molecules sandwiched in-between (Figure 1). For this device, the bias to the bottom contact was applied to the back of the entire silicon wafer, whereas the top contact of each device was individually biased.

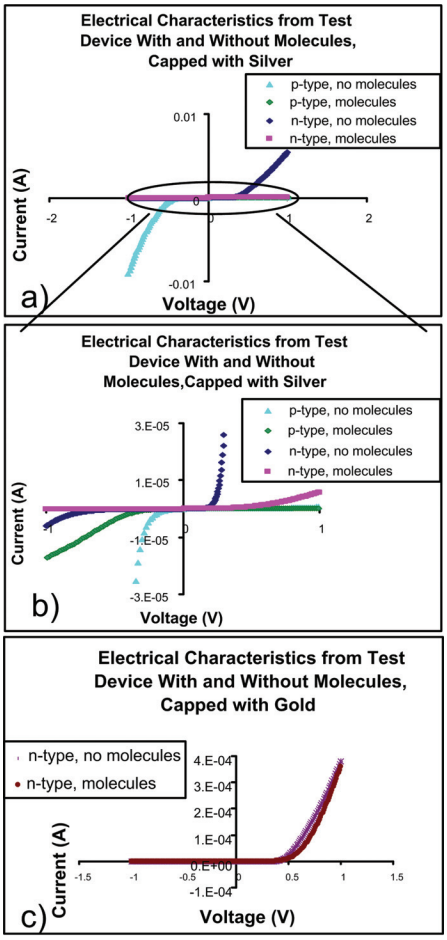


**Figure 2: Experimental electrical characteristics of molecular devices that were (a) n- or p-type silicon/ with or without molecules/ silver, (b) lower current scale of (a), (c) n-type silicon/with or without molecules/gold.**

The effectiveness of the device was first verified experimentally by external electrical measurement using a standard electrical probe station. Although the eventual goal is on-chip characterization, this initial probing was required to ensure that the simple devices functioned as expected and to establish electrical characterization that would be used for the hybrid circuit simulation. As one can see in Fig-

ure 2, the molecular devices on both n- and p-type silicon with silver top contacts showed different electrical characteristics than the control devices with no molecules (Figure 2 (a), (b)). The asymmetry (rectification) that is exhibited by all of the devices is due to the inherent Schottky barrier between the silicon and metal top contact. Figure 2 (a) shows that when each device is "on" by applying +1 V (to the device on n-type silicon) to -1 V (to the device on p-type silicon), the devices with no molecules exhibit more than two orders of magnitude more current than the devices with molecules. This behavior is expected due to the resistive nature of the molecules and indicates that the molecules form an effective current damping layer. The lower current scale in Figure 2 (b) shows that the curves from the devices with molecules are rectifying with the bias of the "on" state matching the ratification bias direction as for the devices with no molecules, just with lower current. The current at biases below 0.3 V (not clear in the Figure) is actually lower for the devices without molecules than those with, but this has been observed by other groups for similar systems [15] and may be attributed to molecular screening effects and the polarization of the molecules altering the energetics of the silicon surface and lowering the energy barrier [19].

Figure 2 (c) shows a device with a gold contact instead of a silver top contact. This figure shows one disadvantage of using gold as a top metal: the current from the molecular device is not significantly different than that observed from the control device with no molecules. This advantage of silver over gold as a top contact has been attributed to the fact that unlike silver, gold readily interacts with the bottom silicon to form a silicide. Previous work had shown that metals that react with the bottom silicon substrate (such as Al, Ti, and Au) will penetrate the monolayer, react with the bottom, and displace the molecules [22]. We used silicon as the bottom substrate due to the increased compatibility of silicon with CMOS, but also because the flatness of the silicon surface is far superior compared to that of gold, leading to improved devices with improved yields.

## 3. THE FABRICATION OF AN INTEGRATED SILICON-BASED CMOS-MOLECULAR CIRCUIT

In fabricating a hybrid silicon-based CMOS-molecular circuit, there are several obstacles to overcome. As described in section 1 (see Figure 1), the basic device structure consists of: a well in oxide with a silicon bottom that serves as the back contact of the device, the monolayer of molecules, and a top metal contact. This basic design is not easily translated into a circuit. The first complication is that if multiple devices are to be fabricated on the same heavily doped silicon wafer, then all of the devices are going to share a back contact (the silicon wafer). This is not a problem when testing individual devices, but is undesirable for an integrated circuit. Additionally, electrically isolated bottom contacts are easily fabricated for metal-molecule-metal devices (which is probably why they are such a popular device configuration) because the bottom metal can be evaporated and patterned on an insulator-coated substrate. Yet, silicon cannot be patterned as easily, and silicon-on-insulator is still a relatively expensive technology that is not directly integratable with mainstream CMOS circuits. Additionally, we wanted to use smooth single-crystalline silicon as the bottom substrate due to its obvious CMOS appeal. One way to achieve this is to dope the bottom silicon substrate to form electrically isolated areas for the device contacts. This is a similar procedure as to what is currently done for CMOS technology and should be effective as long as the voltages used are consistent with reversely biased well-substrate junctions.

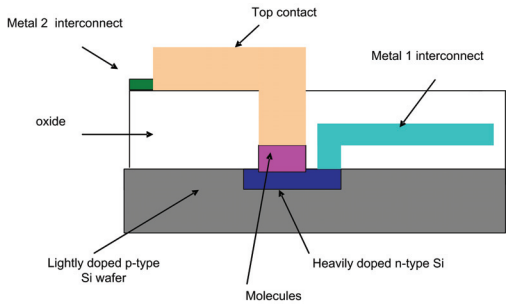


**Figure 3: A side view of a possible device scheme implemented by doping the bottom silicon, using two different metal layers for the interconnects, and then performing back-end processing to form the well for the molecular device, assembling the molecular monolayer, and evaporating a top contact to connect the top of the monolayer to the metal 2 interconnect. Note: The dimensions in the figure are not drawn to scale.**

One design possibility for the electrically isolated areas would be to have a lightly doped p-type substrate and to degenerately dope n-type areas for the molecular device platforms (Figure 3). Then, rather than making a backside contact, the bottom doped area can be directly contacted by a metal interconnect (Metal 1 in Figure 3). Then the insulator can be deposited, a second metal for the top contact interconnect can be patterned (Metal 2 in Figure 3), the molecules assembled, and the top metal contact evaporated. In this example the top contact to the monolayer can be made by contacting the metal 2 interconnect, and the bottom contact can be made by contacting the metal 1 interconnect. A side view of the final device is shown in Figure 3.

Another obstacle to fabricating integrated CMOS-molecular circuits is that of the incompatibility of the molecular devices with high temperatures and other conditions that may be encountered during the CMOS fabrication. Thus, ideally, the CMOS circuitry and all necessary interconnects (including that for the molecular devices) should be fabricated prior to the back-end assembly of the molecular devices by using standard CMOS fabrication procedures and processes. The doping for the molecular device areas could even be implemented during CMOS fabrication by designating the areas to be doped as n-type active areas (or wells) in the circuit layout. These areas would then be doped when the wells for the CMOS devices are doped. The design could also include vias to these doped areas that would also contact the top metal interconnects (see Figure 4). The space above the molecular device areas would be left empty in the layout and as additional CMOS layers are fabricated oxide would simply layer on top of the molecular device areas.

A possible final hybrid circuit layout is shown in Figure 4. The parts of the circuit that would be fabricated during the CMOS processing include: contacts that lead to a bus

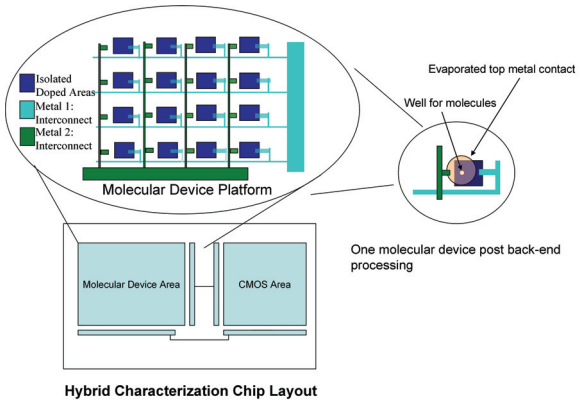


**Figure 4: The hybrid chip layout including the 4 by 4 array to be used as a molecular device platform and the top view of a device after back-end processing where the molecules and top metal contact are added (for side view of individual device see Figure 3).**

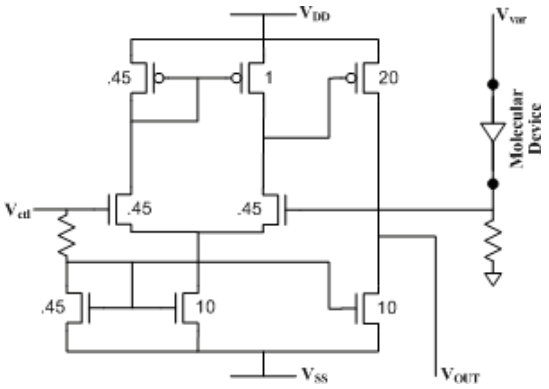


**Figure 5: Comparator circuit for detecting defective molecular devices.**

for the molecular devices, areas of degenerately doped silicon covered in oxide away from the CMOS area, and the isolated degenerately doped silicon connected through vias to the bus for connection to CMOS circuitry (See Figure 4). After this original processing, the back-end processing would include: etching a well for the devices above each highly doped n-type region (in dark blue), assembling the molecular monolayer in the wells, and evaporating the top metal via a shadow mask. In more complicated processing approaches, the top metallization could be formed by a carefully designed blanket metallization and post-deposition lithography and etching to create smaller top metal features than can be achieved with shadow mask techniques. Figure 4 also shows the top view of a device after back-end processing (see Figure 3 for a side view).

With a clear understanding of what electrical characteristics would be expected from the molecular devices and how the molecular devices and circuits would be fabricated, the question that remains is: how could CMOS circuitry be used for on-chip molecular device characterization?

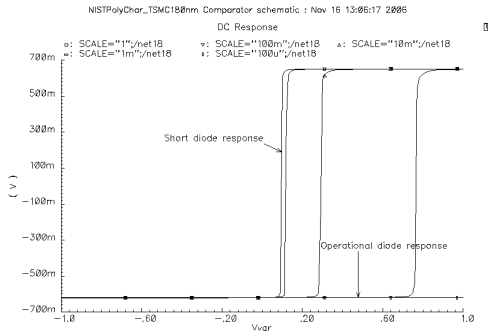


**Figure 6: Simulation results showing the response of the comparator circuit as the read voltage $V_{var}$ is varied. The curves vary from left to right as a function of the magnitude of current through the molecular device.**

# 4. APPROACHES FOR MEASURING DEVICES VIA CMOS

Perhaps the most important purpose of the proposed CMOS characterization circuitry is to determine whether or not a particular molecular device is defective. It is for this reason that we first describe a simple technique for determining if the current magnitude observed from a molecular device is consistent with that expected. A similar approach is used to evaluate the symmetry of the I-V characteristics of the device. In this way, the CMOS circuit can be used to determine if a particular molecular device is defective, if it functions as a diode, and even the direction of any rectification. While the same information could be directly learned by individually probing the devices, the circuits presented below could be used for on-chip characterization of the devices. This has potential advantages including: lowering signal noise, increasing device response, lowering costs, and increasing the availability and portability of the characterization capabilities and would prove especially useful for more complicated devices and circuits.

## 4.1 A Comparator for Detecting Defective Devices

One of the greatest obstacles in the fabrication of realistic molecular electronic devices is the relatively high percentage of defective devices. One common type of defect, in the context of the devices described here, is an electrical "short" where the top metal layer penetrates through the molecular monolayer and contacts the bottom silicon. The electrical characteristics of such shorted devices will be molecule independent. Thus, an important component of the characterization approach presented here is the ability to detect such defective devices.

In order to determine whether or not a molecular device is defective, we use the simple comparator shown in Figure 5. This particular comparator consists of eight transistors and, as can be seen in the figure, each is sized accordingly to achieve the desired functionality. In the simulations we performed the rail-to-rail voltage of the comparator was set to -0.9 V to 0.9 V and the reference voltage held at 0 V, just between the two rails. The output of the comparator is either pulled toward the lower rail, yielding an output of about -0.7 V, or to a higher output of around 0.7 V. When

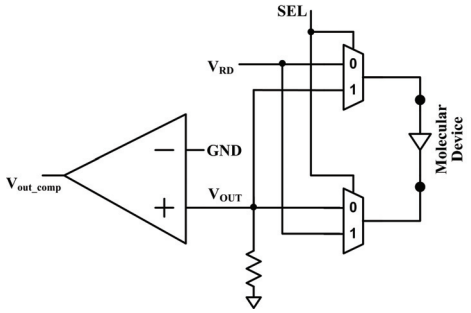


**Figure 7: Combination of both a comparator and symmetry tester.**

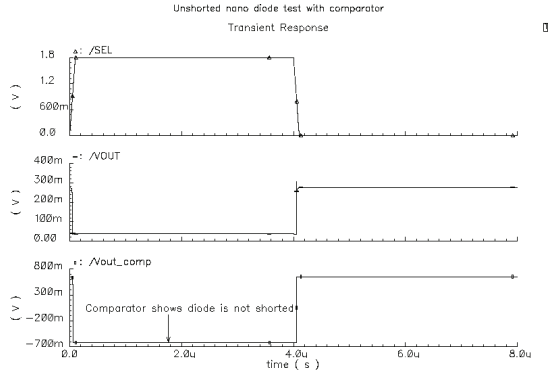


**Figure 8: Results of the symmetry tester accurately measuring a molecular diode indicated by $V_{OUT}$ being higher for SEL=0 V than for SEL=1.8 V. Also, the same output through a comparator indicates whether or not the molecular device is a "short."**

the output of the comparator is high, the molecular device is known to have a current magnitude greater than some predetermined limit, indicating an electrical short.

One important feature of the circuitry shown is that it can be "tuned" to be used with different current magnitudes that may result from variations in device design. This tunability is useful as one may want to either tighten or loosen the range of measured currents through a particular device that indicate a "short." It is also important because the current limit required to indicate a "short" will depend on the specifics of the device (area, type of molecule used, etc.). This "tuning" can be performed by simply changing the read voltage ($V_{var}$) of the circuit. Figure 6 shows the simulated output of this comparator for different magnitudes of current through the molecular device. The curve farthest to the left represents the current observed through a short defined by the highest current relative to the other curves in the same plot (see Figure 2). Put another way, each curve to the right of the first curve in Figure 6 represents a device with a one order magnitude less current. If one wants to define a defective device as a device with current magnitude like that of the "short" device measured in this work (see Figure 2), a read voltage of about 0.12 V could be applied to $V_{var}$. As Figure 6 shows, when $V_{var}$ is just greater than 0.12 V the second curve (which was simulated for current one magnitude lower than expected) has gone high. However, if one wishes to define a short as a device that shows 3 orders of magnitude lower current than the electrical short control device, a read value of 0.8 V could be used. In this manner, the simulation demonstrates not only that the circuitry is effective, but also that it contains the flexibility that is necessary for the user to define the characterization constraints.

## 4.2 A Simple Symmetry Tester

Another significant characteristic of a molecular device to be measured with CMOS circuitry is whether or not the electrical characteristics are linear. We would like to know whether a particular device is diode-like, consisting of higher current for one voltage polarity than the other, or if the device behaves more like a resistor. Obviously, this information is essential for evaluating the device's potential for use as a functional circuit component. Furthermore, unexpected symmetry (or asymmetry depending on the expected behavior) in the electrical characteristics could indicate a defective device.

The purpose of our symmetry tester is to first determine if a molecular device is more diode-like or resistive and, if it is a diode, to determine its orientation. The right side of Figure 7 shows the tester schematic. Similar to that of the stand-alone comparator, this is a simple design consisting of a couple of multiplexers which set the signal SEL to effectively orient the device in either a reverse or forward biased direction. Figure 8 shows the simulated output of the tester when the 10 $\mu$m molecular device with n-type Si is measured. The $V_{OUT}$ curve in Figure 8 (middle) shows that when the SEL signal is high it puts the diode in forward bias and when low the diode is reverse biased. If the voltage output of the tester remains essentially the same for both cases of SEL being high or low, the device is more of a resistor than a diode. When the output varies for different values of SEL, the orientation is determined by which SEL setting results in a higher output voltage.

The above two characterization techniques are integrated into a single tester with a built-in option to test both the symmetry of the diode as well as the possibility of it being defective. This is illustrated in Figure 7 where both the symmetry tester and comparator are combined, and Figure 8 shows the output when an n-type 10 $\mu$m molecular diode is measured. The results show that the comparator measures the diode by producing a high output signal from the comparator.

# 5. CONCLUSIONS

The simple CMOS circuits used in this work are the first step in demonstrating the potential for on-chip characterization of molecular electronics. We used the electrical characteristics of actual CMOS-compatible molecular devices for the design and simulation of on-chip characterization circuitry. Through this circuitry we showed that devices can be effectively evaluated for defects that result in undesirable current magnitudes. The acceptable current magnitudes are tunable by the user and thus allow for flexibility in molecular device design. We also designed and simulated a circuit for on-chip molecular device current symmetry assessment. We will now fabricate the circuits as optimized based upon the simulations and move on to using the same principles for the design of circuits integrating complex conjugated molecules expected to exhibit more interesting electrical functionality.

Similar circuits or variants of the ones presented here may also be useful as part of a built-in-self-test (BIST) methodology for a more complete CMOS-molecular architecture. Additionally, this same approach can be used to design and simulate the integration of other devices and circuitry incorporating other emerging nanoelectronic materials such as quantum dots, nanowires, carbon nanotubes, or organic field effect transistors. Ultimately, this work should represent an important stepping-stone on the path towards complete integration of molecular electronic devices with existing circuitry paradigms.

## Acknowledgment

This work was funded in part by the NIST Office of Microelectronics Programs and the DARPA MoleApps Program. The devices were fabricated with the support of the NIST Center for Nanoscale Science and Technology's Nanofab facility. This experimental research was performed while the author held a National Research Council Research Associateship Award at the National Institute of Standards and Technology.

Certain equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental details. Such identification does not imply recommendation by the National Institute of Standards and Technology nor does if imply the materials are necessarily the best available for the purpose.

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