# Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test Structures Fabricated from Silicon Preforms

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*Abstract*— **Test structures have been fabricated to allow Electrical Critical Dimensions (ECD) to be extracted from copper features with dimensions comparable to those replicated in IC interconnect systems. The implementation of these structures is such that no conductive barrier metal has been used. The advantage of this approach is that the electrical measurements provide a non-destructive and efficient method for determining CD values and for enabling fundamental studies of electron transport in narrow copper features unaffected by the complications of barrier metal films. This paper reports on the results of various tests which have been conducted to evaluate the current design.**

## I. Introduction

The need to develop a test structure capable of facilitating electrical extraction of parameters such as sheet resistance and linewidth from copper interconnect features has been presented in a number of papers [1]–[3]. A detailed description of the fabrication of a copper test structure that provides such a capability has been recently published [4]. The benefits of using this structure are that, due to the process and nature of the substrate material used, the copper interconnect features possess a nearly rectangular cross section. This allows linewidth to be extracted primarily by way of electrical measurements from specially designed all-copper test structures. Although a copper interconnect, in commercial applications, employs barrier layers for adhesion, diffusion, and oxidation properties, the structure reported here does not include a barrier metal in order to allow fundamental studies of all-copper features. The work aims to further the understanding of copper interconnects both with and without barrier layers. As a means of determining the traceability of this method as well as providing necessary calibration measurements, the structure reported also allows the linewidth to be measured using previously demonstrated techniques including, Atomic Force Microscopy (AFM), Critical Dimension - Scanning Electron Microscopy (CD-SEM), Optical Microscopy, and High Resolution Transmission Electron Microscopy (HRTEM) [5]–[7]. The NIST 35 design [8] was used to fabricate the all-copper test structures. Analyses of extended electrical measurements made on them are presented in this paper.

## II. Fabrication Overview

The substrate material employed for these structures is ⟨110⟩ silicon, chosen for its etch characteristics in anisotropic wet etch solutions. The test patterns are aligned to the ⟨112⟩ crystal-lattice vectors in the surface of the wafer and printed using a silicon oxide ($SiO_2$) hard mask. The pattern is then etched into the silicon with a tetramethylammonium hydroxide (TMAH) wet etch solution, which is inherently lattice plane selective. Due to the nature of the single crystal silicon and the etch solution, the sidewalls of the structures as defined by the ⟨111⟩ crystal planes provide a rectangular cross section with nearly atomically parallel sides [9]. This resulting silicon mesa is referred to as a "Silicon Preform" and may be used as a reference for linewidth. The dimensions of this silicon preform are preserved with a multilayer dielectric stack of low pressure chemical vapour deposition (LPCVD) and plasma enhanced chemical vapour deposition (PECVD) silicon nitride (SiN). These layers are then chemical mechanical polished (CMP) to expose the top of the silicon preform which also presents a planar surface. A portion of this silicon is isotropically removed to form a trench of which the bottom is oxidised to provide electrical isolation from the substrate. Subsequent copper deposition and CMP steps define the final copper test structures. Throughout the fabrication of these devices, care has been taken with the process steps to ensure that the copper film does not oxidise. The final step involves the deposition of parylene to act as a passivation layer and hence prevent any oxidation of the copper features. The parylene film is removed from probe pads to allow electrical contact during testing. At this point the structure is ready for electrical measurements to extract electrical parameters of sheet resistance and linewidth (Fig. 1). Typical copper thickness seen in the structures used for this study was 300 nm.

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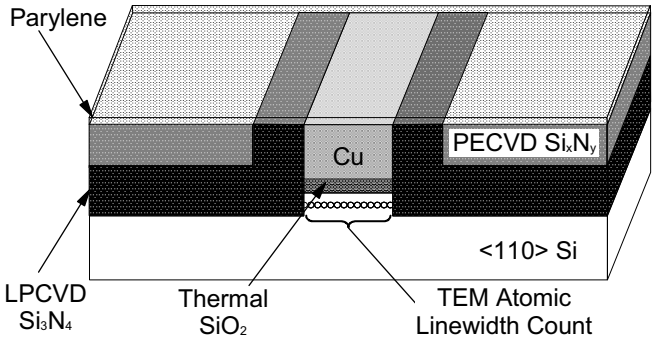


Fig. 1. Diagram cross section of test structure used [4]

## III. **Method**

The analyses of sheet resistance and linewidth of the copper test structures are based on work which has been reported previously [10]. Measurements are designed to be undertaken using a standard DC parametric test system comprising of a current source and a high sensitivity voltmeter[2]. Electrical contact is made to the devices using a probe station and probe card fixtures. During electrical testing, parameters were chosen to maintain the linearity of the V-I variables and to reduce the impact of joule heating.

### *A. Sheet Resistance*

Sheet resistance measurements reflect thickness variations in the copper film as well as provide a useful parameter for linewidth extraction. V-I measurements were taken from three different van der Pauw sheet resistance structures located at various sites over the entire die. The three structures are the Greek Cross, Corner Tapped Box Cross, and the Side Tapped Box Cross (Fig 2).

Fig. 2(a) is used to explain the measurement strategy for sheet resistance measurements. Forcing a set current from arm 4 to 1 and measuring the voltage drop across arms 3 and 2 as well as similarly forcing current the reverse direction from 1 to 4 and measuring the voltage between 2 and 3 provides two values which can be averaged to determine the $(V/I)_1$ value for the obtuse angle. In the same manner, the acute angle is measured by forcing current in both directions on arms 1 and 2 while measuring the voltage drops across arms 4 and 3, providing $(V/I)_2$. The actual sheet resistance value is then calculated using the $(V/I)$ values to solve for Rs in the generic van der Pauw equation (1) [11].

$$exp\left(\frac{-\pi(V/I)_1}{Rs}\right) + exp\left(\frac{-\pi(V/I)_2}{Rs}\right) = 1 \qquad (1)$$

[2]As DC electrical tests are performed to extract parameters from the copper test structures, skin effects, which become noticeable in copper lines at high frequency applications, are not present.

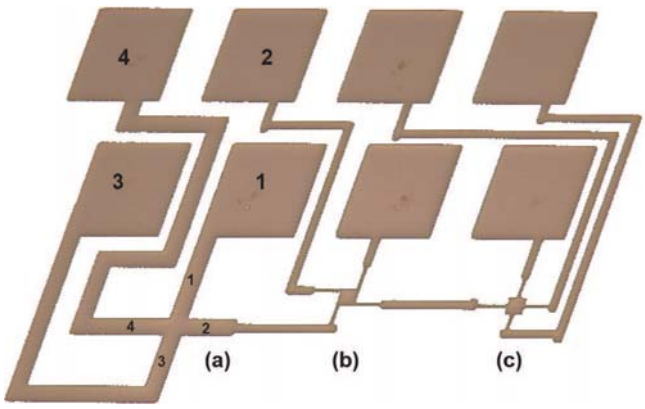


Fig. 2. Test structures used to extract sheet resistance for copper interconnect features (a) Greek Cross (b) Corner Tapped Box Cross and (c) Side Tapped Box Cross

### *B. Linewidth*

The linewidth test structures used for these measurements are specifically designed to eliminate the need for strict design rule restrictions as seen in standard linewidth cells [12]. From Fig. 3 it can be observed that they consist of multiple tapped bridge resistors with a range of segment lengths having a constant linewidth from which V-I values can be extracted.

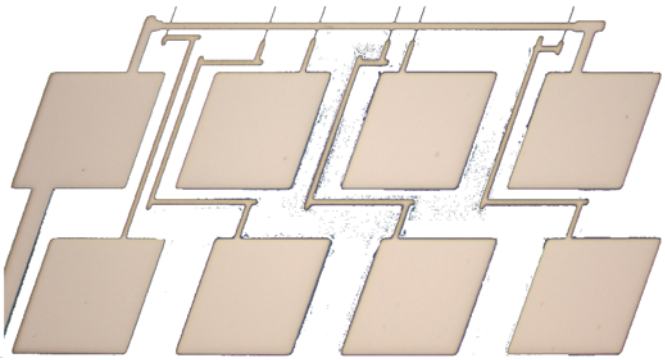

Fig. 3. Test structure used to extract linewidth for copper interconnect features

*1) Individual Segment Analysis:* In this method linewidth is extracted using the standard formula for Kelvin type bridge resistor structures as defined in equation (2), where $W_m$ is the measured linewidth, $L_i$ and $(V/I)_i$ are the segment length and $(V/I)$ values for each segment respectively, and $Rs_n$ is the representative value for the sheet resistance of the bridge resistor.

$$W_m = \frac{Rs_n L_i}{(V/I)_i} \qquad (2)$$

As there are multiple segments in each structure all having the same linewidth, extracted values for $W_m$ can

be taken and averaged to reduce measurement error.

*2) Multiple Segment Analysis:* Another approach to extracting ECD values from the test structures is to apply linear regression techniques to solve for linewidth. One point to note is that, due to the nature of photolithography and the etching of the silicon, the intersection of the line and the voltage taps produce facets of unknown dimensions. These facets present an electrical influence on the structure and hence introduce a source of uncertainty seen as a difference from the drawn line length. Furthermore, at small dimensions, where the tap width is of the same or larger dimension than the bridge structure, further variations in measurements due to the intersection of the taps are experienced. This value of line length variation is described by the term $\delta L$ [13], [14]. Equation (3) better defines the formula for determining the linewidth ($W_m$) of a given structure by including the numerical effect of the facets on the linelength [3].

$$W_m = \frac{Rs_n(L_i - \delta L)}{(V/I)_i} \tag{3}$$

This method requires that the test structure has $n \geq 2$ line segments each having the same linewidth. The process starts by plotting the $(V/I)$ values against the tap separation distances of the segments from which they were measured. Then by applying least squares fit a linear relation can be derived to relate the data points to one another as described in equation (4), where $m$ is the slope of the line and $b$ is the intercept of the line at the $L_i = 0$ axis.

$$(V/I)_i = mL_i + b \tag{4}$$

The standard equation of a line becomes apparent by re-writing equation (3) to the form seen in (5).

$$(V/I)_i = \left(\frac{Rs}{W_m}\right) L_i + \left(\frac{Rs_n}{W_m}\right)(-\delta L) \tag{5}$$

Therefore:

$$slope(m) = \left(\frac{Rs}{W_m}\right) \tag{6}$$

and

$$intercept(b) = \left(\frac{Rs}{W_m}\right)(-\delta L) \tag{7}$$

Equation (6) defines the relationship between Rs and measured linewidth while the $\delta L$ term is found by dividing the intercept of the line relating the segments by the slope of the same line as seen in (7). Using the slope of the line and a measured Rs value, the linewidth can be calculated.

[3]Lateral current flow through single-level patterning means that transmission line model issues do not have to be provided for.

*3) Multiple Structure Analysis:* This final technique further improves upon the values and data gathered from the multiple segment approach. As will be seen in the results presented later, issues arise when using the van der Pauw structures to determine values for Rs. Sheet resistance is used as a measure of resistivity of thin films that have a uniform thickness. One issue with the current van der Pauw structures is due to the facets (as explained earlier) which present an asymmetrical geometry in the structure, and therefore the film in the crosses is not of uniform thickness. Furthermore, when CMP is used, process induced effects, present in small lines used for ECD extraction, result in variations in Rs between the van der Pauw structures and the multiple tapped bridge resistors. The most predominant of these effects is the dishing of the copper lines which can also result in nonuniformity of Rs values within a single structure. For example, the extent of the dishing of the middle of a line may vary from the dishing at the intersection between the line and the taps, hence presenting thickness variations over the length of the structure. Therefore the Rs term used in equations (2), (3) and (6) is not necessarily truly representative of the sheet resistance of the copper in the structure. As a consequence alternative means for determining Rs values need to be implemented.

This is achieved by comparing drawn linewidth against the slope values for each device, provided there are $n \geq 3$ structures. The drawn linewidths are used to provide a measure of the relation between the full set of structures without incorporating any process bias that may be present in the fabricated structures. By applying non-linear regression with a least squares fit approach, a curve described by equation (8) can be used to represent the relationship between multiple structures with different drawn linewidths.

$$m_i = \frac{a}{(W_m)_i^k} \tag{8}$$

In this equation $m_i$ is the slope of a structure as determined from (4), *a* is a term primarily proportional to the sheet resistance of the measured structures, and *k* is proportional to the range in measured linewidth $(W_m)_i$ from the result of the regression fit. With values for *a* and *k* the linewidth for each structure can be calculated by substituting the slope of each line into (8) and solving for $(W_m)_i$.

## IV. **Results**

### *A. Sheet Resistance*

A contour plot can be generated to represent the sheet resistance over a complete die using data measured from a six by three array of van der Pauw structures. A typical example of one of these contour plots can be seen in Fig 4. These data display a systematic variation for the different types of van der Pauw structures within a single die. There are a number of process induced

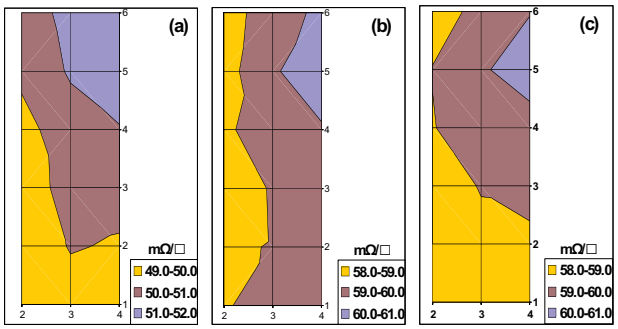


Fig. 4. Contour plot of sheet resistance over the surface of a single die taken from the van-der-Pauw structures shown in Fig. 2 : (a) Greek Cross, (b) Corner Tapped Box Cross, and (c) Side Tapped Box Cross

effects which can be used to explain this occurrence. The first is due to the dependence of the process on CMP for both nitride and copper planarization, where dishing can vary over the wafer as well as within each die. Another source is the trench depth in which the copper is deposited, which can vary in the trench etch stage of the fabrication. One important factor to note is that the mask set used to define these structures was intended for use on doped SOI substrates which would not have undergone a CMP step and therefore be more likely to have a uniform distribution of sheet resistance over a single die. For this reason, the NIST 35 design includes large (20 μm) crosses/boxes on each of the van der Pauw structures to allow for more accurate measurements of sheet resistance. However these large features pose a problem for the copper CMP stage as larger linewidths are known to dish to a greater extent than smaller linewidths [3]. This leads to the need to use smaller dimensions to reduce the dishing of the copper and provide more appropriate measurements of sheet resistance with minimal variation.

The values obtained for the sheet resistance from Greek Cross test structures are consistently lower than the other two structures. This is made apparent by an average sheet resistance of 50 mΩ/□ (implying a copper thickness of 336 nm) for the Greek Cross while the values for the corner tapped and side tapped box are both 59 mΩ/□ (implying a copper thickness of 284 nm). This suggests that the thickness varies between the Greek Cross and the other two structures by roughly 50 nm. Once more, dishing can be used to explain this occurrence. The dimensions of the arms of the Greek cross structure are the same as the body (20 μm), while both the Box Cross structures employ smaller arms for the taps (5 μm) yet maintain a 20 μm body. Because of this, the measurement from the Greek Cross structure is more likely to be influenced by dishing near to the centre of the cross than the other two structures. By observing the contour plots of sheet resistance it can be noted that, while there is a general agreement in the sheet resistance variation over the whole die, there is no specific agreed value between the three structures for each location.

### B. Linewidth

Linewidths have been measured electrically, from the same six by three array as the sheet resistance measurements, to fully assess the capabilities of the current design on copper ECD extraction. Results are presented for each of the analysis approaches described in section III-B. As a means for comparison, SEM images have been used to provide a value for linewidth, which in this case is defined by the width of the copper on the surface of the wafer. While the SEM measurements do not produce results to the degree of accuracy required for CD metrology, they do provide a baseline for comparing the analysis methods. For situations where sheet resistance measurements are required to calculate linewidth, the average of estimates produced by all three van der Pauw structures for each location on the die are used. Data from the analysis methods is presented as a graph of drawn linewidth minus the extracted linewidth versus the drawn linewidth. This applies for both ECD values as well as SEM linewidth values.

*1) Individual Segment Analysis:* The individual segment analysis was conducted as described previously. A plot of the results gathered from the average of 5 segments of the bridge resistor using this method for the array of 18 structures is presented in Fig. 5. The error bars on the individual data points represent the range of linewidths extracted from each segment of the multiple tapped bridge resistor. These errors are proportional to the linewidth, so as the linewidth decreases the range in linewidth values also decrease. One source for the difference between the ECD values and the SEM measurements is the use of the sheet resistance structures that are physically separate from the linewidth structures and subject to dishing effects caused by locality. Furthermore, the van der Pauw structures are 20 μm wide while the linewidth structures range from 10 μm to 0.55 μm. This introduces further effects of dishing during CMP which are related to feature size.

*2) Multiple Segment Analysis:* Using the linear regression technique, slope values $(m)$ were determined for each linewidth structure. By using the average measured $Rs$ value from the van der Pauw structures in closest proximity, the linewidth was calculated using equation (6). A plot of the results using this method for all 18 structures is presented in Fig. 6. These values are in better agreement with the SEM values than those derived using the individual segment analysis. However, repeating the individual segment analysis with the $\delta L$ correction makes no improvement in the present set of data.

*3) Multiple Structure Analysis:* Equation (8) is applied to determine the relationship between the slopes and drawn linewidths of the structures in the six by three

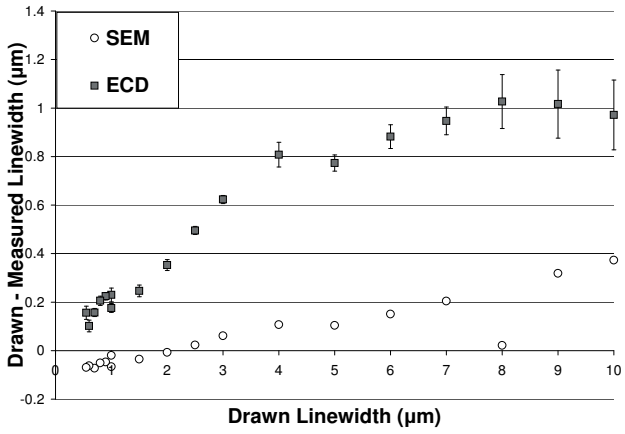


Fig. 5. Plot of drawn linewidth - measured linewidth for individual segment analysis

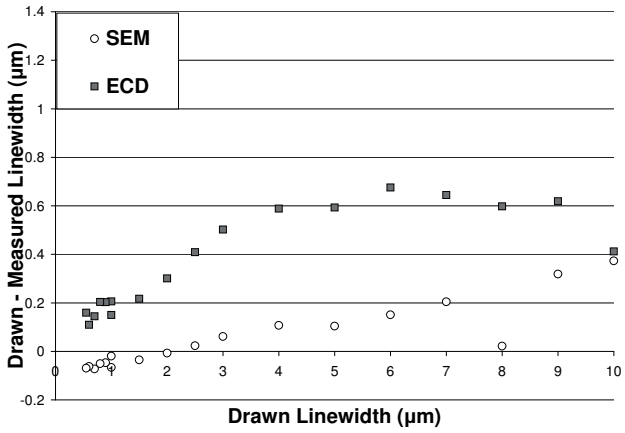


Fig. 6. Plot of drawn linewidth - measured linewidth for linear regression analysis

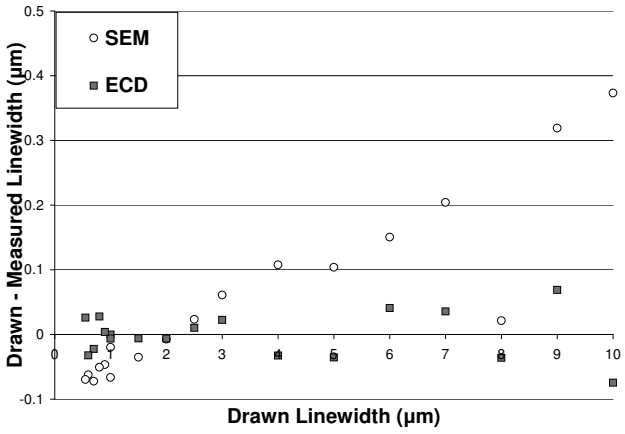


Fig. 7. Plot of drawn linewidth - measured linewidth for multiple structure analysis of separate columns

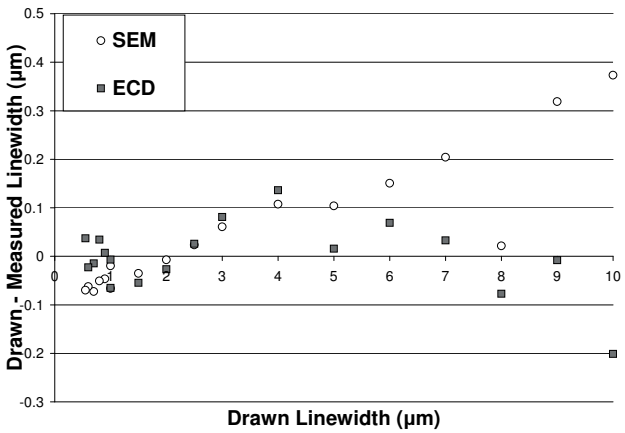


Fig. 8. Plot of drawn linewidth - measured linewidth for multiple structure analysis with all structures

array. The first approach for this technique was to analyse each column individually and plot the results. From Fig. 7 it can be seen that the values extracted for ECD measurements are in better agreement with the drawn linewidth values.

The second approach uses data from the entire array to determine the non-linear relationship and hence can be used as a smoothing for any abnormalities in individual structures. Results from this method are presented in Fig. 8. Once again these data are in agreement with the drawn linewidths, however there is a noticeably better fit to the SEM measurements.

## V. **Conclusions**

Structures have been fabricated using a novel process to produce all-copper ECD test structures. Electrical measurements have been taken to extract various parameters and derive values for sheet resistance and linewidth. Based on data gathered from extensive electrical measurements of the copper interconnect features, issues with the current design as well as the fabrication process have been highlighted. In light of the diverse range of values for sheet resistance, the need to control the dishing of the copper and nitride has become much more critical. This can be achieved with the combination of different CMP slurries and polishing pads, as well as improvements to the process recipes. Dishing of copper lines is a well known phenomenon amongst the semiconductor community, and much work is ongoing to improve this aspect of copper CMP.

The work conducted for the purposes of this paper has highlighted an approach to analysing the data from all copper test structures which yields the best results. Future process improvements can be closely monitored to observe their effect on the extraction of ECD values. Ongoing work will involve the use of more precise CD

measurement tools to determine the linewidth of the copper interconnects and serve as calibration/reference values for more in depth analysis of the presented techniques. For the purpose of this exploratory work, g-line lithography was used to define the pattern. However more advanced technologies, such as i-line and Deep UV (DUV) lithography, can be employed to print much smaller features. Analysis of these smaller features will bring the work in line with current roadmap predictions for copper ECD values.

## VI. **Acknowledgements**

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## REFERENCES

[1] M. W. Cresswell, N. Arora, R. A. Allen, C. E. Murabito, C. Richter, A. Gupta, L. W. Linholm, D. Pachura, and P. Bendix, "Test chip for electrical linewidth of copper-interconnect features and related parameters," in *Int. Conference on Microelectronic Test Structures*, vol. 14, March 2001, pp. 183–188.

[2] T. Turner, "Requirements for dual-damascene cu-linewidth resistivity measurements," *Solid State Technology*, vol. 43, no. 4, pp. 89–94, April 2000.

[3] S. Smith, A. J. Walton, A. W. S. Ross, G. K. H. Bodammer, and J. T. M. Stevenson, "Evaluation of sheet resistance and electrical linewidth measurement techniques for copper damascene interonnect," *Solid State Technology*, vol. 15, no. 2, pp. 214–222, May 2002.

[4] B. J. R. Shulver, A. S. Bunting, A. M. Gundlach, L. I. Haworth, A. W. S. Ross, A. J. Snell, J. T. M. Stevenson, A. J. Walton, R. A. Allen, and M. W. Cresswell, "Design and fabrication of a copper test structure for use as an electrical critical dimension reference," in *Microelectronic Test Structures, 2006 IEEE International Conference on*, 6-9 March 2006, pp. 124–129.

[5] R. A. Allen, B. A. Ende, M. W. Cresswell, C. E. Murabito, T. J. Headley, W. F. Gutherie, L. W. Linholm, C. H. Ellenwood, and E. H. Bogardus, "Test structures for referencing electrical linewidth measurments to silicon lattice parameters using HRTEM," *IEEE Transactions on Semiconductor Manufacturing*, vol. 16, no. 2, pp. 239–248, 2003.

[6] R. A. Allen, T. J. Headley, S. C. Everist, R. Ghoshtagore, M. W. Cresswell, and L. W. Linholm, "High-resolution transmission electron microscopy calibration of critical dimension (CD) reference materials," *IEEE Transactions on Semiconductor Manufacturing*, vol. 14, no. 1, pp. 26–31, 2001.

[7] T. Hatsuzawa and K. Toyoda, "Critical dimension measurements by electron and optical beams for the establishment of linewidth standards," in *Proc. IEEE 1992 Int. Microelectronic Test Structures*, vol. 5, March 1992, pp. 180–184.

[8] R. A. Allen, M. W. Cresswell, and L. W. Linholm, "Junction-isolated electrical test structures for critical dimension calibration standards," *Semiconductor Manufacturing, IEEE Transactions on*, vol. 17, no. 2, pp. 79–83, May 2004.

[9] M. W. Cresswell, R. G. Dixson, W. F. Guthrie, R. A. Allen, C. E. Murabito, B. Park, J. V. Martinez, and A. Hunt, "Critical dimension reference features with sub-five nanometer uncertainty," in *SPIE 30th International Symposium Microlithography Metrology, Inspection, and Process Control*, vol. 5752, San Jose, CA, May 30. 2005, pp. 288–303.

[10] M. W. Cresswell and R. A. Allen, *Handbook of Silicon Semiconductor Metrology*. Marcel Dekker, Inc, 2001, ch. Electrical CD Metrology and Related Reference Materials, pp. 377–410.

[11] L. J. van der Pauw, "A method of measuring specific resistivity and Hall effects of discs of arbitrary shape," *Phillips Res. Rep.*, vol. 13, pp. 1–9, 1958.

[12] M. W. Cresswell, J. J. Sniegowski, R. N. Ghoshtagore, R. A. Allen, W. F. Guthrie, A. Gurnell, L. W. Linholm, R. G. Dixson, and E. C. Teague, "Recent developments in electrical linewidth and overlay metrology for integrated circuit fabrication processes," *Jpn. J. Appl. Phys.*, vol. 35, pp. 6597–6609, 1996.

[13] M. W. Cresswell, R. A. Allen, and L. W. Linholm, "Linewidth micro-bridge test structure," *US Patent 5,247,262*, 1993.

[14] R. A. Allen, M. W. Cresswell, and L. M. Buck, "A new test structure for the electrical measurement of the width of short features with arbitrarily wide voltage taps," *Electron Device Letters, IEEE*, vol. 13, no. 6, pp. 322–324, June 1992.