



Practical Aspects Impacting *Time Synchronization Data Quality* in Semiconductor Manufacturing

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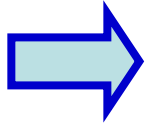
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Outline



- **Why is time synchronization so important in semiconductor manufacturing?**
- Components in the end-to-end synchronization problem
- Currents efforts in semiconductor manufacturing impacting time synchronization data quality
 - NIST and the University of Michigan
- Key points and future efforts



Time Synchronization and Manufacturing

Manufacturing Automation

- Process Control
- Coordination among tools
- Scheduling/Dispatching



Robotics Coordination for Auto Industry



Fault Diagnosis for Power Industry

Test and Measurement

- Fault Diagnosis

Network Operations

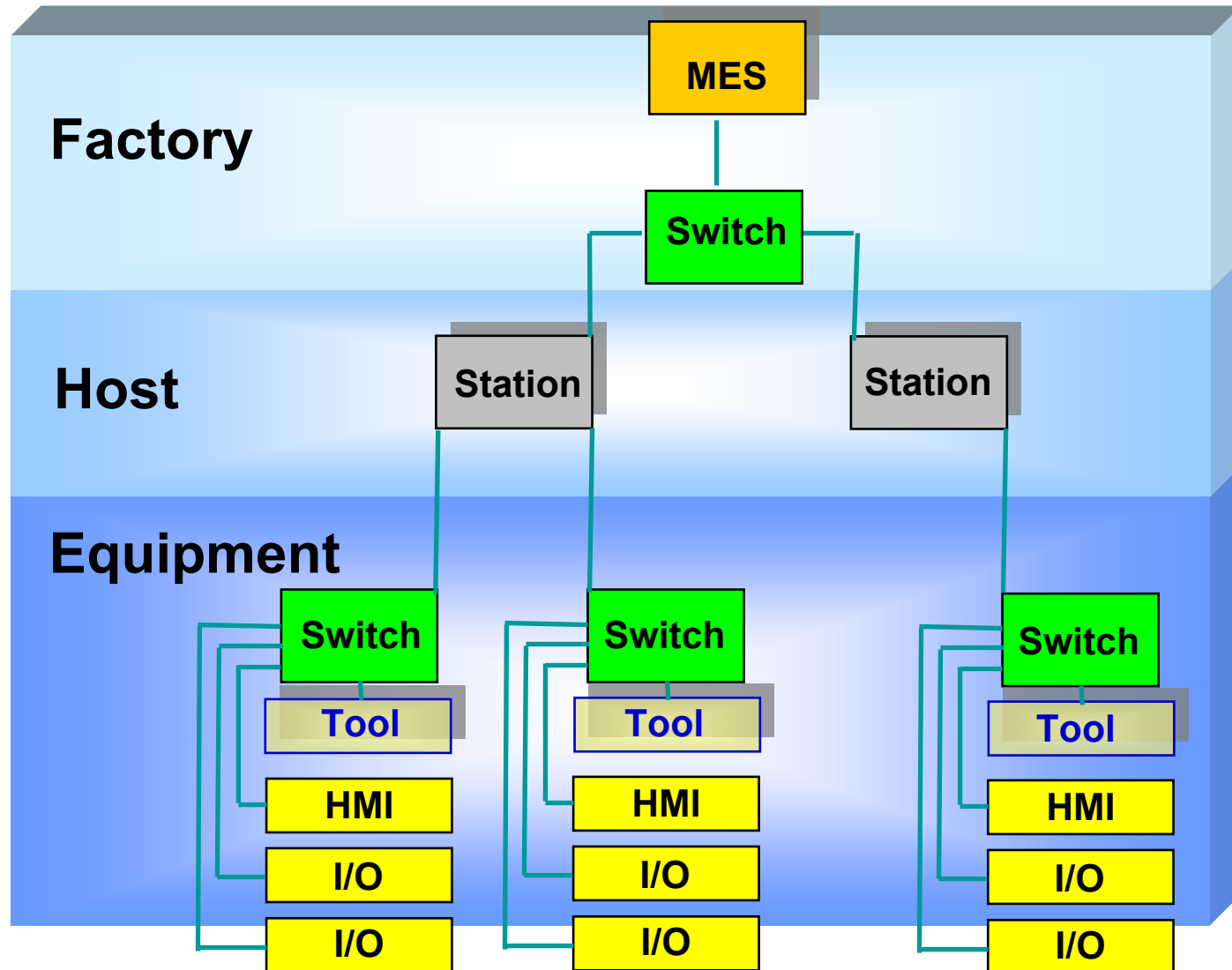
- Security
- QoS measurement



Motivation: The Move to Networks

Ethernet Everywhere!

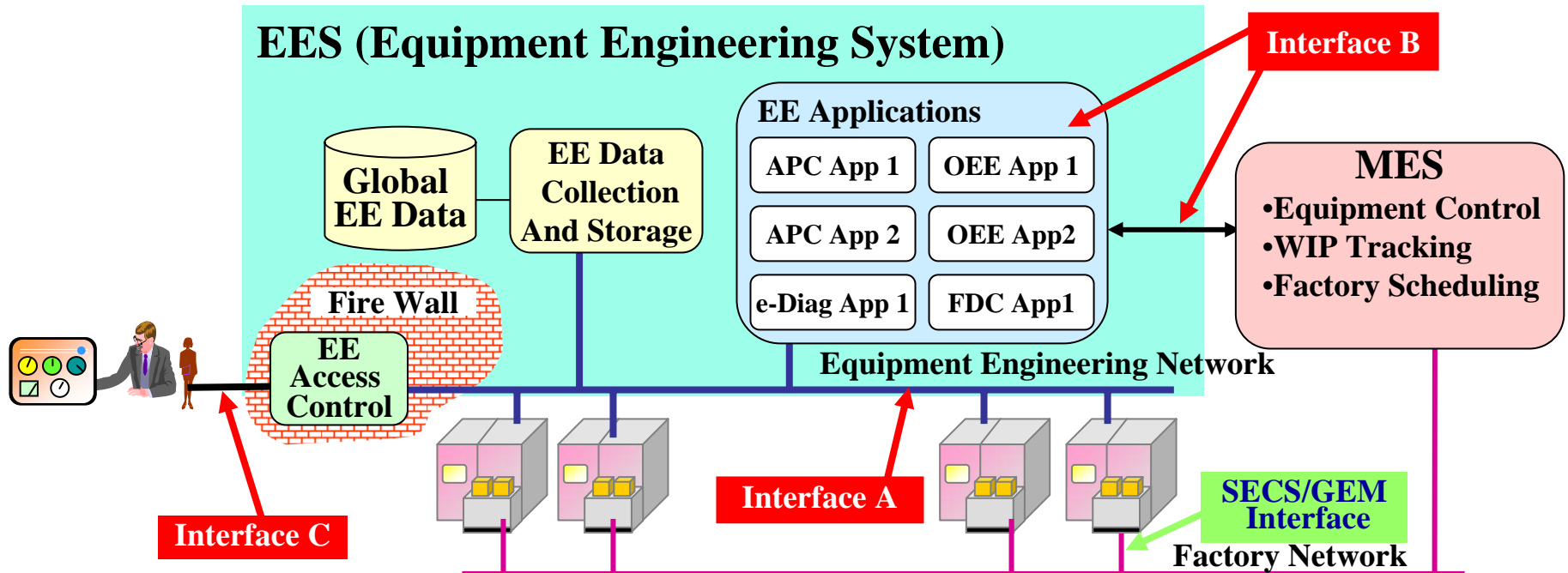
- Interfaces A, B and C
- EDA, PCS, e-diagnostics
- HSMS
- XML, VPN, OPC
- MES to I/O Level



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Semiconductor Factory

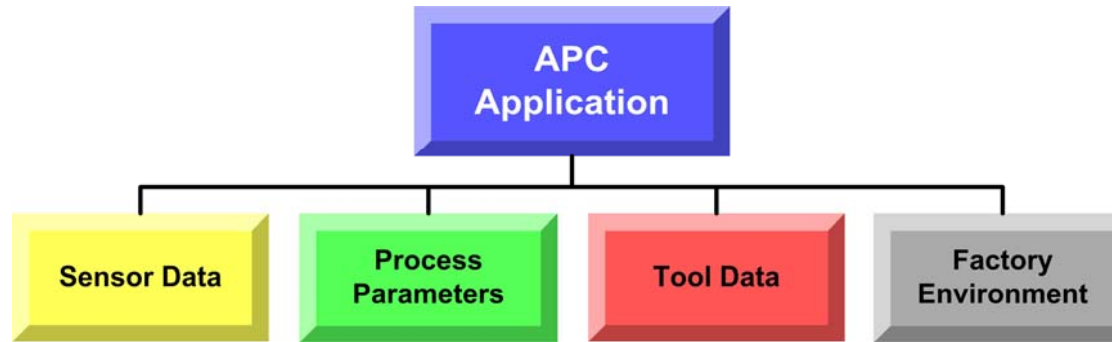


•Interface "A" Components

- Process Control and Equipment Operational Data
- Host-Independent Data Collection
- Data Collection Plans → E134
- Equipment Self-Description → E125
- Authentication and Authorization → E132



Motivation in Chip Manufacturing



Precision Time Stamping to Merge Various Data Streams

Advanced Process Control:

- Fault Detection Classification (FDC)
- e-Diagnostics
- Process optimization
- Virtual metrology

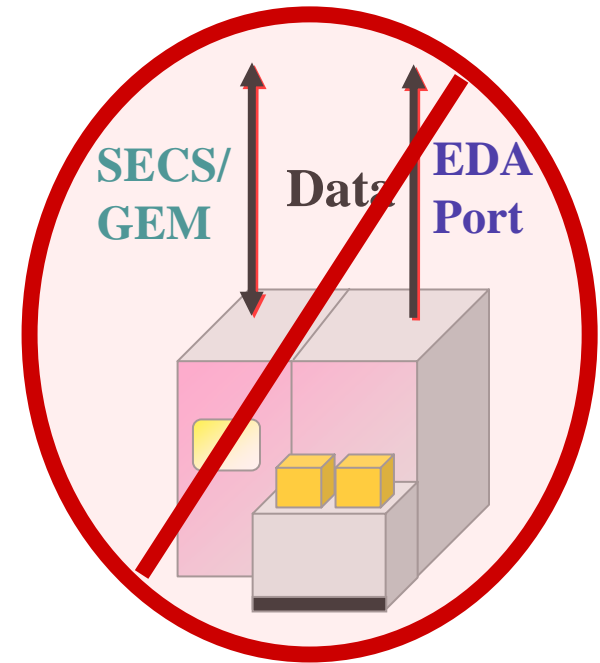
Precision time-stamping and time synchronization:

- Merging data from heterogeneous sources
- Maintain data and event ordering
- Improve multivariate, advanced correlation and analysis
- Expose new cause-effect relationships



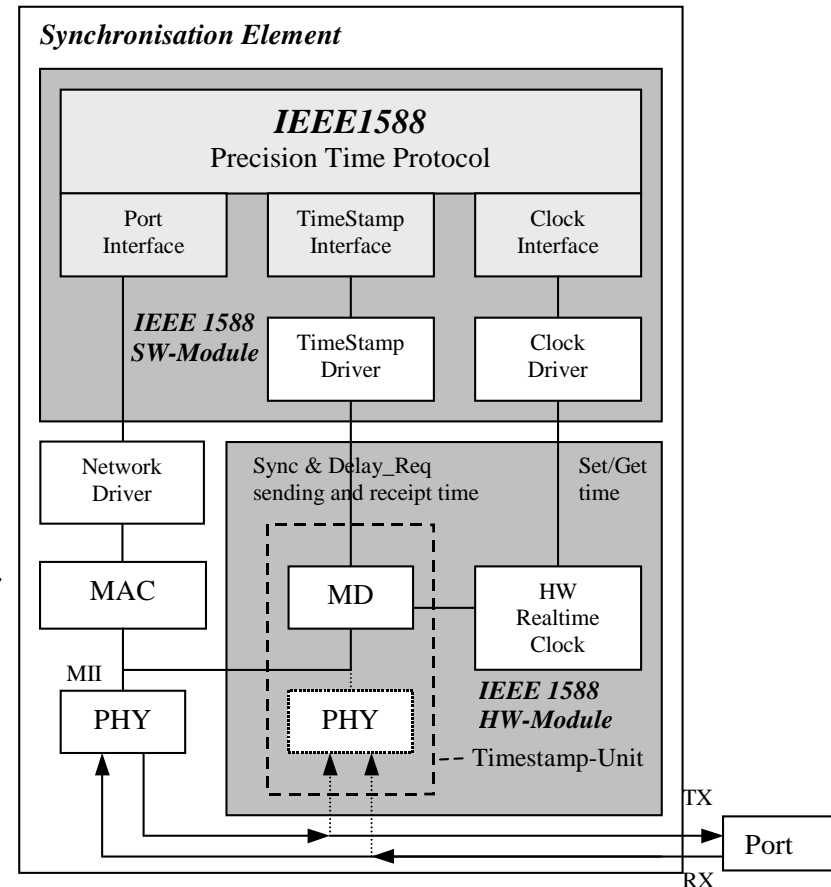
Common Time Sync. Pain Points in APC

- Events and data are received out-of-order
- Inability to support high data collection rates with good data quality
- **Cannot synchronize data across multiple systems (e.g., equipment & metrology systems)**
- **“False Positives” in fault detection systems bring equipment down unnecessarily**
 - Out-of-order data, poor time-stamping
 - Time-stamping at point of sending instead of point of event occurrence
- “Out-of-control” situations for R2R controllers
 - Poor data quality due to delay and delay variability
- Inability to migrate from the equipment level to the factory-wide level with APC systems
- Etc...



Solutions for Time Synchronization

- NTP 4.0 or SNTP 4.0
 - Software only
 - 50 us to 50 ms accuracy, depending largely on software environment
 - More mature
- ANSI/IEEE 1588 – (IEC 61588)
 - Software and hardware
 - Approx 100ns accuracy
 - Infancy in standard and solutions



..... necessary if no MII- interface available

MD – Message Detector for *Sync* and *Delay_Request* packets

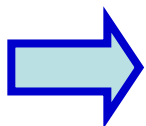


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Outline

- Why is time synchronization so important in semiconductor manufacturing?



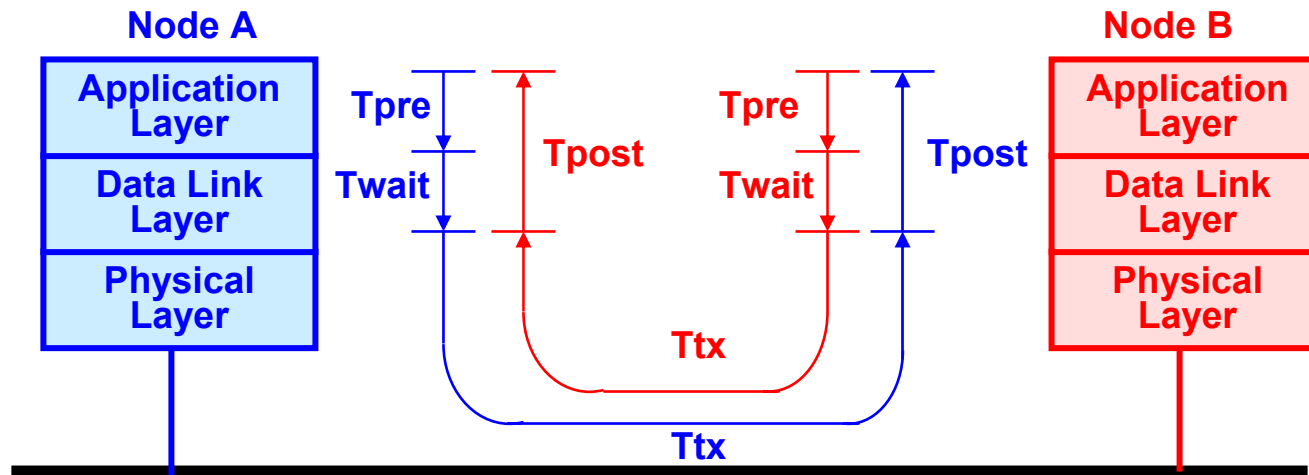
- **Components in the end-to-end synchronization problem**
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Components of Delay

Where are the sources of delay and variability?

- Network and nodes



- Total end-to-end delay is the sum of
 - Pre-processing time: microprocessor
 - Waiting time: network protocol - MAC
 - Transmission time: data rate & length
 - Post-processing time: microprocessor

Device
Delays

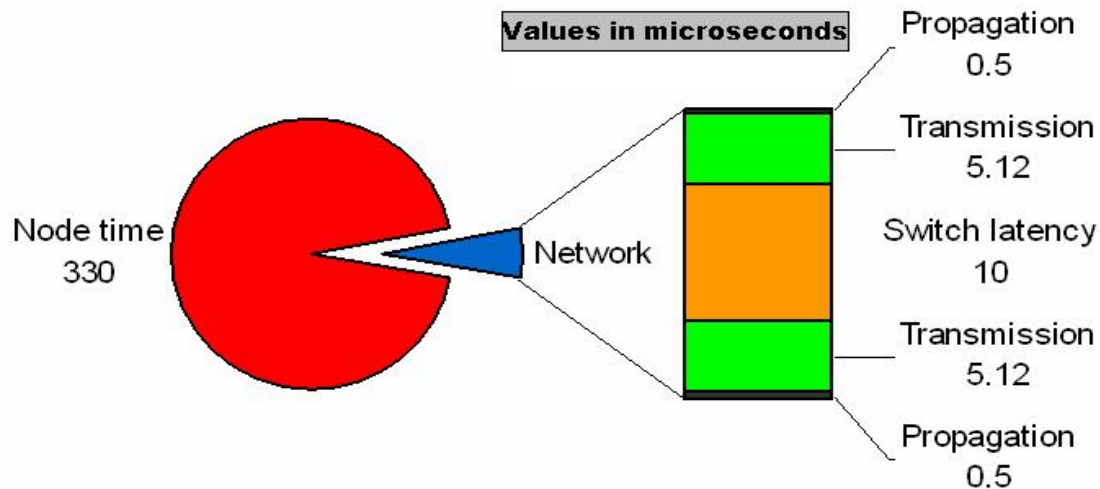
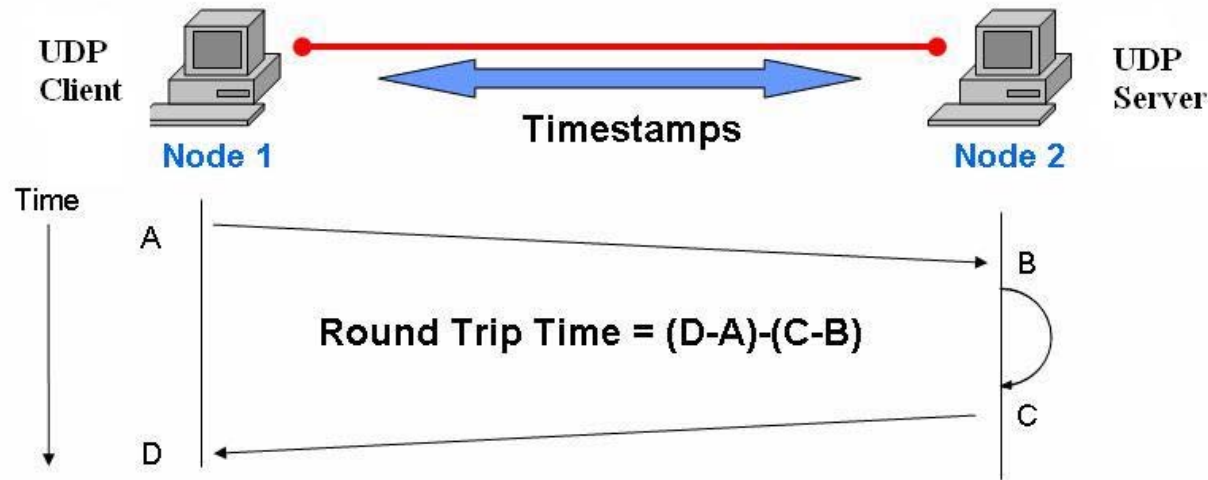
Network
Delays



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Experimental Analysis



**The Delay
is in the
Node Software**

**(T_{pre} , T_{wait}
and T_{post})**

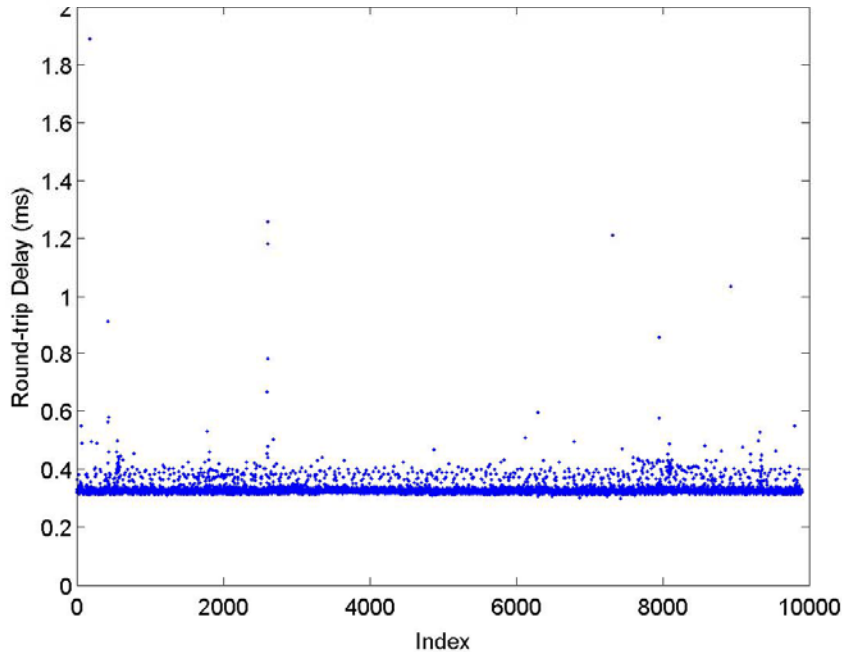


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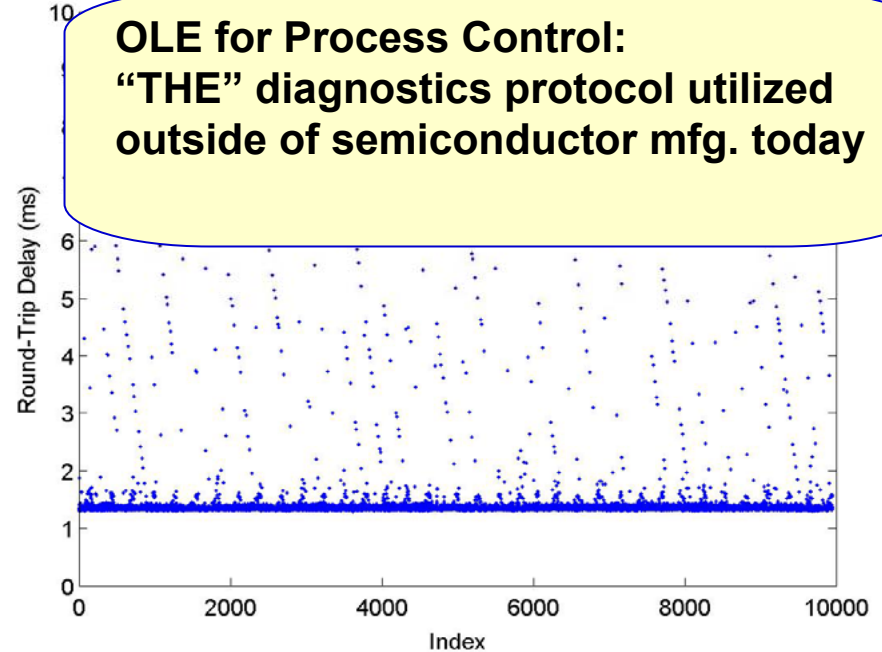
Application level delays

- UDP round-trip delays (100Mbps switched network)



- Mean = 0.33ms, max = 1.89ms
- Stdev = 0.03ms

- OPC round-trip delays (100Mbps switched network)



OLE for Process Control:
“THE” diagnostics protocol utilized
outside of semiconductor mfg. today

- Mean = 1.5ms, max = 16.8ms
- Stdev = 0.81ms

The Delay and delay Variability
is in the Node Software

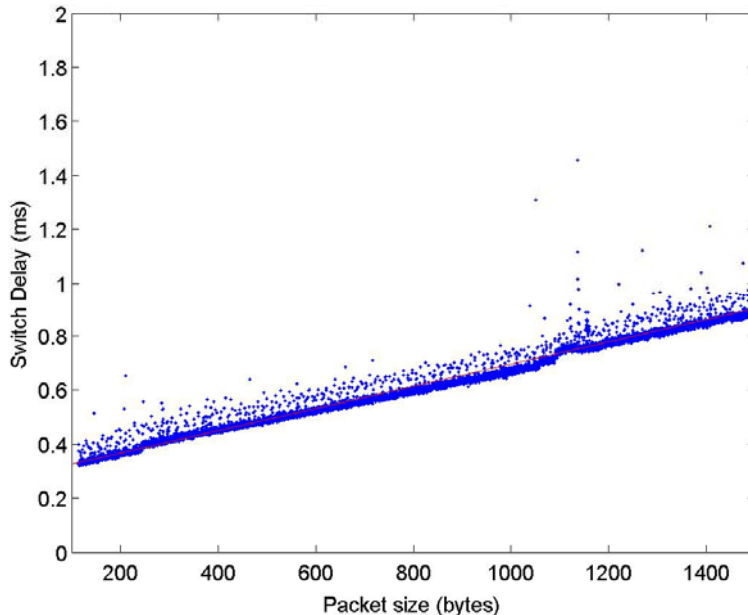


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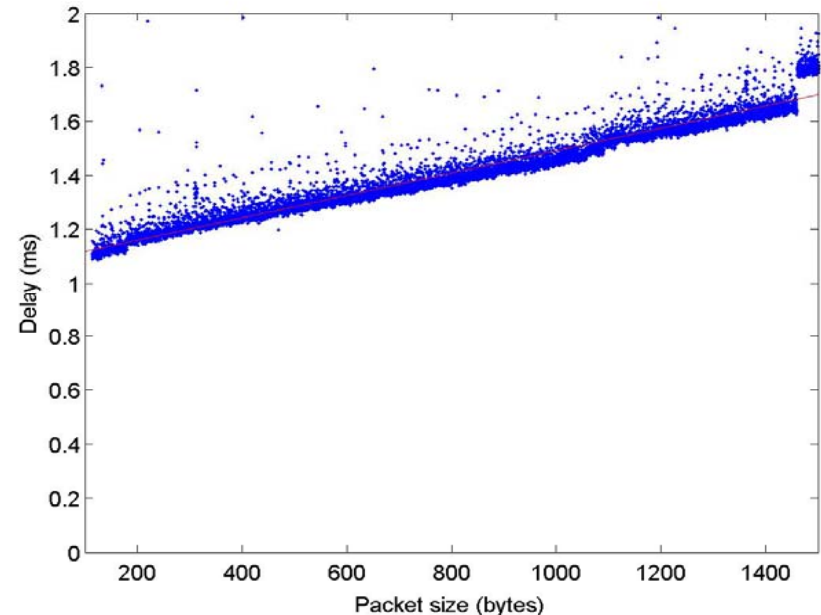
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Varying packet size

- UDP round-trip delays (100Mbps switched network)
- VPN round-trip delays (100Mbps switched network)



- Slope = $0.411\mu\text{s/bit}$
 - Theory: $0.32\mu\text{s/bit}$
- Intercept: 0.285ms



- Slope = $0.848\mu\text{s/bit}$
- Intercept: 1.07ms
- Using DES (data encrypt. std)



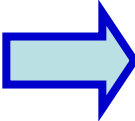
Network Delay Test Results

	UDP	VPN (UDP)	OPC (TCP)		DeviceNet
Delay Average (ms)	0.33	1.21	1.48		0.3-1.2
Delay Variation (3σ) (ms)	0.09	0.49	2.43		0.005-0.2
Min. Network Delay Contribution (ms)	0.035	0.035	0.035		0.188
% of Delay Due to Network	11%	3%	2%		63%

The Message:

- We need time synchronization and time-stamping to mitigate delay and delay variability disturbances of end-to-end network communication
- We need standards for time synchronization and *when* to timestamp information in the end-to-end communication path
- Using synchronization and time-stamping, we can decouple application node time from communication network time

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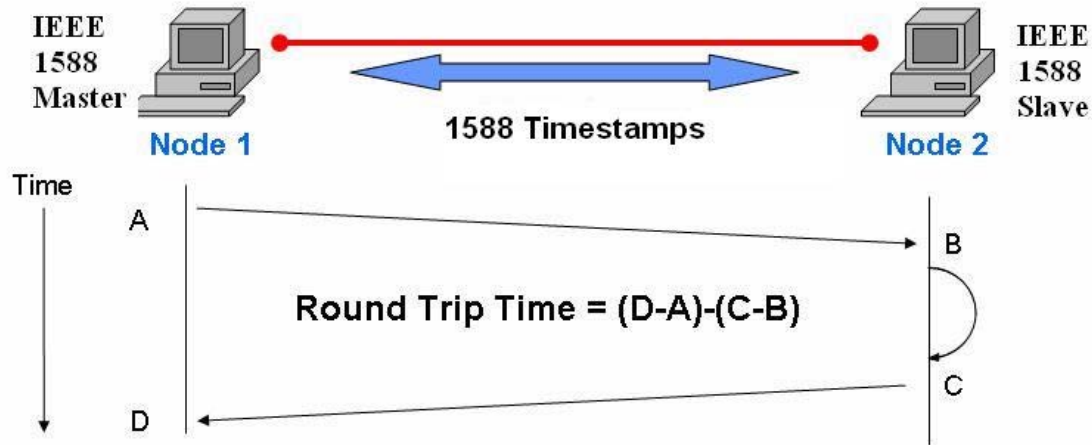
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- **IEEE 1588 testbed in operation**
 - 1588 hardware I/O cards
 - LabVIEW as the application software
 - XML traffic generators
 - Routines for encapsulation, e.g., VPN, OPC, UDP, as necessary
- **Performance testing of IEEE 1588 for semiconductor manufacturing applications**
 - Data collection
 - Event reporting
 - Remote monitoring



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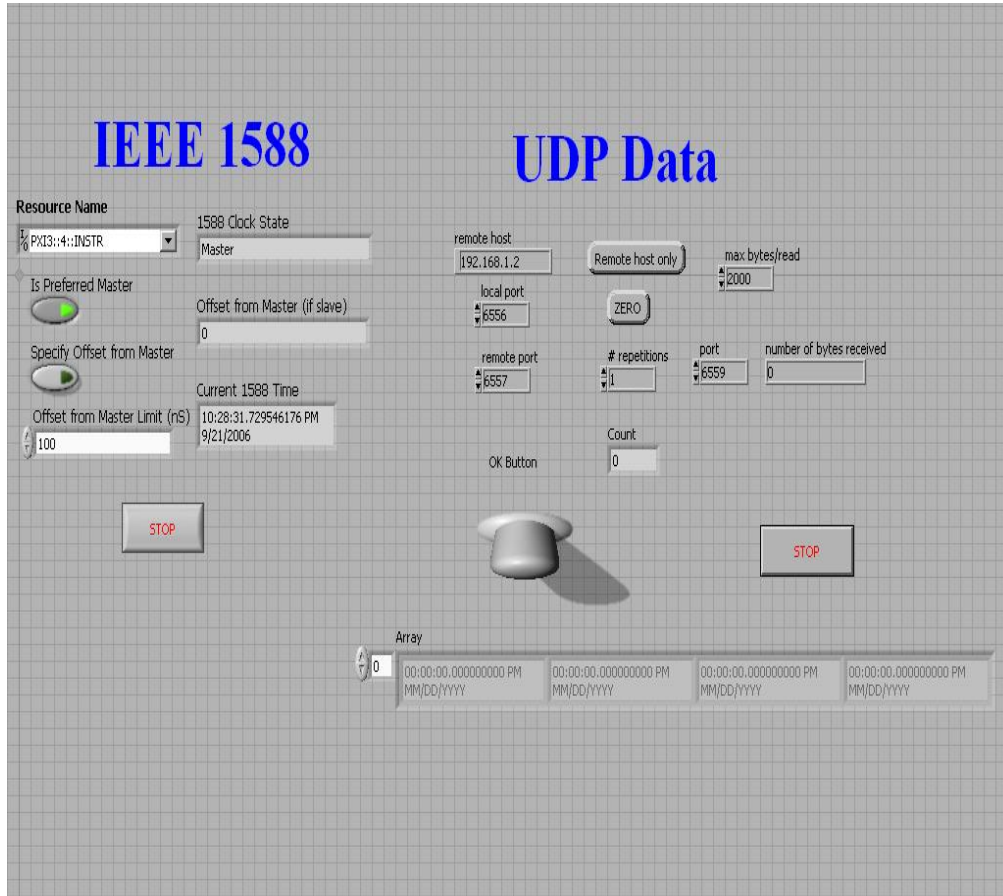
- Tests with 1588



- Tests designed to see effect of 1588 time-stamping and synchronization
- Nodes synchronized through IEEE 1588 protocol
- Time-stamping through 1588 clock
- 1588 timestamps exchanged



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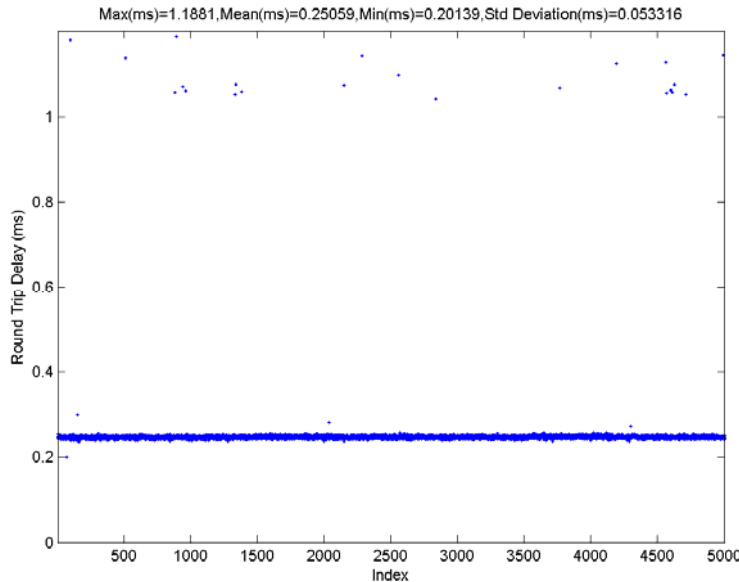
- LabVIEW is used as the application layer for programming
- Time synchronization interval for PTP set at two seconds
- Interface through LabVIEW for accessing 1588 clock
- UDP data time-stamped with 1588 clock and exchanged
- UDP Round Trip time calculated from data exchange



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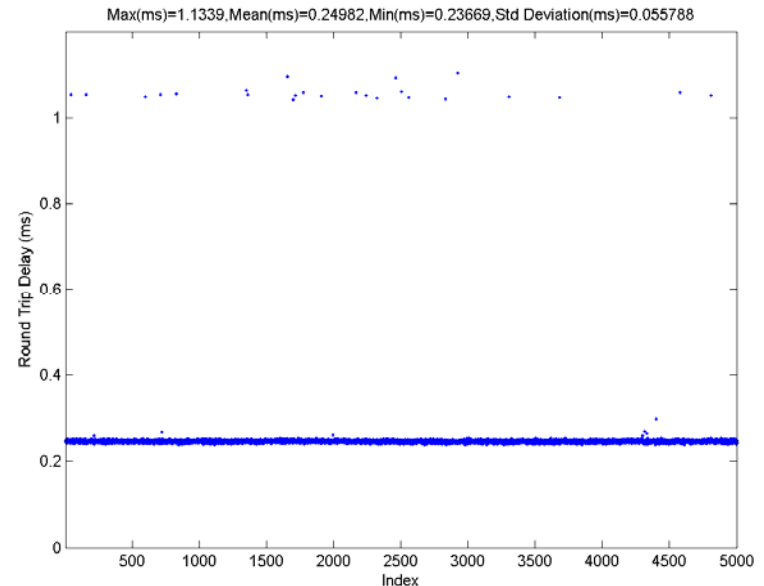
UDP Round Trip delays for 100 Mbps network (250ms delay between packets)

UDP Round Trip Delay with IEEE 1588 Synchronization and Timestamping over Crossover Cable



Crossover Cable

UDP Round Trip Delay with IEEE 1588 Synchronization and Timestamping over Switch



Switch

Values for 5000 packets with a delay of 250ms between packets

	Max (ms)	Mean (ms)	Min (ms)	Std Dev (ms)
Crossover	1.188	0.251	0.201	0.053
Switch	1.134	0.250	0.237	0.056



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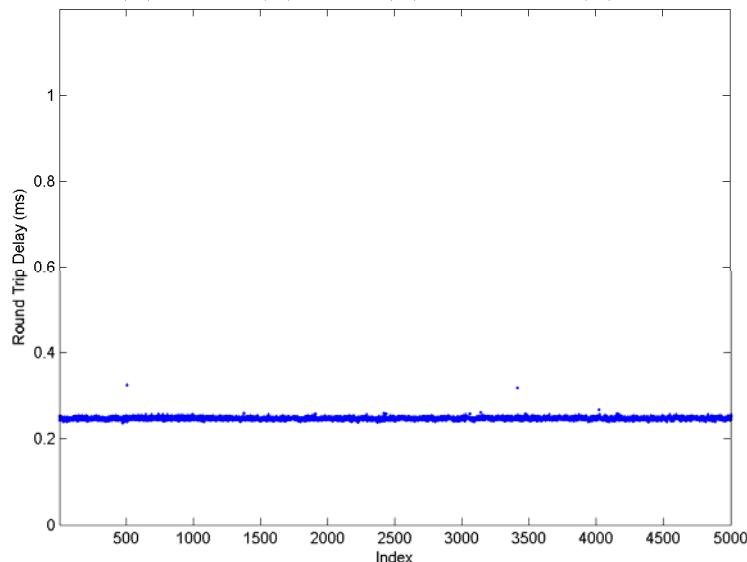
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UDP Round Trip delays for 100 Mbps network (1s delay between packets)

UDP Round Trip Delay with IEEE 1588 Synchronization and Timestamping over Crossover Cable

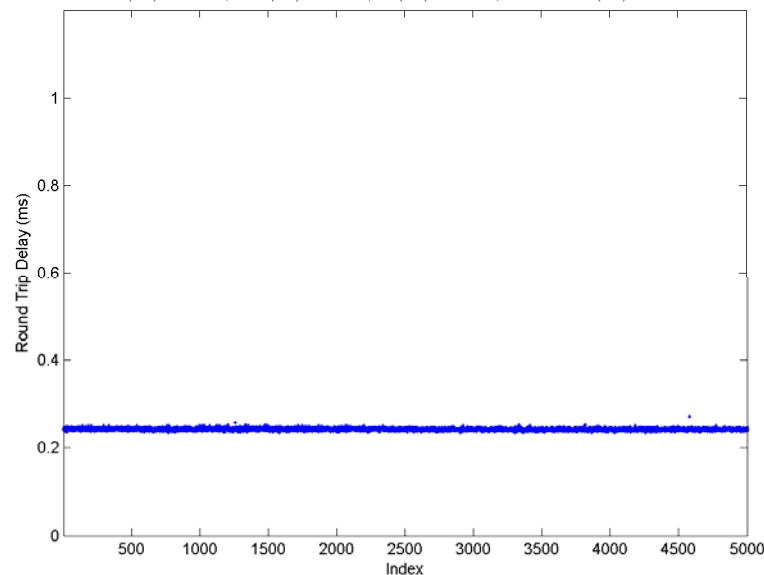
Max(ms)=0.32454, Mean(ms)=0.24765, Min(ms)=0.23581, Std Deviation(ms)=0.0031538



Crossover Cable

UDP Round Trip Delay with IEEE 1588 Synchronization and Timestamping over Switch

Max(ms)=0.31739, Mean(ms)=0.24296, Min(ms)=0.23368, Std Deviation(ms)=0.0028346



Switch

Values for 5000 packets with a delay of 1s between packets

	Max (ms)	Mean (ms)	Min (ms)	Std Dev (ms)
Crossover	0.325	0.248	0.236	0.003
Switch	0.317	0.243	0.234	0.003



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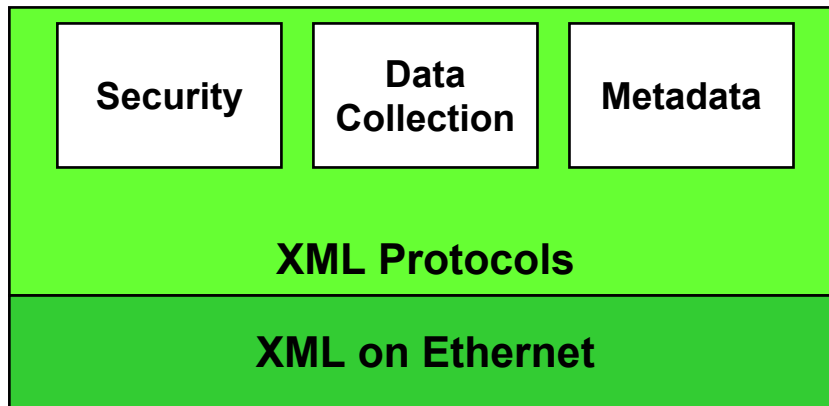
- **Summary of initial results**
 - With 1588 time-stamping, increasing the delay between packets led to lower values of jitter for the UDP round trip delay
 - LabVIEW used on Windows (OS used) may introduce variability
 - UDP data exchanged is time-stamped through the application (LabVIEW) GUI, no hardware time-stamping of data
- **Future tests**
 - Use Linux OS and 1588 time-stamping



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- **Next Steps**

- Benchmark common protocol scenarios (XML, VPN, etc.)



- Interface “A” traffic volume analysis and performance benchmarking

- Simple equipment EDA traffic simulators

- APC scenario analysis

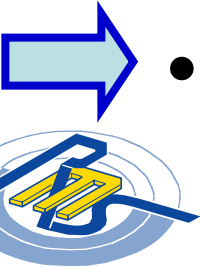
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Traffic patterns similar to Interface A

- **Outcome**

- Exploration of Time Synchronization for Semiconductor Manufacturing
- Identification of weak links in equipment, software systems, standards, etc.
- Input into SEMI standards effort



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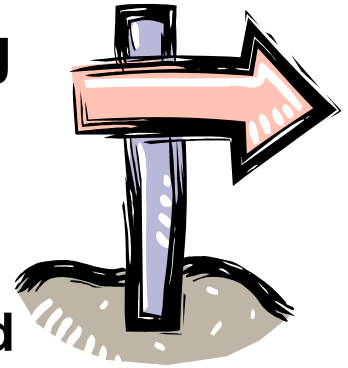
Key Points

- Many efforts in implementing EDA and PCS implementation will fail if data quality is not addressed
- Lack of time synchronization and accurate time-stamping is a common source of poor data quality
- The weak link is often the tool software performance, so *where you timestamp* is very important
- NIST, The University of Michigan and SEMI are working together to address this issue, with the end result being standards and prototypes that will impact PCS, EDA and e-diagnostics



Future Efforts

- **Identify and quantify the weak links in timing and time synchronization for APC**
- **Education**
 - When and how to apply time synchronization, and at what level
- **Simulation of semiconductor factory environment**
- **Provide cost / benefit analysis**
 - What level of time synchronization is needed at various places throughout the fab; e.g., is hardware time synchronization required?
- **SEMI standards for time synchronization and time-stamping**



Thank You !! ☺

- **For further information**

- James Moyne: moyne@umich.edu
- UM-ERC-RMS: <http://erc.engin.umich.edu>
- J. T. Parrott, J. R. Moyne, D. M. Tilbury, "Experimental Determination of Network Quality of Service in Ethernet: UDP, OPC, and VPN," *Proceedings of the American Control Conference*, Minneapolis, MN, June 2006.

- **Acknowledgments**

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- **Questions?**



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