# Design of SNS Josephson Arrays for High Voltage Applications

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***Abstract*—The voltage from a single, microwave-biased Josephson junction is a small quantity; thus useful voltages are generated only through series arrays of many thousands of junctions. Arrays of superconductor-normal metal-superconductor junctions have been fabricated and tested with as many as 16,500 junctions per array. The arrays are optimized for the highest voltage operation with the largest operating margins for the current bias. Measurements show that these arrays, driven with 20 GHz microwaves, generate a dc voltage greater than 680 mV per array with a dc bias margin over 1 mA. To increase the microwave uniformity across the array, the transmission line impedance has been tapered. By use of this technique, ac Josephson voltages over 110 $\mathrm{mV_{rms}}$ per array have been generated, also with over 1 mA dc bias margin.**

***Index Terms*—Josephson voltage standard, microwave devices, SNS junctions.**

## I. Introduction

PROGRAMMABLE dc and ac Josephson Voltage Standards (PJVS and acJVS) need the highest possible voltage per array to meet the measurement needs of the metrology community. NIST has been using superconductor-normal metal–superconductor (SNS) [1] Josephson junctions rather than superconductor-insulator-superconductor (SIS) or SINIS [2] junctions because SNS junctions are typically more reproducible to fabricate and have larger absolute current margins than junctions whose barriers dependent on thin oxides. The main disadvantages of using SNS junctions stem from the energy dissipation in the junctions, namely heating and microwave attenuation. Thermal management issues have been addressed previously [3]. This paper will concentrate on new work increasing the maximum voltage per array and the resulting issue of microwave uniformity throughout an array.

The voltage from an array of Josephson junctions is given by: $V = Nnf/K_J$, where $N$ is the number of junctions in the array, $n$ is the constant voltage step number (typically $n = 1$), $f$ is the drive frequency, and $K_J$ is the Josephson constant ($K_J = 0.4835979\ \mathrm{GHz}/\mu\mathrm{V}$). Typically for distributed arrays of SNS junctions, most of the microwave power is dissipated in termination resistors, thus requiring applied power substantially higher than that required to bias only the junctions in the array. If dissipative junctions are used, the theoretical maximum voltage per array is also independent of frequency [4]. Furthermore, for acJVS circuits, available high-speed code generators have a limited number of output channels, thus limiting the number of arrays that can be biased in parallel. Thus, for both dc and ac applications, the only way to maximize the total voltage is to increase the number of junctions in each array. Typical SNS arrays used in a 1 Volt PJVS system have used 4,000 to 5,000 junctions per array for ∼150 mV/array [1], [5]. Typical SNS arrays used in the acJVS have ∼2500 junctions per array for $\sim 50\ \mathrm{mV_{rms}}$/array [6].

Microwave attenuation is caused by the normal-state resistance of the junctions embedded in a coplanar transmission line, leading to a structure similar to that of a lossy transmission line in which the power decays as $exp(-NR_n/Z)$, where $R_n$ is the normal-state resistance of the junction and $Z$ is the transmission line impedance. Unfortunately, the junctions are highly nonlinear elements, thus this simplified model does not account for losses that may vary with dc bias, the applied microwave power, or frequency. However, for small signals, the resistively shunted SNS junction model can be represented as a Josephson inductance, $\mathrm{L_J} = \Phi_0/(2\pi I_c)$ in parallel with $R_n$, where $\Phi_0$ is the quantum of flux and $I_c$ is the critical current of the junctions. Thus, at frequencies lower than the characteristic frequency, $f_c = I_c R_n/\Phi_0$, more current goes through the Josephson channel, limiting the dissipation. In the high frequency limit, the lossy transmission line model is likely to be a reasonable approximation.

In order to compensate for the loss of microwave power in a lossy transmission line, the characteristic impedance of the coplanar transmission line may be tapered to a lower value to maintain a constant microwave current throughout the array. The main challenge is that the tapering must accurately match both dissipation (through $R_n$ of the junctions) and the designed operating frequency of the array.

Another important tool to consider in the design of large $N$ arrays is the use of stacked junctions [7]. Typically, stacks with two or three junctions per stack show little or no degradation of operating margins. Thus many more junctions may be packed into a fixed-length transmission line, and thus a single chip, with only a small increase in fabrication complexity.

## II. Measurements and Discussion

### A. Programmable JVS Circuits

In order to generate large voltages from Josephson arrays, multiple arrays are connected in series for low frequency signals through a quarter-wave tap between the arrays. The microwave drive is then capacitively coupled to each array (or a

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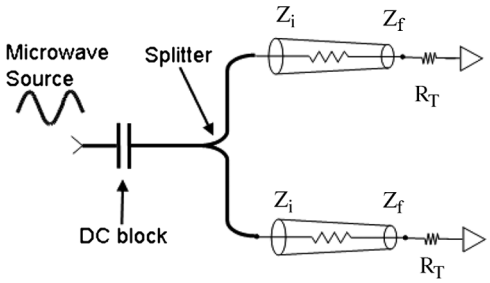


Fig. 1. Schematic of a single PJVS cell. The microwaves are split into two Josephson array segments, which are represented by lossy, tapered transmission lines. The impedance is tapered from the initial impedance $Z_i$ to the final impedance $Z_f$ and is terminated with a resistor $R_T = Z_f$.

pair of arrays). External to the Josephson part of the circuit, the microwave bias must be split to drive the separate arrays; this may be done either on-chip or external to the chip and launched onto the chip at multiple sites.

PJVS circuits have been designed for high voltage applications by several groups [2], [8] for 10 V operations using 64- or 32-way microwave splits, each driving a single array. This massive parallel division demands large amounts of microwave power for SNS circuits, most of which must be dissipated on chip. The demands of both chip cooling and available microwave amplifier power make this a practically challenging approach. For these reasons, we plan to design a 10 V PJVS system using only 16 arrays, which will be more efficient with regard to these challenges, and, hopefully, more practical for cryocooler applications.

Because off-chip splitters and microwave launches are difficult to design and fabricate, we have decided that, for the 10 V PJVS system, the microwaves will have a single launch onto the chip and an 8- or 16-way on-chip split using quarter-wave splitters and coupling capacitors. These techniques are well established [8] and initial tests have shown that, given sufficient on-chip area, the microwave splits should be reliable. A schematic of an array pair is shown in Fig. 1. The microwaves enter at the left and are split in a binary fan that is capacitively coupled to two arrays. Because the splitter is an intrinsic impedance transformer already, there is no reason why the initial array transmission line impedance $Z_i$ must be remain 50 Ω. In practice, the physical on-chip coplanar waveguide dimensions are too large to increase the impedance above $Z_i = 80$ to 90 Ω. The transmission line containing the Josephson junctions may then be tapered from the initial value, $Z_i$, to the final impedance, $Z_f = R_T$, which is the same as the termination resistance to prevent reflections from the end of the line.

This leaves the major design constraint as the number of arrays needed to generate 10 Volts, and thus the number of junctions in each array. We must therefore determine how many junctions can be placed in a single array while maintaining a large dc current range for the constant-voltage step. First, we consider untapered arrays in which $Z_i = Z_f = 50\ \Omega$ which are easiest to design and fabricate.

By use of three-junction $MoSi_2$-barrier stacked arrays [9], existing 1 V high resolution PJVS designs were modified to pack more junctions into the eight existing arrays. Instead of 4400 junctions per array of the existing design, 5500 stacks were squeezed into the same space to get a sufficiently high junction number to generate 5 V. The results are shown in Table I for 20 GHz operation at a temperature of 4 K. This approach produced a maximum voltage of 625 mV/array, as compared to 125 mV/array for previous circuits.

TABLE I
OPERATION OF HiRes5 CIRCUIT WITH THREE JUNCTIONS PER STACK BIASED WITH 20 GHz MICROWAVE DRIVE AT 4 K. THE CURRENT RANGE OF THE ZERO AND FIRST CONSTANT-VOLTAGE STEPS ARE REPORTED FOR EACH ARRAY TO INDICATE PROPER OPERATION

| Array | N | "0" Step [mA] | "1" Step [mA] |
|---|---|---|---|
| 1 | 16500 | 6.2 | 1.28 |
| 2 | 16500 | 3.9 | 1.22 |
| 3 | 16500 | 5.93 | 1.03 |
| 4 | 16500 | 5.15 | 1.15 |
| 5 | 16500 | 4.21 | 1.22 |
| 6 | 16500 | 4.44 | 0.94 |
| 7 | 16500 | 2.58 | 1.18 |
| 8 | 8442 | 3.83 | 1.66 |

TABLE II
MAXIMAL OPERATING POINTS OF ARRAYS IN 5 V TEST CIRCUITS IN WHICH N IS THE NUMBER OF JUNCTIONS IN THE ARRAY, $F$ IS THE OPERATING FREQUENCY, THE MARGIN IS THE CURRENT RANGE OVER WHICH THE VOLTAGE STEP IS CONSTANT, AND $I_C$ IS THE JUNCTION CRITICAL CURRENT

| Design | N | $f$ [GHz] | $f/f_c$ | Margin [mA] | Barrier | Ic[mA] |
|---|---|---|---|---|---|---|
| HiRes5 | 16500 | 23.24 | 1.0 | 2.24 | $MoSi_2$ | 10.2 |
| PV7 | 15600 | 18.7 | 0.81 | 1.97 | $MoSi_2$ | 11.8 |
| PV7 | 15594 | 18.9 | 0.82 | 1.76 | $MoSi_2$ | 11.8 |
| PV9C | 10152 | 14.6 | 0.50 | 2.22 | NbSi | 7.9 |
| PV9C | 10152 | 14.7 | 0.53 | 2.24 | NbSi | 7.7 |

Further experiments used arrays with different junction barrier technology. Test circuits were designed and fabricated using both $MoSi_2$ and amorphous NbSi ($a-Nb_xSi_{1-x}$) barrier materials [10]. The advantage of the $a-Nb_xSi_{1-x}$ is that the barrier resistivity may be tuned using the concentration, $x$, which is independent from the characteristic frequency (which is typically set using the barrier thickness for a fixed resistivity barrier material), and the critical current (which is set by the junction size). For a drop-in replacement for $MoSi_2$-barrier devices however, it has a higher resistivity for a fixed junction size and characteristic frequency. However, the latitude of device applications and the ease of fabrication have led us to supplant $MoSi_2$ as a barrier material in favor of $a-Nb_xSi_{1-x}$.

Table II summarizes results for single arrays using a variety of chip designs. In order to show the limitations of the microwave dissipation, we list the largest measured current range of each constant-voltage step that was found for each design. Various fabrication defects and other noninherent nonuniformities decrease the current range, so the maximum value shown in Table II is most representative for evaluating the microwave designs.

From Table II it is clear that the $a-Nb_xSi_{1-x}$-barrier devices have a larger normal-state resistance ($R_n = 7\ m\Omega$), and thus more microwave attenuation. Thus, the maximum

number of junctions for these arrays is closer to 10,000 than the 15,000 limit of $MoSi_2$-barrier devices. The reason for this is that the photolithographic reticles used for this fabrication were originally designed for $MoSi_2$-barrier junctions, and larger area junctions are needed to produce similar dissipation using the $a$-NbSi-barrier devices. The maximum array voltage for the $MoSi_2$-barrier circuits is over 600 mV, while that of the $a$-NbSi-barrier circuits is only about 300 mV. All of these arrays have large steps in the frequency range $15\ \mathrm{GHz} < \mathrm{f} < 24\ \mathrm{GHz}$, but the largest steps are listed in the table. Because of microwave resonances and reflections in the PJVS circuits caused by unoptimized microwave circuits, it is difficult to achieve a large frequency range over which all the arrays work properly. Research is ongoing to remove these microwave deficiencies.

Of the arrays shown in Table II, all are from chips for which the total voltage was near, or above, 5 V with ~1 mA of dc current margin. The HiRes5 circuit uses a design similar to that of the 1 V PJVS system [1] with a four-way splitter off-chip and a two-way on-chip splitter for eight microwave segments. The PV9C design uses an eight-way off-chip splitter, and a two-way on-chip splitter for a total of 16 arrays, while the PV7 design uses only eight arrays with no on-chip splitters. Both the PV9C and PV7 designs use a flex-bonded launch with an eight-way on-flex splitter. Because these later designs could be tested only on a flex-mounted package, a limited number of chips were tested. The HiRes5 designs could be tested in a spring-finger probe, which increased the testing throughput.

### *B. Tapered Transmission Lines*

Tests were also performed on chips with both tapered and untapered transmission lines. The tapered transmission lines gave consistently larger steps over a broad range in frequency. However, including tapers increases the complexity of the design because the degree of tapering depends on many factors, such as the junction normal-state resistance, the number of junctions per stack, and the designed operating frequency. Preliminary results indicate that our designs do not yet correctly taper to match the design frequency and junction normal-state resistance. However, they do show that tapering is a useful and powerful tool for microwave power management.

The limits of tapering transmission lines are set by the minimum and maximum impedances achievable on-chip. The maximum impedance is set by the width of the coplanar waveguide; in our designs a 30 $\mu$m gap gives around 85 $\Omega$. A larger gap between the center conductor and outer ground could give higher impedance, but would increase the area needed for an array segment. The minimum transmission line impedance is limited by the capacitance achievable between the center and ground conductors. By overlapping the base electrode and wiring layers, capacitance can be dramatically increased, leading to lower transmission line impedances of only $\sim 8\ \Omega$. Clearly, tapering over this range could have drastic consequences if the impedance profile were poorly matched to the attenuation profile.

A further advantage of tapering the transmission line comes from the reduced power dissipated in the termination resistor. For example, decreasing the transmission line from 50 $\Omega$ to 30 $\Omega$ decreases the power dissipation in these terminations by 40%.

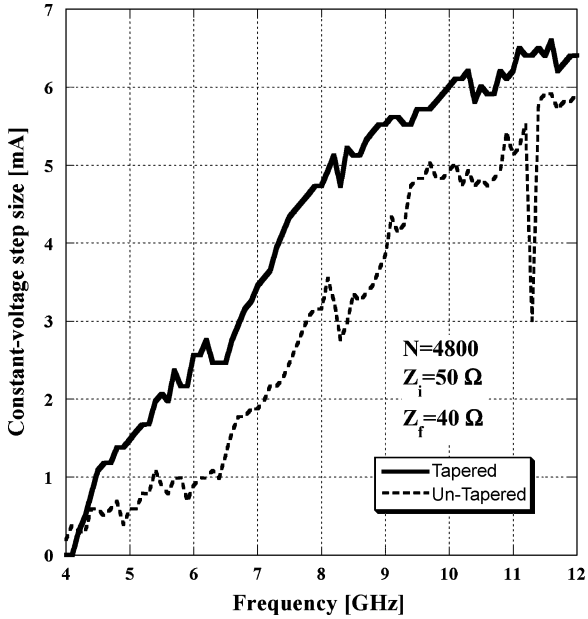


Fig. 2. Comparison of the first constant-voltage step for tapered and untapered transmission lines. The critical current for these junctions is 14 mA and the normal-state resistance is 4.1 $\mathrm{m}\Omega$.

In order to eliminate reflection from the end of the transmission line, the termination resistor is chosen to match $\mathrm{Z_f}$.

### *C. ac JVS Circuits*

The ac Josephson Voltage Standard system also needs the highest possible voltage per array. Unlike the PVJS, the acJVS applies the microwave signal to at most two arrays. The maximum voltage per drive is the limiting factor for the ac voltage. Until recently, the voltage per array was limited to $\sim 50\ \mathrm{mV_{rms}}$ per array (2048 junctions at 15 GHz drive) [11]. Fig. 2 is a plot of the magnitude of the first constant-voltage step over a range in frequency for tapered and un-tapered transmission lines with all other fabrication and junction parameters held constant. The tapered transmission line clearly has a nearly 1 mA larger step size over much of this range. Although the tapering improved the size of the step, there is still some room for further improvement. Similar to the longer arrays used for the PJVS system, optimization of the tapering to correctly match the microwave loss in the lossy transmission line remains to be done.

Nevertheless, with optimized filters and tapered transmission lines, the acJVS now will generate $110\ \mathrm{mV_{rms}}$ ($155\ \mathrm{V_{peak}}$) per array with over 1 mA of dc bias margin [12]. When a tapered transmission line is fully optimized it should be possible to get over $220\ \mathrm{mV_{rms}}$ per array, assuming nonlinearities of the junctions allow such an array to have a broadband response.

## III. Conclusion

SNS junction arrays with over 10,000 junctions have been fabricated and shown to have uniform constant-voltage steps with large operating current range. In order to optimize these arrays for operation in a 10 V PJVS system, the junction dissipation must be reduced (either by increasing the junction size or decreasing the barrier resistivity), and the transmission lines

must be carefully tapered to compensate the impedance for the microwave loss.

Tapering the impedance has already led to significant improvement on the output of the acJVS system. If junction dissipation is decreased and transmission line tapering is optimized, higher voltages should be achievable.

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## REFERENCES

[1] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable 1-volt programmable voltage standard," *Appl. Phys. Lett.*, vol. 71, pp. 1866–1868, Sept. 1997.

[2] J. Kohlmann, H. Schulze, R. Behr, F. Müller, and J. Niemeyer, "10 V SINIS Josephson junction series arrays for programmable voltage standards," *IEEE Trans. Instrum. Meas.*, vol. 50, pp. 192–194, Apr. 2001.

[3] Y. Chong, P. D. Dresselhaus, and S. P. Benz, "Thermal transport in stacked superconductor-normal metal-superconductor Josephson junctions," *Appl. Phys. Lett.*, vol. 83, pp. 1794–1796, September 2003.

[4] N. Hadacek, P. D. Dresselhaus, and S. P. Benz, "Lumped 50 Ohm arrays of SNS Josephson junctions," *IEEE Trans. Appl. Superconduct.*, vol. 16, pp. 2005–2010, Dec. 2006.

[5] H. Yamamori, M. Ishizaki, M. Itoh, and A. Shoji, "$\mathrm{NbN/TiN_x/NbN/TiN_x/NbN}$ double-barrier junction arrays for programmable voltage standards," *Appl. Phys. Lett.*, vol. 80, pp. 1415–1417, Feb. 2002.

[6] S. P. Benz, C. J. Burroughs, and P. D. Dresselhaus, "Low harmonic distortion in a Josephson arbitrary waveform synthesizer," *Appl. Phys. Lett.*, vol. 77, pp. 1014–1016, Aug. 2000.

[7] P. D. Dresselhaus, Y. Chong, J. H. Plantenberg, and S. P. Benz, "Stacked SNS Josephson junction arrays for quantum voltage standards," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 930–933, June 2003.

[8] H. Yamamori, M. Ishizaki, A. Shoji, P. D. Dresselhaus, and S. P. Benz, "10 V programmable Josephson voltage standard circuits using $\mathrm{NbN/TiN_x/NbN/TiN_x/NbN}$ double-junction stacks," *Appl. Phys. Lett.*, vol. 88, p. 042503, 2006.

[9] Y. Chong, C. J. Burroughs, P. D. Dresselhaus, N. Hadacek, H. Yamamori, and S. P. Benz, "Practical high-resolution programmable Josephson voltage standards using double- and triple-stacked $\mathrm{MoSi_2}$-barrier junctions," *IEEE Trans. Appl. Superconduct.*, vol. 15, pp. 461–464, June 2005.

[10] B. Baek, P. D. Dresselhaus, and S. P. Benz, "Co-sputtered amorphous $\mathrm{Nb_xSi_{1-x}}$ barriers for Josephson-junction circuits," *IEEE Trans. Appl. Superconduct.*, vol. 16, pp. 1966–1970, Dec. 2006.

[11] P. D. Dresselhaus, Y. Chong, and S. P. Benz, "Stacked $\mathrm{Nb-MoSi_2-Nb}$ Josephson junctions for AC voltage standards," *IEEE Trans. Appl. Superconduct.*, vol. 15, pp. 449–452, June 2005.

[12] S. P. Benz, P. D. Dresselhaus, C. J. Burroughs, and N. F. Bergren, "Precision measurements using a 300 mV Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, to appear in this issue..