Thermal stability of Nb/a-Nb_xSi_{1-x}/Nb Josephson junctions

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As a high-resistivity normal-metal barrier for superconducting Josephson junctions, metal-silicon alloys appear to be a good replacement for noble metals and have been applied to the development of quantum voltage standard circuits. We observed that the electrical properties of Nb-based junctions made with amorphous Nb_xSi_{1-x} barriers were slowly evolving over time when stored at room temperature. After systematically investigating both junctions and thin films, we have concluded that the changes in junction electrical parameters are due to changes in the amorphous Nb_xSi_{1-x} and not due to barrier-electrode interface effects. The resistivity of amorphous Nb_xSi_{1-x} increases after heat treatment at temperatures as low as 80 °C when the Nb concentration is less than 33%, that of NbSi₂. Furthermore, we found that annealed barriers behave similarly to barriers with the Nb concentration intentionally reduced to obtain smaller critical current and larger normal resistance with the same barrier thickness, as explained by our I_c - R_n relation developed based on the dirty-limit superconductor–normal-metal–superconductor Josephson junction theory. To explain these effects, we adopt and corroborate a microscopic picture based on alloy phase stability that was previously demonstrated by others. We also successfully demonstrate a method to stabilize junctions made with Nb_xSi_{1-x} barriers by intentionally annealing wafers during fabrication.

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INTRODUCTION

Amorphous metal disilicides, such as TiSi₂, WSi₂, and MoSi₂, have proven useful as barriers for Josephson junctions made with Nb superconducting electrodes. They have been implemented in practical application as junctions with nonhysteretic electrical properties for quantum voltage standard circuits, particularly with MoSi2 normal-metal barriers.¹⁻⁵ When these barriers are sputter deposited from stoichiometric alloy targets, the electrical properties of the junctions are highly reproducible and tunable through the accurate control of the barrier thickness. These features, when combined with a vertical dry-etching process, have enabled uniform arrays of tall stacks of junctions.⁶ More recently, in order to explore a wider range of electrical properties, we have investigated amorphous Nb_rSi_{1-r} films that are cosputtered from single-element targets.⁷ In addition to having similar electrical properties to other metal silicide barriers, cosputtering has allowed us to tune the alloy concentration, and thus the barrier resistivity, over a wide range, including around the metal-insulator transition.⁸

Thin alloy films in an amorphous state may be simultaneously homogeneous and nonstoichiometric. However, the amorphous state is by nature metastable and the structure will change in time. The rate of this transition depends on the temperature, the activation energy of the crystallization, the compound formation, or the phase segregation, and the relative composition of the alloy with respect to a stoichiometric phase. In this paper, we investigate the electrical properties of Nb/*a*-Nb_xSi_{1-x}/Nb Josephson junction arrays subjected to controlled heat treatments at temperatures ranging from room temperature to 200 °C.

FABRICATION

A detailed description of the fabrication of Nb/Nb_xSi_{1-x}/Nb Josephson junction array (JJA) circuits has

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been given elsewhere.^{2,3} Here we mention only the details relevant to the junction barrier. The trilayers for the junctions are sputter deposited in a multitarget sputtering chamber. During deposition, the back side of the Si substrate is cooled with flowing nitrogen gas. The temperature of the wafer during deposition has been measured to be below 130 °C. For the junctions and JJA circuits described in this paper, the Nb_xSi_{1-x} barriers were cosputtered from independent Nb and Si targets. The relative sputter rates were adjusted for a Nb concentration near 15 at. %. During the remainder of the fabrication process, the wafer was kept below 130 °C. Multiple JJA circuits with various junction sizes were fabricated on each chip. Each JJA contains 400 junctions with a fixed size. The individual junctions are squares with sizes ranging from $1.5 \times 1.5 \ \mu m^2$ to $6.5 \times 6.5 \ \mu m^2$. For these junction sizes, a typical barrier composition yielded junctions with critical currents in the range from 0.3 to 10 mA.

ANNEALING

We measured the change of the critical current I_c and normal resistance R_n of series JJAs as a result of annealing. The heat treatment (HT) was done on a hotplate in air. Figure 1(a) shows typical changes in the electrical parameters of a JJA caused by annealing. The first two points show the values for I_c and R_n immediately after processing and after having aged nine months at room temperature (~ 20 °C). The remaining three points show how the electrical parameters continue to change with successive HTs. For all three indicated HT points, the temperature was 100 °C, while the time was 1 h for the first point and 4 h for the subsequent data points. The critical current I_c decreases while the normal resistance R_n increases as a result of both aging and HT. Figure 1(b) shows the measurement results of five different JJAs heat treated at different temperatures, each for 4 h. The junction parameters change by larger amounts with higher HT temperatures. In all cases, the HT duration includes the time for ramping the hotplate at 300 °C/h.



FIG. 1. Change in the Josephson junction parameters with time and heat treatment (HT). (a) HT history of a single JJA. HTs 1, 2, and 3 were performed in succession and the conditions were $100 \degree C$ for 1 h (HT1), $100 \degree C$ for 4 h (HT2 and HT3). (b) Fractional changes in electrical parameters for five different JJAs subjected to a 4 h HT at the indicated temperature. All measurements of the Josephson junction parameters were done at 4 K unless otherwise specified.

From the JJA measurements alone, it is unclear whether the observed changes in the junction parameters are due to changes in the barrier material itself or due to changes in the barrier-electrode interface. It is known that the electrical properties of junctions are particularly sensitive to properties of the interface between the normal and superconducting materials.^{9,10} For example, migration of Si into the electrode or Nb into the barrier may occur at the interface between these materials. Thus it is important to determine whether the differences in measured junction parameters are due to changes at the interface or changes within the barrier material itself.

In order to distinguish bulk from interface effects, we have annealed and made resistance measurements on Nb_xSi_{1-x} thin films alone without the Nb electrodes. These



FIG. 2. Fractional change in sheet resistance measured at 4 K due to annealing for bare $Nb_{0.15}Si_{0.85}$ thin films. The annealing conditions were identical to those for the JJA circuits shown in Fig. 1(b).

films were deposited and patterned on oxidized Si substrates by use of the same fabrication process as for the JJA circuits, except that the films were thicker ($\sim 100 \text{ nm versus} \sim 20 \text{ nm}$ for a barrier) to minimize surface effects. Figure 2 shows the fractional change in the sheet resistance R_s after HTs identical to those shown in Fig. 1(b) for the JJA circuits. The sheet resistance of the bare Nb_xSi_{1-x} material has a monotonic increase with increasing temperature, similar in magnitude and slope to the R_n of the JJA circuits. We believe that these results support the idea that the changing junction properties in the JJA circuits are due predominantly to bulk changes in the barrier material and are not associated with the interfaces with the junctions' Nb electrodes. We note, however, that the magnitude of the change in R_s of the isolated barrier material is smaller than that of the junction R_n , namely, 23% at 200 °C vs 28% for the junction barriers. This minor difference is probably due to variability of thermal contact with the hotplate or other conditions. Under a more controlled HT, where a JJA circuit and a thin film were simultaneously annealed in a convection oven, the percent change in resistance was identical. With this measurement, we feel confident that the measured changes in the junctions are due to bulk changes in the barrier and not to interface effects.

The comparison of junction measurements with bulk measurements may be further complicated by localization effects which would change the effective conductivity at the long length scales used in bulk measurements.¹¹ Because the materials used in this comparison are well into the metallic regime (15% Nb as compared to the metal-insulator transition at 11%Nb), these effects appear to be minimal.

FIT TO SUPERCONDUCTOR-NORMAL-METAL-SUPERCONDUCTOR THEORY

The proximity effect theory of superconductor-normalmetal-superconductor Josephson junctions describes the



FIG. 3. I_c vs R_n plot of as-processed, annealed, and Nbconcentration-reduced JJA circuits for barrier devices 27 nm thick. Each pair of open symbols represents I_c and R_n data measured before and after the corresponding annealing, respectively. Some data belonging to the 80 °C HT are obstructed behind other data. Each junction size was designed to be 3.5 μ m².

characteristic voltage $V_c = I_c R_n = V_{c0}(d/\xi_n) \exp(-d/\xi_n)$, where d is the barrier thickness and ξ_n is the normal coherence length.¹² Any change in the barrier resistivity will directly affect ξ_n because $\xi_n \propto (v_n l_n)^{1/2}$, where v_n is the Fermi velocity in the normal metal and l_n is the mean free path.¹¹ Electrical conductivity and tunneling measurements by Hertel et al.⁸ showed that the conductivity and the density of states of amorphous Nb_xSi_{1-x} linearly increase with $x - x_c$, where x_c is the Nb concentration for the metal-insulator transition of Nb_xSi_{1-x} for, at least, $x_c = 0.115 < x < 0.2$. This supports the conjecture that we can regard Nb atoms as electron dopants because x=0.15 in our Nb_xSi_{1-x} barriers, and there is no appreciable change in disorder, or mean free path l_n . From the Drude model, the conductivity of metal is given by σ_n $=e^2n\tau/m$, where n is the carrier density, τ is the mean relaxation time, and *m* is the mass of an electron. With $n \propto v_n^3$ and $\tau = l_n/v_n$, we get $\sigma_n \propto n^{2/3}$ and also $\xi_n \propto n^{1/6}$. Consequently, $\xi_n \propto \sigma_n^{1/4} \propto R_n^{-1/4}$. Now we find I_c as a function of R_n :

$$I_c \propto R_n^{-1}(d/\xi_n) \exp(-d/\xi_n) \sim R_n^{-3/4} \exp(-BR_n^{1/4})$$

Here, B is a constant that includes the barrier thickness d, the junction area A, temperature T, and material parameters.

The I_c vs R_n plot shown in Fig. 3 shows a good fit between the above I_c - R_n relation and the two cases of both different Nb concentration and the effects caused by HT. In deriving the above relation, we used only the resistivity change of the barrier material, which results entirely from changes in carrier concentration. Since the HT data fit this relation so well, we conclude that HT annealing follows the same behavior as changing Nb concentration and can be regarded as a method to control the carrier concentration of the Nb_xSi_{1-x} barrier.



FIG. 4. Temperature dependence of Josephson critical current density for different arrays: a JJA circuit before and after annealing, and a JJA with reduced Nb concentration. The junction size for the JJA with reduced Nb concentration is 5.5 μ m², and that for the annealed JJA is 4.5 μ m². The inset shows nearly identical 4 K *I-V* curves of heat-treated (solid) and Nb-concentration-reduced (dashed) JJA circuits, where both the junction sizes are 5.5 μ m².

In the metallic regime, the Drude model produces satisfactory agreement with the experimental data. It should be emphasized that this model is overly simplistic, particularly approaching the insulating regime where localization effects play a more important role in the conduction. Near the metalinsulator transition, the appropriate conductivity entering into the Josephson equations is likely to be greater than the measured film conductivity. A detailed study of this effect is beyond the scope of this paper.

COMPARISON OF ANNEALING AND Nb CONCENTRATION CONTROL

Having found that both annealing and Nb concentration reduction move the junction parameters along the same trajectory in the I_c - R_n plane, the shape of I-V curves and the temperature dependences of the critical current densities (Fig. 4) were compared for the two JJA circuits that had produced similar values of I_c and R_n . This comparison shows similarly shaped I-V curves and critical current density vs temperature characteristics, suggesting that both annealing and Nb concentration control the electronic properties of the Nb_rSi_{1-r} barrier by changing the carrier concentration. The temperature dependence of the critical current density is used to infer the normal-metal coherence length of the barrier since the exponential dependence on the coherence length dominates the change of the critical current density. The fact that the temperature dependence is so similar indicates that the normal-metal coherence length of these two devices is nearly identical. Moreover, we note that the possible interface modification from annealing is insignificant compared to the effects of carrier concentration. These data for I-V curves and temperature dependence data provide further evidence that HT changes the effective carrier concentration.

ANNEALING OF AMORPHOUS Nb_xSi_{1-x} THIN FILMS

Of the various Nb-Si alloys, Nb₅Si₃ and NbSi₂ are known to be stable crystalline phases. Although every amorphous thin film is unstable or metastable, amorphous nonstoichiometric alloys can exhibit phase segregation in addition to the structural relaxation found in stoichiometric amorphous materials. Crystallization of Nb-Si thin films was investigated by Nava et al.,¹³ who concluded that significant crystallization occurs near 270 °C, while an irreversible increase in resistivity was observed with heat treatments at temperatures lower than 270 °C. Further annealing at a higher temperature results in reduced resistivity, which becomes a minimum for the fully crystalline state. For the Nb_xSi_{1-x} material used in our application, the Nb concentration was about 15%. At this concentration, the most stable phases must be NbSi₂ and pure Si, as was previously shown by x-ray diffraction and transmission electron diffraction (TED) for the case of 26% of Nb concentration in Ref. 13 both measurements showed the crystalline NbSi₂ hexagonal phase appeared after HT at 900 °C for 30 min. However, the better detectability by TED revealed the earlier stage of crystallization at a much lower temperature following HT at 352 °C. In contrast with the crystalline NbSi₂, the Si crystallization peak was not observed up to 900 °C. These measurements suggest the following microscopic picture, in which NbSi2 nucleation results in Nb-deficient and silicon-rich neighboring material. The limiting conductivity will be that of the silicon, which is reduced by removing the Nb "dopant" atoms into the more stable NbSi₂ phase. A similar picture has been suggested elsewhere, although such agglomerates were observed by transmission electron microscope, but using higher temperature (500 °C) annealing.¹⁴

If the above model is correct, the resistivity increase should be minimized at the stoichiometric composition NbSi₂ because the phase segregation would be minimized. To verify this conjecture, we annealed Nb_xSi_{1-x} films with various concentrations x, and the resulting fractional change in resistivity is shown in Fig. 5. The annealing conditions were 150 °C for 4 h in N₂. We used a convection oven and a specific temperature profile for heating and cooling ramps. The Nb concentration was measured by Rutherford backscattering spectroscopy (RBS). At concentration less than 0.33 (the concentration of the stable disilicide phase), the resistivity increases rapidly for decreasing concentration. If the increased Nb segregation is mostly responsible for the resistivity increase, as suggested above, such a change must be greater for smaller x as the doped silicon approaches the metal-semiconductor transition, as is observed. This is supported by the trend that as-deposited resistivity tends to be more sensitive to the change of x with smaller x, as shown in the inset of Fig. 5. On the other hand, the origin of negative fractional change in resistivity (higher conductivity) can be understood by the creation of Nb-richer volumes, which effectively reduces overall resistivity, in contrast to the Nb-



FIG. 5. Fractional change in resistivity at room temperature after annealing of Nb_xSi_{1-x} thin films with different compositions. The annealing conditions were: 150 °C, 4 h in N₂. A convection oven was used. The duration includes ~30 min for heating, but does not count the extra 85 min for cooling. The fractional change is defined as $(R-R_{\rm HT})/R$. Inset shows the as-deposited Nb_xSi_{1-x} resistivity versus x.

deficient volumes. The vanishingly small changes in resistivity near the stoichiometric 0.33 concentration further support the hypothesis of phase segregation as the primary cause of instability in the electrical properties of the junctions.

In Fig. 6, we show in detail the time dependence of the change in resistivity for Nb_xSi_{1-x} films kept at room temperature. We believe that oxidation is not a significant effect because the same relative changes are observed independent of



FIG. 6. Fractional change in the sheet resistance of amorphous Nb_xSi_{1-x} thin films over time. The ambient temperature was approximately 20 °C. The Nb concentration was ~8%. A dotted line representing $t^{0.37}$ has been drawn as a guide. Inset shows a log-log plot for extracting α in $\delta R_s(t) = At^{\alpha}$, where A and α are fitting parameters.

the film thickness. Furthermore, other research has shown that oxygen contamination is limited only to the surface.^{13,15} In the model described previously, Nb atoms should diffuse until captured by NbSi₂-like agglomerates. We observe that the fractional change in sheet resistance has a time dependence $\sim t^{0.37}$, which is probably dominated by typical diffusion dynamics. However, the exponent of our measured time dependence is different from that for typical one-dimensional diffusion dynamics ($t^{0.5}$), and the difference likely arises from a more complicated microscopic nonhomogeneity, etc. Because nucleation is easy in this system, as suggested by the aging and annealing results, the aging effect for nonstoichiometric Nb_xSi_{1-x} can cause undesirable long-term changes in junction parameters.

STOICHIOMETRIC BARRIER: MoSi₂

For comparison, we also annealed junctions made with $MoSi_2$ barriers deposited with a stoichiometric target. In particular, we examined a Nb/MoSi₂/Nb Josephson junction circuit that was annealed at 150 °C for 4 h. We chose this system instead of junctions with a NbSi₂ barrier because NbSi₂ has a superconducting $T_c \sim 2.5$ K, which is close to our 4 K measurement temperature, while no superconducting transition has been observed in MoSi₂.¹⁶ We measured only a very small increase (<0.2%) in R_n for this JJA circuit, in spite of a 7% measured reduction in I_c . No phase segregation should occur because MoSi₂ is stoichiometric.

The cause of the I_c reduction is unclear, although it is much (about five times) smaller than the I_c reduction observed for nonstoichiometric Nb_xSi_{1-x} with the same annealing conditions. We suspect that this small change may be due to degradation of the MoSi₂/Nb interface by solid-state reaction among those atoms. For example, formation of a Nb-Si phase could reduce the superconducting order parameters at the boundaries, thus reducing the critical current.

RAMIFICATIONS FOR APPLICATIONS

The changes in resistivity of Nb_xSi_{1-x} and the corresponding changes in the Nb/Nb_xSi_{1-x}/Nb Josephson junction parameters that occur even at room temperature are undesirable for quantum voltage standard applications. As an example, if I_c and R_n were each changed by ~6% and ~1.4%, respectively, after aging only 9 months at room temperature, and assuming the time dependence of $t^{0.37}$ as in Fig. 6, then the changes would grow to roughly 12% and 3% in five years. These changes are even more dramatic if any unintended thermal treatment is included. On the other hand, if the superconducting integrated circuits remain at 4 K temperature, there will be negligible changes to the junction parameters. Since keeping devices at cryogenic temperatures typically occurs only for systems in continuous operation, another way to stabilize these nonstoichiometric barriers is desirable. One way is to add a fabrication step that intentionally anneals the barriers to yield predetermined electrical characteristics. If a nonstoichiometric barrier is required for an application, an intentional annealing step can accelerate agglomeration and reduce the potential impact of aging-related annealing.

Such a reduced aging effect is shown in Fig. 7. The junc-



FIG. 7. Fractional change in junction R_n approximately two months after annealing at the specified temperature. Each circuit was stored in ambient air at room temperature. The point for room temperature (20 °C) is the result for no annealing. The size of error bars comes from common measurement errors and ambiguity in determination of R_n or I_c from *I*-*V* curves. Inset shows how I_c changes for the same conditions.

tion parameters of three JJA circuit chips were measured after annealing for four hours at 80, 125, and 200 °C and again after being aged for about two months. The fractional changes for the JJAs that had been heat treated were significantly smaller than those for the circuit that was not annealed.

However, there is one drawback to a postprocess annealing performed either to tune the circuit parameters or to reduce aging effects. We observed that the maximum applied bias current before the junctions become normal from self-heating, I_{max} , degrades after annealing for both Nb/Nb_rSi_{1-r}/Nb and Nb/MoSi₂/Nb Josephson junctions.¹⁷ This maximum current is an important design parameter for the stable operation of voltage standard circuits. Experiments suggest that the contacts to the wiring layer become degraded by the annealing step. Annealing up to ~ 150 °C reduces I_{max} gradually, but annealing at 200 °C causes a precipitous drop in I_{max} . This problem can be overcome by annealing before the wiring deposition step instead of at the end of the fabrication process. We verified that this HT step produces no degradation of the maximum current even at the HT temperature of 200 °C. For future circuits using nonstoichiometric Nb_xSi_{1-x} barriers we can anneal our trilayers at 100-200 °C for about 4 h without compromising the maximum applicable bias current when better long-term barrier stability is required.

CONCLUSIONS

We measured and modeled the thermal stability of Nb/*a*-Nb_xSi_{1-x}/Nb Josephson junctions and a-Nb_xSi_{1-x} films. Increased resistivity with aging at room temperature and higher-temperature heat treatment annealing in both

junctions and films has been attributed to an agglomeration of stable NbSi₂ in a-Nb_xSi_{1-x}. We have demonstrated improvement in the long-term stability of junction parameters through stabilization of the junction barriers by including intentional heat treatment as part of the circuit fabrication process.

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