Practical Aspects Impacting *Time Synchronization Data Quality* in Semiconductor Manufacturing

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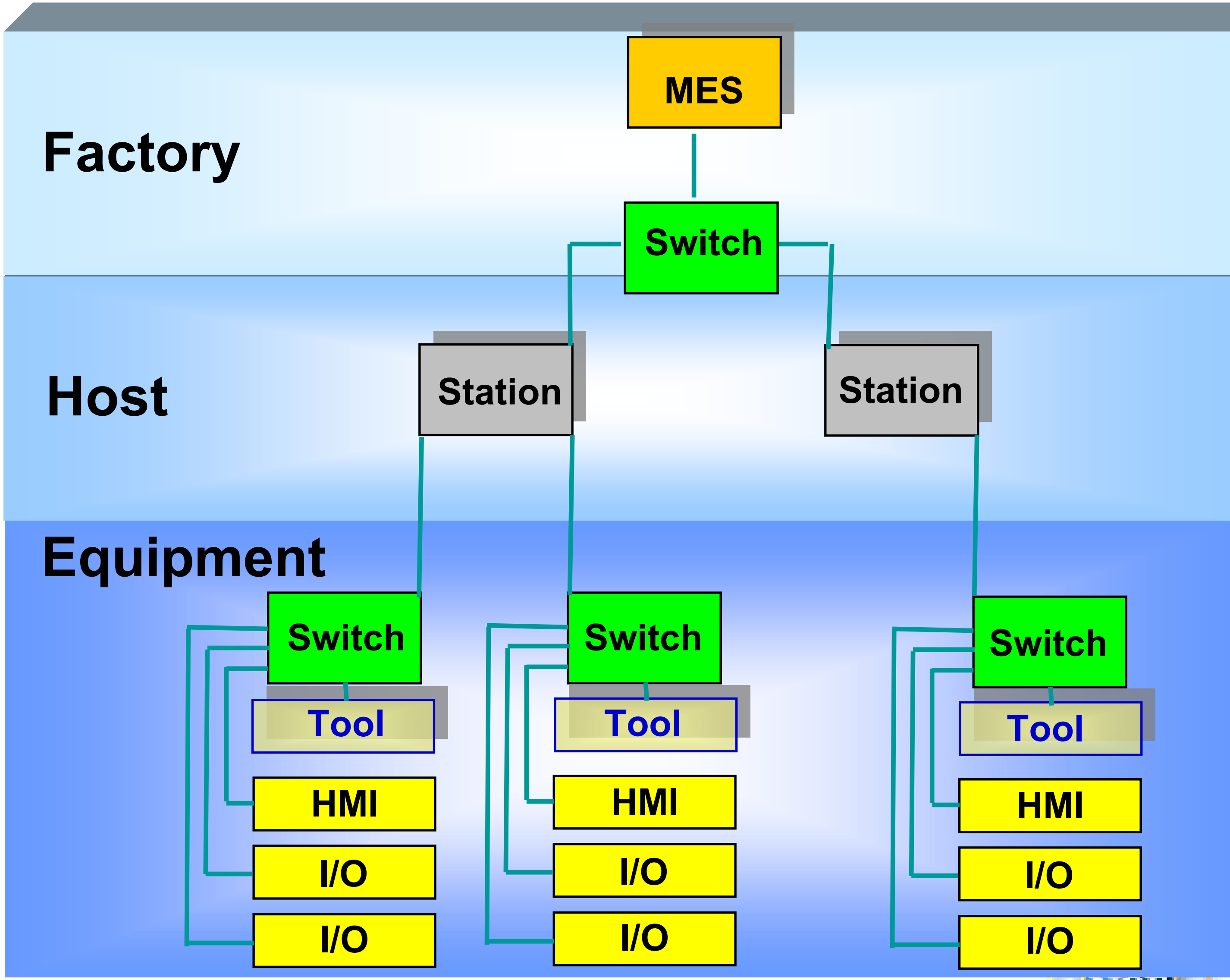
Outline

- Why is time synchronization so important in semiconductor manufacturing?
  - Components in the end-to-end synchronization problem
- Currents efforts in semiconductor manufacturing time synchronization data quality
  - NIST and the University of Michigan
  - SEMI Standards
- Key points and future efforts

Motivation: The Move to Networks

Ethernet Everywhere!

- Interfaces A, B and C
- EDA, PCS, e-diagnostics
- HSMS
- XML, VPN, OPC
- MES to I/O Level



Why Synchronize Time?

Manufacturing Automation
- Process Control
- Coordination among tools
- Scheduling/Dispatching

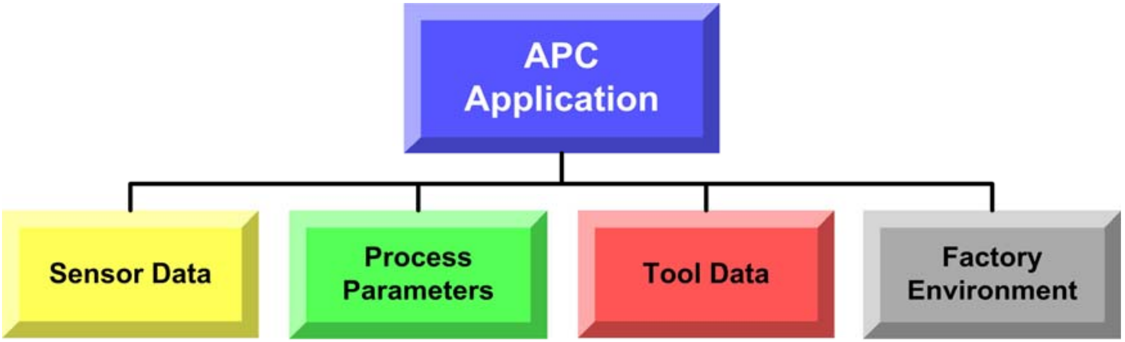
Robotics Coordination for Auto Industry

Test and Measurement
- Fault Diagnosis

Network Operations
- Security
- QoS measurement

Fault Diagnosis for Power Industry

Motivation in Chip Manufacturing



Precision Time Stamping to Merge Various Data Streams

Advanced Process Control:

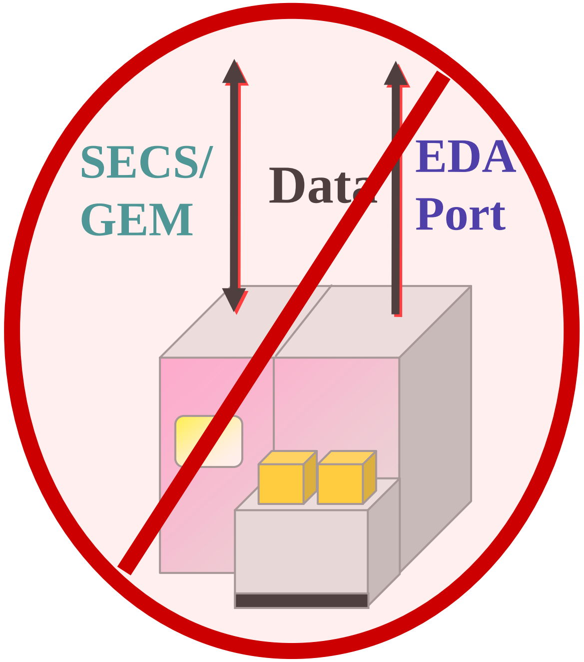
- Fault Detection Classification
- Process Optimization

Precision Time Stamping:

- Merging data from heterogeneous sources
- Maintain data and event ordering
- Improve multivariate, advanced correlation and analysis
- Expose new cause-effect relationships

Common Time Sync. Pain Points in APC

- Events and data are received out-of-order
- Inability to support high data collection rates with good data quality
- Cannot synchronize data across multiple systems (e.g., equipment & metrology systems)
- "False Positives" in fault detection systems bring equipment down unnecessarily
  - Out-of-order data, poor timestamping
  - Timestamping at point of sending instead of point of event occurrence
- "Out-of-control" situations for R2R controllers
  - Poor data quality due to delay and *delay variability*
- Inability to migrate from the equipment level to the factory-wide level with APC systems
- Etc…



How Does Time Synchronization Work?

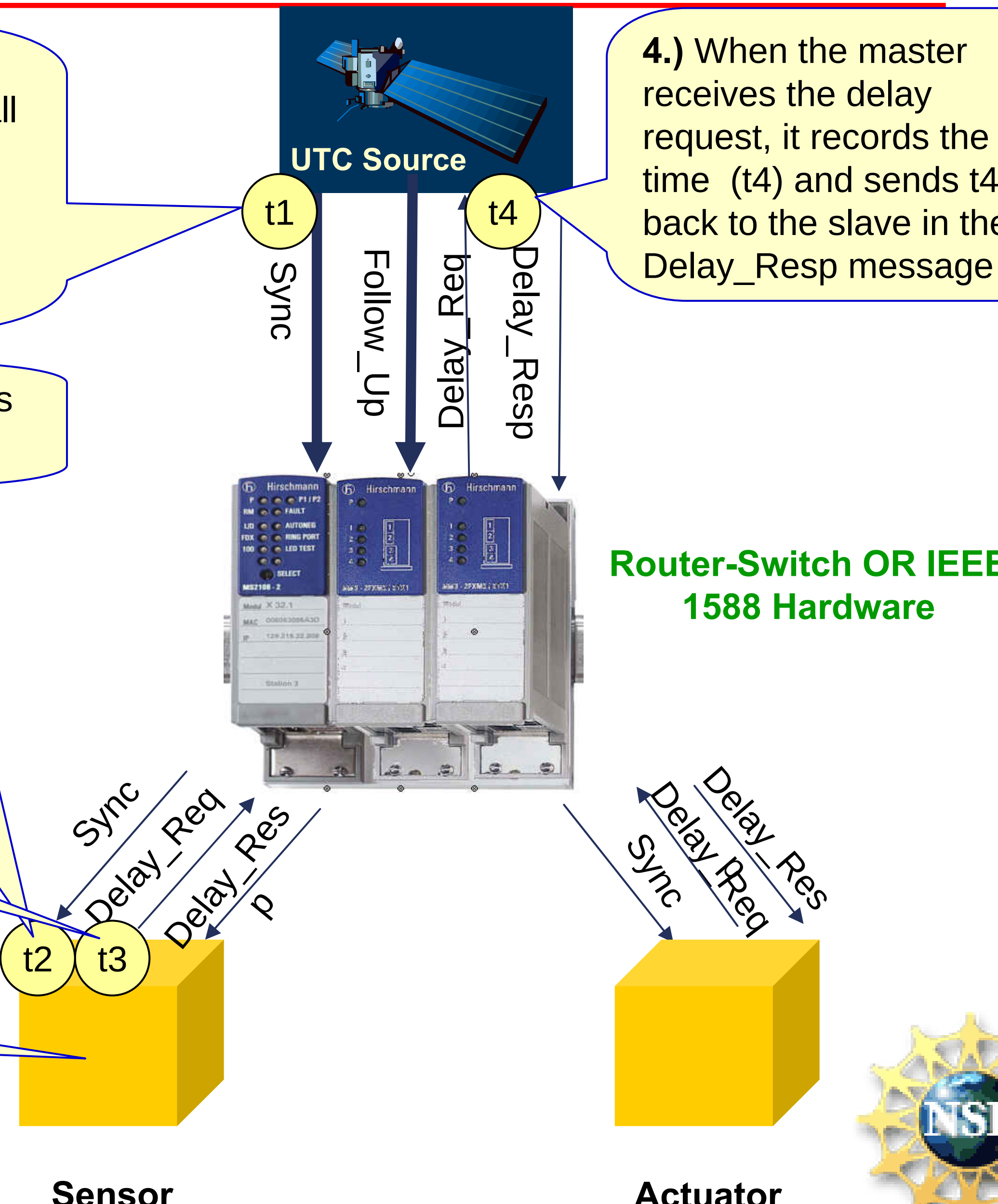
1.) Master (UTC-based_ clock) multicasts Sync messages to notify synchronization to all of its slaves
1.5) Master follows up with a time stamp of when the Sync message was actually sent using the Follow_Up message

2.) Slave receives the Sync message, records time of receipt

3.) Slave returns with a Delay_Req message used to gauge the latency from the slave to the master and records the time that message was sent

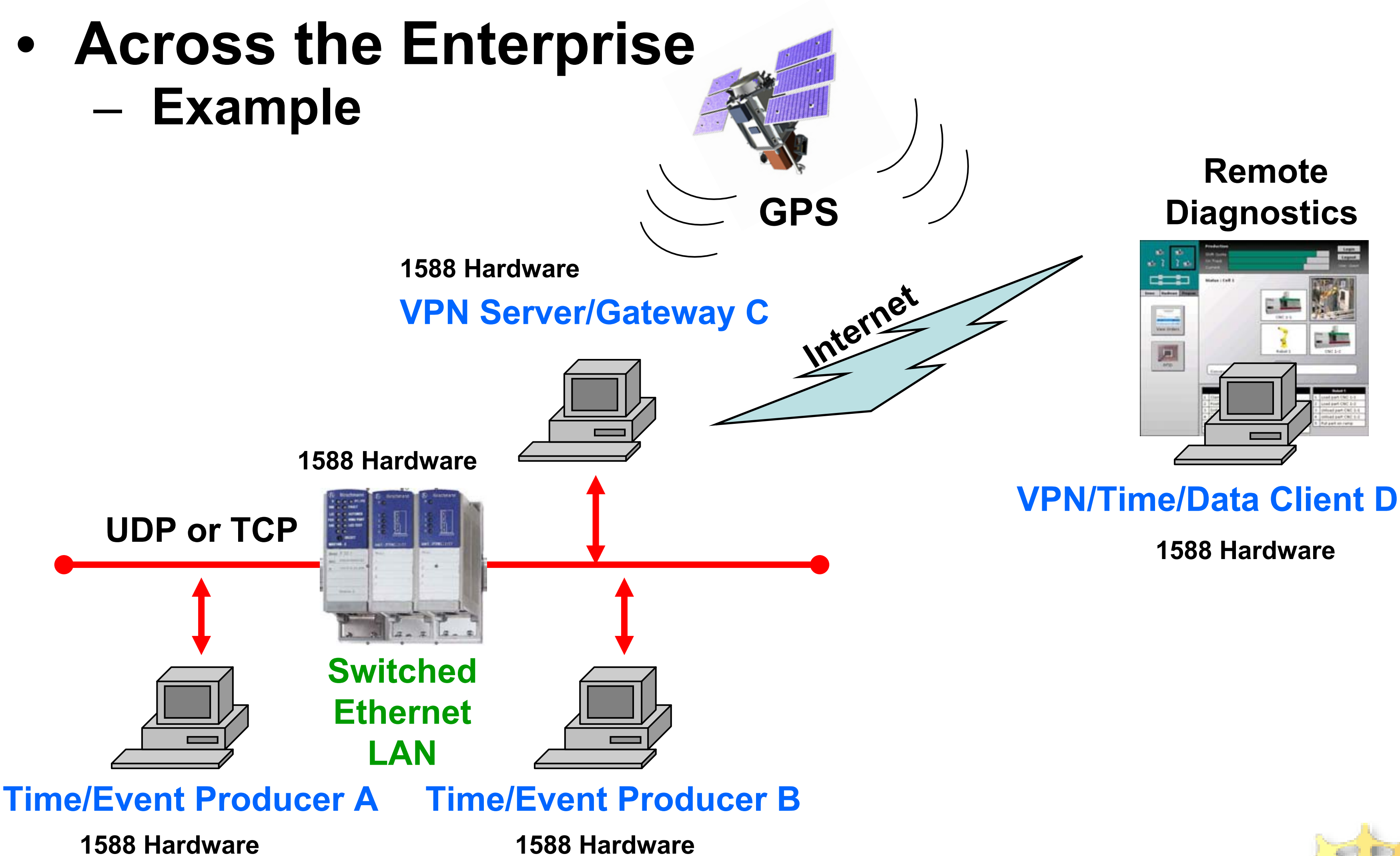
4.) When the master receives the delay request, it records the time (t4) and sends t4 back to the slave in the Delay_Resp message

5.) Slave calculates offset based on t1,t2,t3, and t4



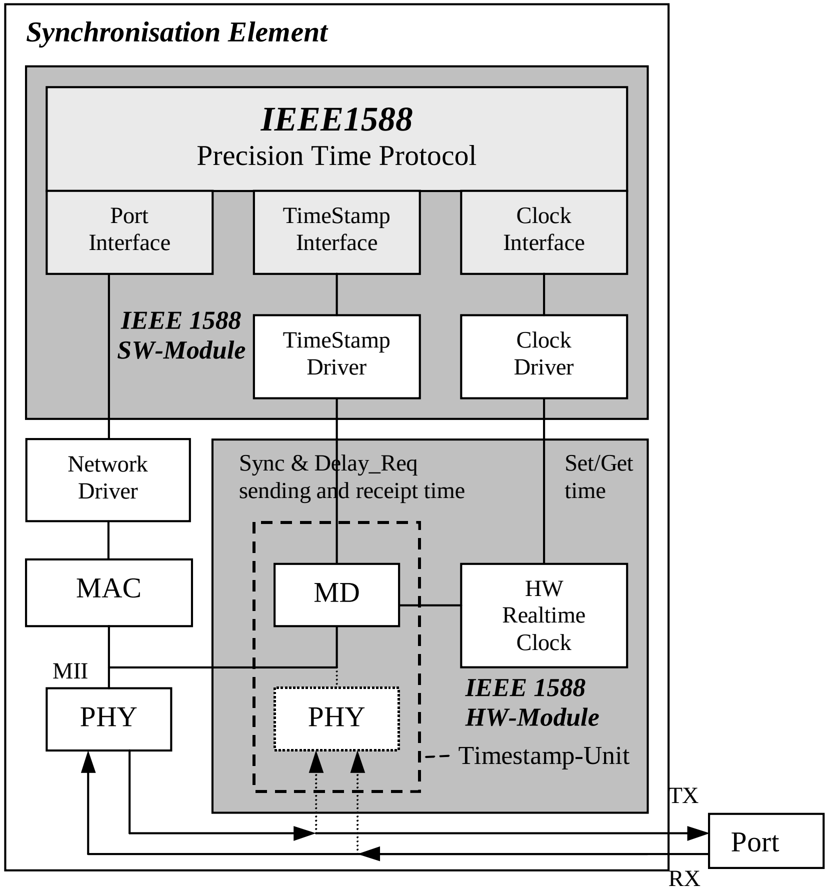
How Does Time Synchronization Work (2)

- Across the Enterprise
  - Example



Solutions for Time Synchronization

- NTP 4.0 or SNTP 4.0
  - Software only
  - 50 us to 50 ms accuracy, depending largely on software + network environment
  - More mature
- ANSI/IEEE 1588 – (IEC 61588)
  - Software and hardware
  - Approx 100ns accuracy
  - Infancy in standard and solutions



necessary if no MII- interface available

MD – Message Detector for *Sync* and *Delay_Request* packets

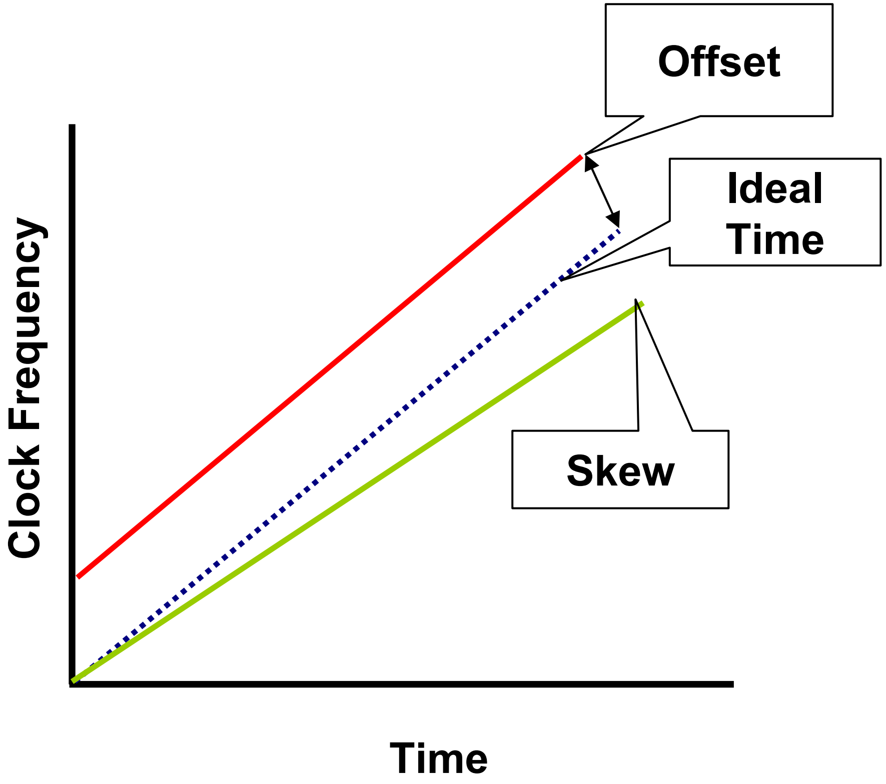
What Needs To Be Synchronized?

Clocks have

–Offset from absolute time

–Skew, rate difference from frequency source

- Due to clock imperfections, temperature, etc.
- Typical computer system clocks can reach several hundreds parts per million (PPM)
- Several seconds off per day

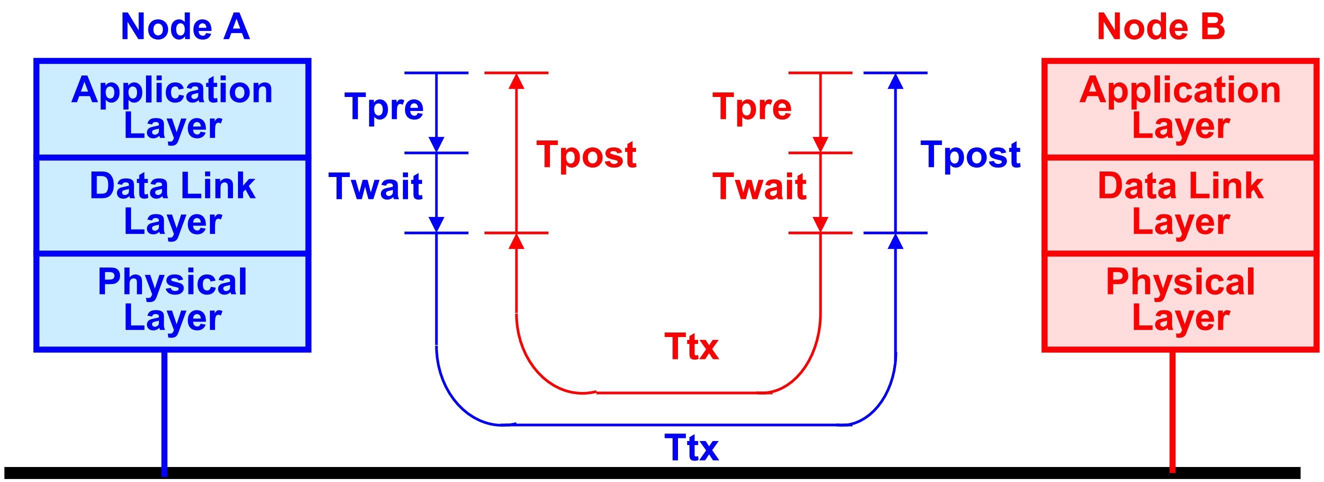


Today's Factories

- **Switched Fast Ethernet (100Mbps)**
  - No collisions, Low utilization
- **Protocols on top of Ethernet for end-to-end communication diagnostics, security, etc.**
  - UDP and TCP for end-to-end connectivity
  - Equipment Data Acquisition (E134, interface "A") and OPC for diagnostics (SCADA)
  - VPN for security (E132, interface "C")
- **A lot of data traveling to a lot of places**

- **So where is the weak link??**

Components of Delay



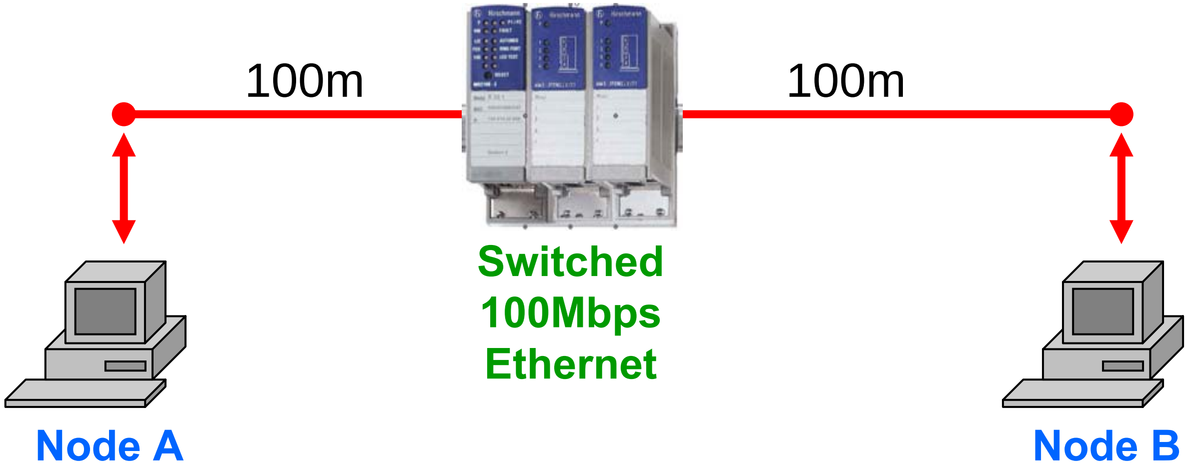
- **Total end-to-end delay is the sum of**
  - Pre-processing time: microprocessor
  - Waiting time: network protocol - MAC
  - Transmission time: data rate & length
  - Post-processing time: microprocessor

Device Delays

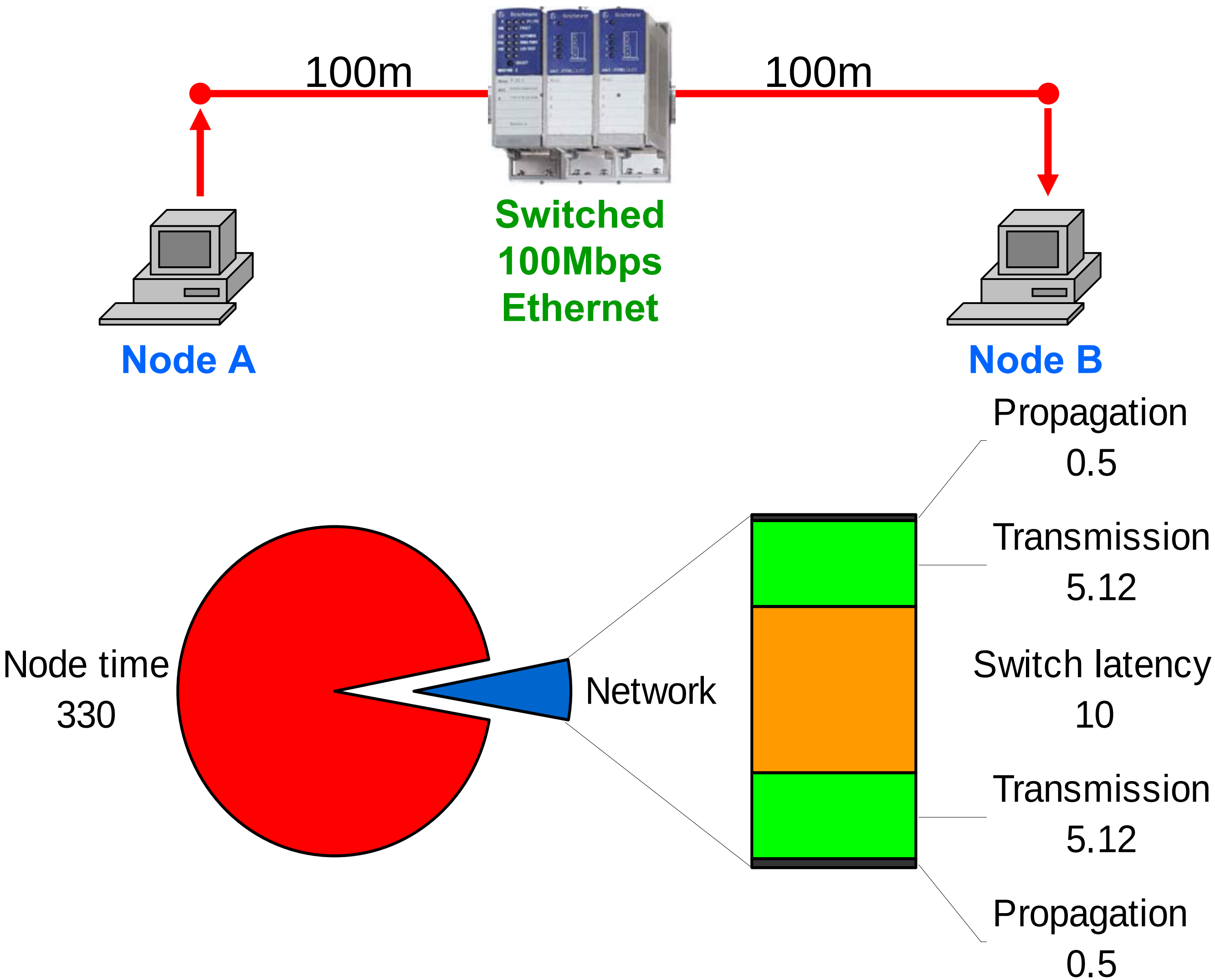
Network Delays

A Simple Switched-Ethernet Experiment

– Where are the sources of delay and variability?
  - Network and nodes



One-way Delay Contributions



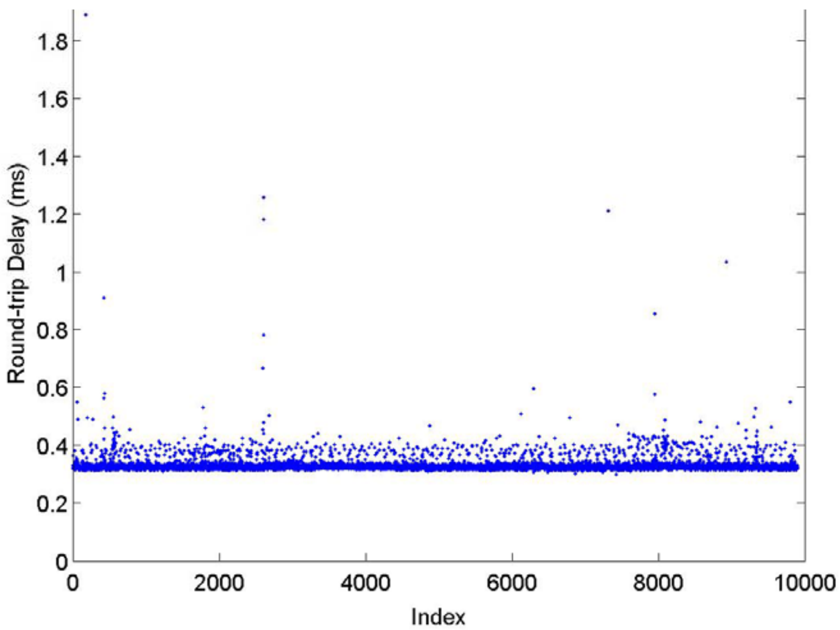
64-byte packet

The Delay is in the *Node Software*

(Tpre, Twait and Tpost)

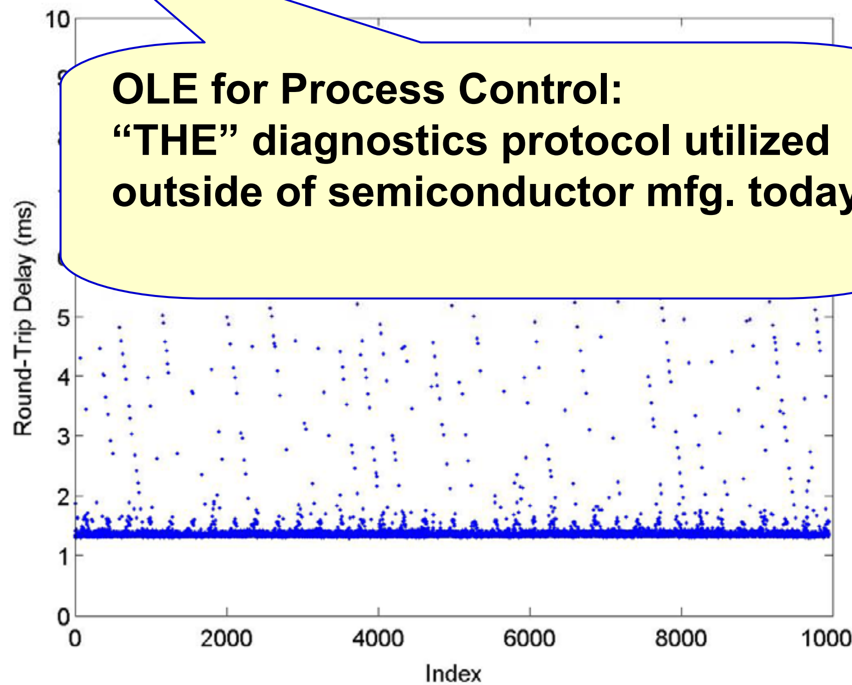
Application level delays

- UDP round-trip delays (100Mbs switched network)



- **Mean = 0.33ms**, max = 1.89ms
- Stdev = 0.03ms
- **Network round-trip time: 0.035ms**

- OPC round-trip delays (100Mbs switched network)



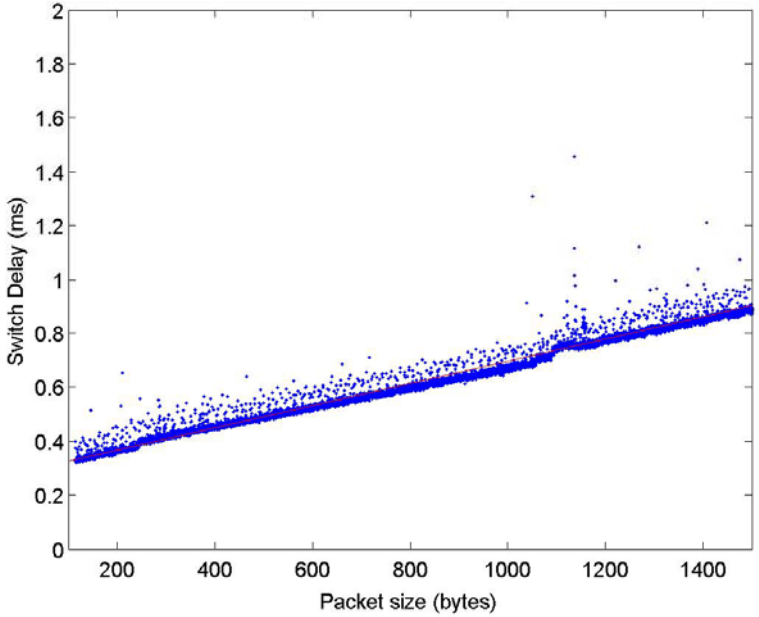
OLE for Process Control: "THE" diagnostics protocol utilized outside of semiconductor mfg. today

- **Mean = 1.5ms**, max = 16.8ms
- Stdev = 0.81ms

The Delay and delay Variability is in the *Node Software*

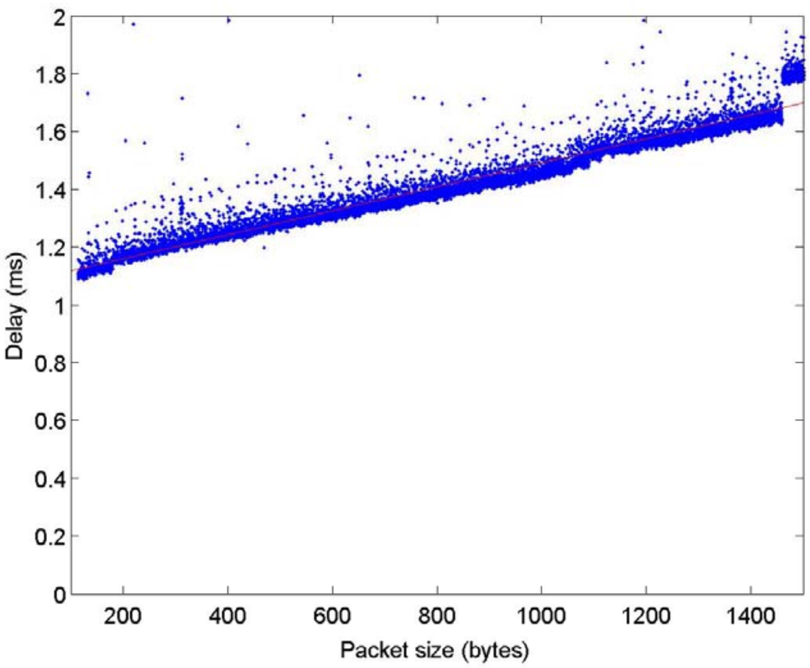
Varying packet size

- **UDP round-trip delays (100Mbs switched network)**



- **Slope = 0.411μs/bit**
  - **Theory: 0.32 μs/bit**
- **Intercept: 0.285ms**

- **VPN round-trip delays (100Mbs switched network)**



- **Slope = 0.848μs/bit**
- **Intercept: 1.07ms**
- **Using DES (data encrypt. std)**

Test Results Summary

	UDP	VPN (UDP)	OPC (TCP)	DeviceNet
Delay Average (ms)	0.33	1.21	1.48	0.3-1.2
Delay Variation (3σ) (ms)	0.09	0.49	2.43	0.005-0.2
Min. Ntwrk. Contrbutn (ms)	0.035	0.035	0.035	0.188
% of Delay Due to Network	11%	3%	2%	63%

The Message:

- **We need time synchronization and time stamping to mitigate delay and delay variability disturbances of end-to-end network communication**
- **We need standards for time synchronization and *when* to time stamp information in the end-to-end communication path**
- **Using synchronization and time stamping, we can decouple application node time from communication network time**

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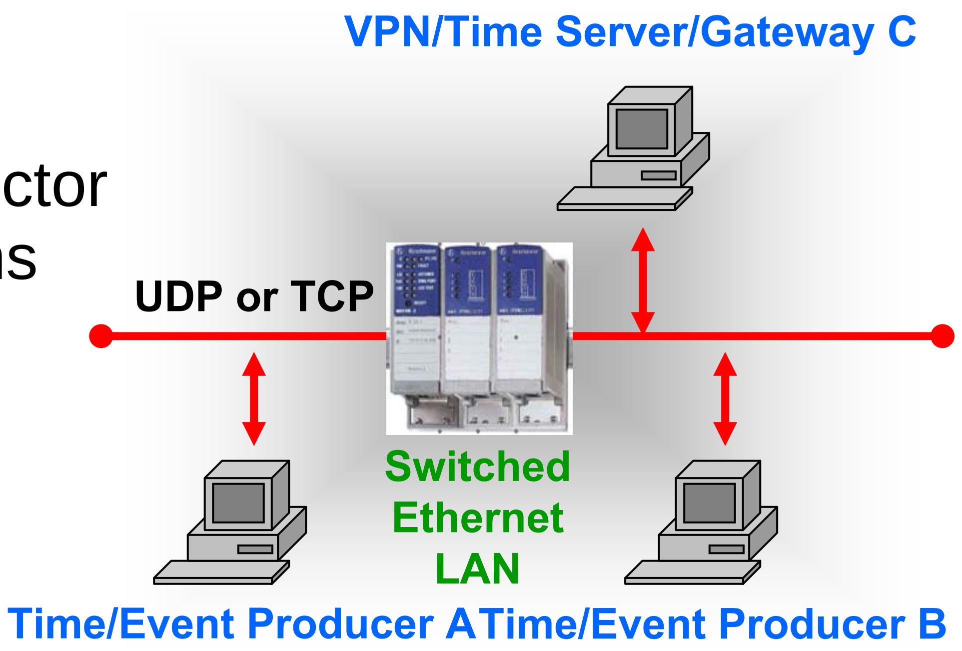
NIST / University of Michigan Project

- Performance testing of IEEE 1588 for semiconductor manufacturing applications
  - Data collection
  - Remote monitoring



- IEEE 1588 testbed in operation
  - 1588 hardware I/O cards
  - XML traffic generators
  - Routines for encapsulation, e.g., VPN, OPC, UDP, as necessary
  - Performance analysis software

NIST / University of Michigan Project

- Benchmark common protocol scenarios (XML, VPN, etc.)
- Interface "A" traffic volume analysis and performance benchmarking
  - Simple equipment EDA traffic simulators
- APC scenarios performance analysis
  - Equipment EDA and PCS simulators; control scenarios
- Exploration of Time Synchronization for Semiconductor Manufacturing
  - Identification of weak links in equipment, software systems, standards, etc.
  - Input into SEMI standards effort

SEMI *Time Synchronization Task Force* Progress

- **Characterized processes** from I/O level up through MES in terms of timing accuracy and precision requirements
- **Surveyed existing SEMI standards** to determine current time protocols and timing needs
- **Developed ballot standard**
  - "Provisional Specification for the Usage and Definition of Time Synchronization"
    - Defines key requirements for factory applications and equipment to maintain and manage data and time accurately
    - Currently out for early balloting
- **Impact on existing I&CC standards is expected**
  - EDA, sensor bus, PCS, etc.

Sample Time Synchronization Requirements

Application	Description/Needs	Absolute Accuracy	Relative Accuracy	Min Data Sampl Interval	Precision Required
Real-Time Data Base (Data Repository, Historian)	Provide high-speed storage and retrieval of detailed equipment and process data to support wide range of application needs.	5 sec	10 ms	20 ms	1 ms
Control / Fault Model Development	Analyze equipment, process, metrology, and yield information to development control models used for APC applications.	10 sec	10 ms	1 min	1 ms
Statistical Process Control (SPC)	Track equipment / process parameters and flag SPC rule violations; not a real-time control technique.	5 sec	100 ms	1 sec	1 ms
Run-to-Run Control (R2R)	Adjust recipe parameters between individual production runs (wafer, lot, batch) based on results of previous runs; uses combination of metrology and equipment data to calculate adjustments.	5 sec	50 ms	100 ms	1 ms
Fault Detection and Classification (FDC)	Analyze equipment and process parameters to ensure tool is in its acceptable operating envelope; identify and classify (or prevent) equipment faults and interrupt processing accordingly.	5 sec	10 ms	50 ms (in process) 20 sec (post-process)	1 ms
Event / Alarm Management	Capture, analyze, communicate, and support user response to events and alarms across the production environment.	5 sec	1 sec	1 sec	1 ms
Scheduling/ Dispatching (RTD)	Provides ability to accurately estimate time of completion, arrival of wafers, and to prepare a tool for wafer processing.	5 sec	2 sec	2 sec	1 ms
Factory Time Synchronization	Maintain and provide reference time for all systems in the fab.	5 sec	1 ms	10 sec	1 ms

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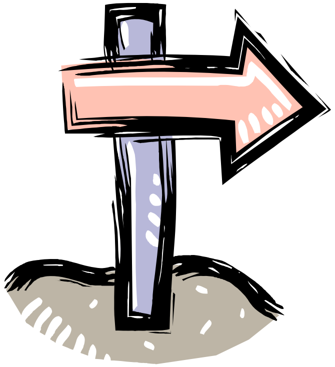
Key Points

- Many efforts in implementing EDA and PCS implementation will fail if data quality is not addressed
- Lack of time synchronization and accurate time stamping is a common source of poor data quality
- The weak link is often the tool software performance, so *where you time stamp* is very important
- NIST, The University of Michigan and SEMI are working together to address this issue, with the end result being standards and prototypes that will impact PCS, EDA and e-diagnostics

Future Efforts



- Identify and quantify the weak links in timing and time synchronization for APC
- Provide cost / benefit analysis
  - What level of time synchronization is needed at various places throughout the fab; e.g., is hardware time synchronization required?
- SEMI standards for time synchronization and time stamping
- Raise awareness
  - APC applications are only as good as the data and data quality is usually the weak link
  - Lack of time synchronization is hindering our movement to fab-wide APC, especially for Fault Detection
  - Techniques are available to provide enterprise-wide time synchronization
- Education
  - When and how to apply time synchronization
- Impact the ITRS; indicate importance of time synchronization, time stamping and data quality in general

Thank You !! ☺

- **For further information**
  - **James Moyne: moyne@umich.edu**
  - **UM-ERC-RMS: http://erc.engin.umich.edu**
  - J. T. Parrott, J. R. Moyne, D. M. Tilbury, "Experimental Determination of Network Quality of Service in Ethernet: UDP, OPC, and VPN," *Proceedings of the American Control Conference,* Minneapolis, MN, June 2006.

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- **Questions?**