Low frequency noise characterizations of ZnO nanowire field effect transistors

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We fabricated ZnO nanowire field effect transistors (FETs) and systematically characterized their low frequency (f) noise properties. The obtained noise power spectra showed a classical $1/f$ dependence. A Hooge's constant of 5×10^{-3} was estimated from the gate dependence of the noise amplitude. This value is within the range reported for complementary metal-oxide semiconductor (CMOS) FETs with high-k dielectrics, supporting the concept that nanowires can be utilized for future beyond-CMOS electronic applications from the point of view of device noise properties. ZnO FETs measured in a dry O_2 environment displayed elevated noise levels that can be attributed to increased fluctuations associated with O_2^- on the nanowire surfaces. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2496007]

I. INTRODUCTION

Semiconductor nanowires (NWs) represent an important class of nanoscale building blocks for future beyond-complementary-metal-oxide-semiconductor (CMOS) electronics.[1] One fundamental factor that determines the performance of electronic devices is the signal-to-noise ratio, which poses the lower limit for device operation.[2–4] Hence, a thorough understanding of the noise properties is critical for the successful design and integration of semiconducting nanowire functional units in nanoelectronics. Low frequency (f) noise, which contains important information about current transport and fluctuations in materials and devices, has been traditionally utilized as a quality and reliability indicator for semiconductor devices.[2–6] Recently, extensive low frequency noise characterizations of carbon nanotube field effect devices have been carried out,[7–14] which has significantly improved our knowledge of the noise properties in these devices. However, so far there are only limited reports of noise characterizations of semiconductor nanowire devices[15] despite the fact that such structures hold great promise for future nanoelectronic applications. In this study, we fabricate ZnO nanowire field effect transistors (FETs) and characterize their low frequency noise properties. ZnO, a wide band gap (~3.36 eV at room temperature) semiconductor material, has a wurtzite crystal structure and is intrinsically n-type because the zinc interstitials and/or oxygen vacancies act as dominant donors.[16–18] Lately, ZnO NWs have found potential applications as photodetectors, light-emitting diodes, and gas sensors.[19] ZnO NWs have also been configured as FETs, and their electronic transport properties have been investigated.[20–22] In this work, we synthesized single crystalline ZnO NWs, fabricated individual ZnO NW FETs, and subsequently characterized their noise properties. The Hooge's parameter in the noise characteristics was determined from the gate dependence of the noise amplitude. Furthermore, since ZnO NW FETs show promise for oxygen sensing applications,[21] the noise properties of the ZnO NW FETs have also been characterized in a dry oxygen environment.

II. EXPERIMENTAL SECTION

A. ZnO nanowire synthesis

ZnO nanowires were synthesized by thermally vaporizing a mixed source of commercially available ZnO powder (99.995%) and graphite powder (99%) with a ratio of 1:1 in a tube furnace. A c-plane sapphire was used as the substrate for the ZnO nanowire growth. After an initial cleaning, a 3 nm Au thin film was deposited on the sapphire substrate. Then, the substrate and the source materials were loaded into a quartz tube and the ZnO NWs were grown on the substrate surface at a temperature of 920 °C for 20 min under the flow of a gas mixture of O_2 and Ar (0.2% O_2 in Ar) with a flow rate of 50 SCCM.

Figure 1(a) shows the field emission scanning electron microscopy (FE-SEM) image (tilted view) of vertically and uniformly grown ZnO NWs on the entire sapphire substrate. Figure 1(b) shows a high-resolution transmission electron microscopy (HR-TEM) image and a selected-area electron diffraction pattern (inset) of the ZnO NWs. The discrete diffraction spots indicate that the ZnO nanowires are hexagonal wurtzite single crystalline, as previously reported.[23] The x-ray diffraction spectrum in Fig. 1(c) further shows that the as-synthesized ZnO NWs have the hexagonal wurtzite struc-

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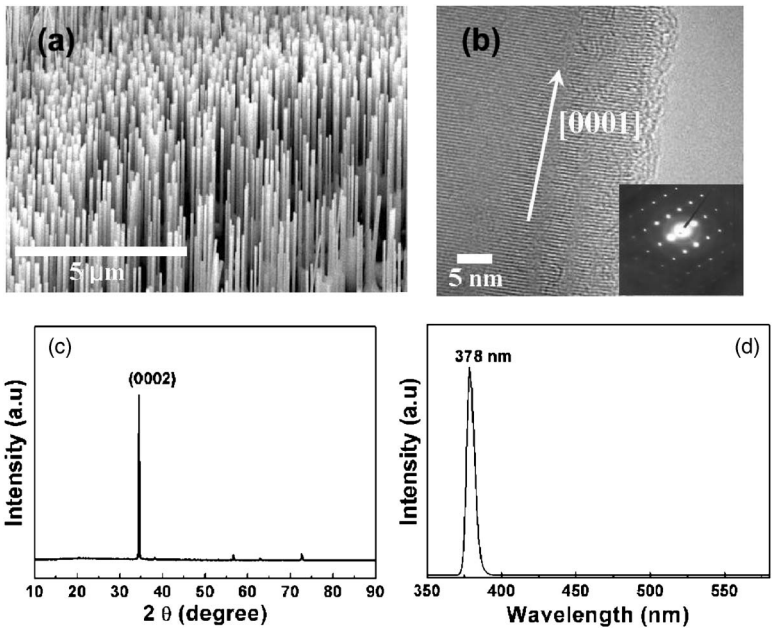

FIG. 1. (a) FE-SEM image of ZnO NWs grown on a sapphire substrate (tilted view). (b) HR-TEM image of an individual ZnO nanowire showing its [0001] preferred growth direction. The inset shows a selected-area electron diffraction pattern. (c) X-ray diffraction spectrum of the ZnO NWs. (d) PL emission spectrum showing a strong emission at ~378 nm.

ture with lattice parameters of $a=0.33$ nm and $c=0.52$ nm. A single peak at approximately 378 nm is observed in the photoluminescence (PL) spectrum [Fig. 1(d)] of the ZnO NWs. This peak is attributed to near the band-edge recombination of free excitons.[24] These results confirmed that these are high quality single crystalline ZnO NWs and the preferred growth direction is [0001].

B. FET device fabrication

The grown ZnO NWs were removed from the substrate by a brief sonication in ethanol (30–60 s). The nanowires in solution are then dropped onto a 100 nm thick, thermally grown oxide on a highly doped *p*-type silicon substrate that can be used as a gate electrode. Ti/Au (30 nm/200 nm) contacts were deposited by using an electron beam evaporator and defined by standard photolithography and a lift-off process to form the source and drain electrodes. The distance between source and drain electrodes is typically 2–4 μm. The inset in Fig. 2(a) shows a SEM image of a typical ZnO NW FET device. Current-voltage characteristics of the ZnO NW FETs were measured by using a semiconductor parameter analyzer. The low frequency noise characterization for these devices was performed by using a typical noise measurement setup composed of a low noise dc biasing source, a low noise current amplifier, and a dynamic spectrum analyzer. All of the measurements were carried out at room temperature and under moderate vacuum (~4 mTorr) unless otherwise mentioned. The noise properties of the ZnO NW FETs were also measured in a dry oxygen environment.

III. RESULTS AND DISCUSSION

A. ZnO NW FET properties

Figure 2(a) shows typical drain current versus drain voltage (I_d-V_d) characteristics of a ZnO NW FET device at different gate biases (V_g), where V_g was applied to the silicon substrate in a back gate configuration. The conduction channel in this particular FET device is a ZnO NW of diameter of 140 nm with a channel length (L) of 4 μm. Figure 2(b) shows the drain current versus gate voltage (I_d-V_g) characteristics of the same device at a fixed drain bias of 1 V. These characteristics display the expected *n*-type semiconducting transport behavior.[20–22] From the I_d-V_g characteristics, a gate threshold voltage (V_{th}) of 0.05 V was extracted according to the method described in Ref. 25. The on/off ratio of this device at $V_d=1$ V is ~10^7 (comparing I_d at $V_g=8$ V and -3 V) and the subthreshold slope is ~270 mV/decade. The carrier concentration (n) in the nanowire can be calculated using the equation[13,21,22,26,27]

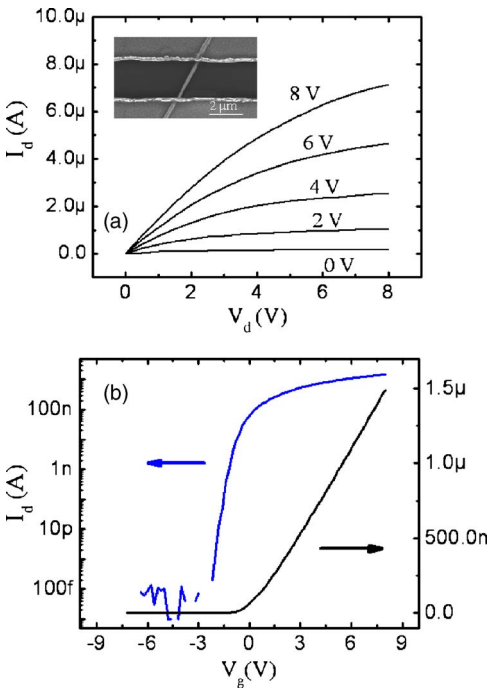

FIG. 2. (Color online) (a) Typical I_d-V_d characteristics of a ZnO NW FET at gate biases of 0, 2, 4, 6, and 8 V measured at room temperature and under a vacuum of 4 mTorr. The inset shows a SEM image of a typical ZnO NW FET device. (b) Semilogarithmic (left axis) and linear (right axis) plots of the I_d-V_g characteristic of the same device at a drain bias of 1 V.

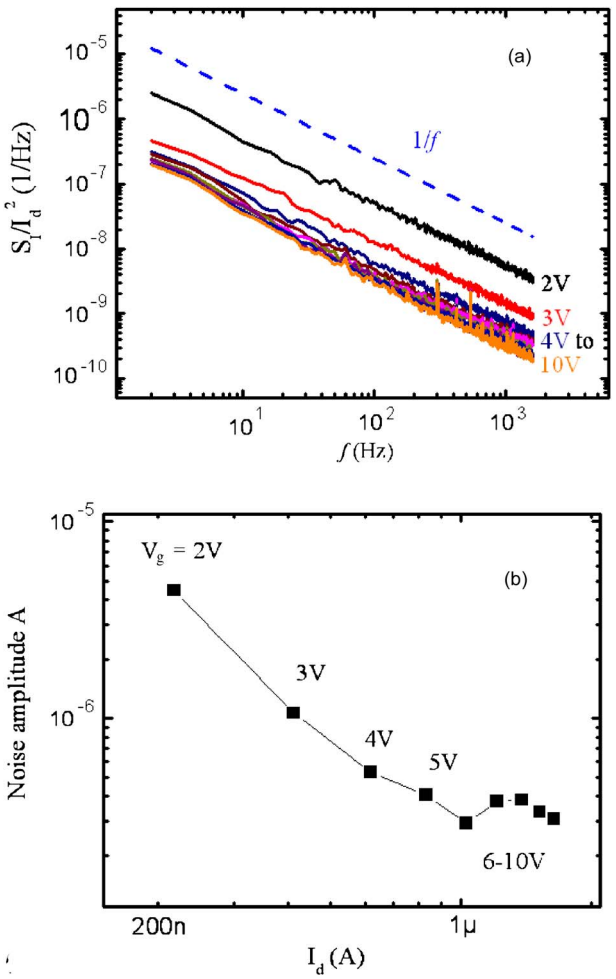

FIG. 3. (Color online) (a) Typical normalized drain current noise power spectra at gate biases from 2 to 10 V measured in the vacuum. V_d=1 V and the frequency range is from 1 Hz to 1.6 kHz. The dashed line indicates the ideal $1/f$ dependence. (b) Noise amplitude A obtained from Fig. 2(a) and Eq. (2) plotted as a function of the drain current. The numbers in the plot are the gate biases. V_d=1 V.

$$n = \frac{|V_g - V_{\text{th}}|}{e} \frac{2\pi\varepsilon\varepsilon_0}{\cosh^{-1}(1 + h/r)}, \tag{1}$$

where ε is the dielectric constant of the SiO_2, ε_0 is the permittivity of free space, h is the oxide layer thickness, and r is the nanowire radius. $2\pi\varepsilon\varepsilon_0/\cosh^{-1}(1+h/r)$ is the gate capacitance (C_g) per unit length of the system presuming a cylindrical nanowire.[27] In our case since the device diameter is comparable to the oxide thickness, the simplified gate capacitance equation $2\pi\varepsilon\varepsilon_0/\ln(2h/r)$ is not valid. For our device, a carrier concentration of 5.2×10^7 cm^{-1} was estimated at a gate bias of 6 V by using h=100 nm, r=70 nm, and ε =3.9. Similarly, the effective electron mobility was calculated to be ~53 $cm^2/V\,s$ at a drain bias of 1 V by using $\mu_e=(dI/dV_g)L/(C_gV_d)$,[21,22,26] where dI/dV_g was obtained from the data in Fig. 2(b). These transport parameters of the ZnO NW FET device are consistent with previously published results.[21]

B. Noise characteristics

Low frequency noise measurements of the ZnO NW FETs were carried out to study the current fluctuations in single nanowire devices. Figure 3(a) shows typical normalized drain current noise power spectra (S_I) at selected gate biases measured in vacuum. The drain bias was kept at 1 V and the frequency range was varied from 1 Hz to 1.6 kHz. For $1/f$-type fluctuations, the noise behavior can be described by[3,12,13]

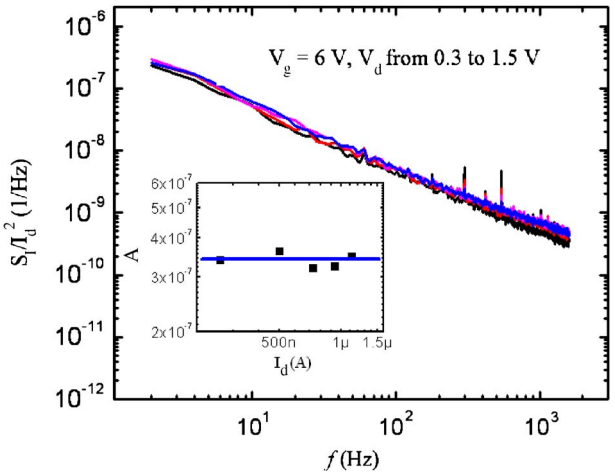

FIG. 4. (Color online) Normalized drain current noise power spectra at different drain biases from 0.3 to 1.5 V with a step of 0.3 V. The gate bias is kept at 6 V. The inset shows the noise amplitude as a function of drain current at different drain biases (the line is a guide to the eye).

$$S_I = \frac{AI^2}{f^\beta}, \tag{2}$$

where A is the noise amplitude and the frequency exponent β is ideally 1. As shown in Fig. 3(a), ZnO NW FET exhibited $1/f$ noise behavior with β values in the range of 0.92–1.02, which were obtained by doing linear fits to each spectrum in Fig. 3(a). As a comparison, a dashed line indicating ideal $1/f$ dependence is also plotted in this figure. No generation-recombination (GR) noise was observed for our devices at room temperature as long as $V_g \geqslant V_{\text{th}}+1$ V. From the data in Fig. 3(a) the noise amplitude A can be obtained at f=1 Hz according to Eq. (2). Figure 3(b) shows the noise amplitude A as a function of the drain current at different gate voltages. The noise amplitude decreases almost linearly at low gate biases and becomes saturated at high gate biases. Figure 4 is the normalized drain current noise spectra at a gate voltage of 6 V and drain voltages from 0.3 to 1.5 V with 0.3 V interval, which are in the linear current regime of the I_d-V_d characteristics [see Fig. 2(a)]. The inset shows the noise amplitude versus drain current curve for the same plot. As Fig. 4 shows, the device current noise S_I is proportional to I_d^2 in the linear regime at a constant gate voltage, where the device can be treated as a conventional resistor. In summary, noise characterizations of ZnO NW FETs at different drain and gate voltages reveal that the noise behavior in the devices at low frequencies is $1/f$ type, and the corresponding noise amplitudes are dependent on the gate modified carrier numbers in the devices. Since the normalized noise is almost independent of the applied drain bias in the linear regime, it is most likely that the noise originates from the channel. Another possible noise source is from the contacts between the electrodes and the nanowires, which has been discussed

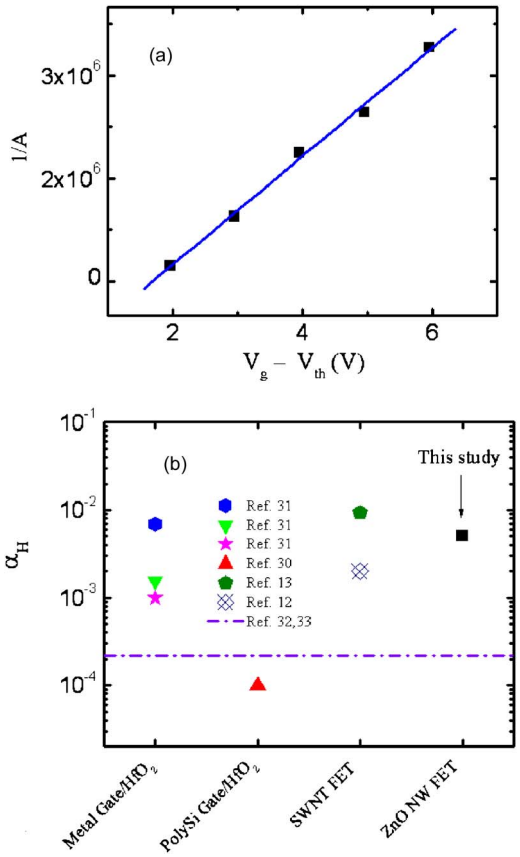

FIG. 5. (Color online) (a) The inverse of the noise amplitude plotted as a function of $V_g - V_{th}$. The solid line is a linear fit to the data (squares). Hooge's constant is calculated from the slope of the linear fit. (b) Summary plot of Hooge's constant obtained in this study (black square) with previously published data for poly-silicon gate/HfO_2, metal gate/HfO_2, and single-wall nanotube FET devices. Different values of the same type of device are from different reports. The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node.

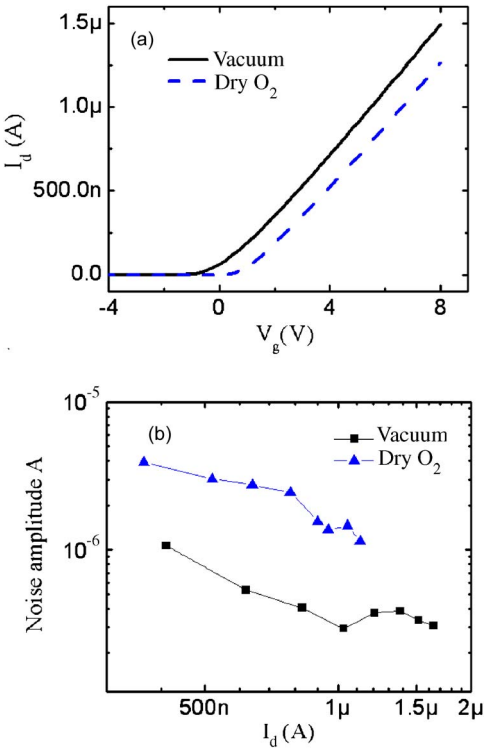

FIG. 6. (Color online) (a) I_d-V_g characteristics of the ZnO NW FET device in vacuum and dry oxygen environments. $V_d = 1$ V. (b) Noise amplitude as a function of drain current under different gate biases in vacuum and the oxygen environments. $V_d = 1$ V.

recently in carbon nanotube FETs.[14] Further noise characterizations of NW FETs with different channel lengths or different contacts will help clarify this issue.

According to Hooge's empirical law, the $1/f$ noise amplitude can be expressed as[2]

$$A = \frac{\alpha_H}{N}, \tag{3}$$

where α_H is the Hooge's constant and N is the total carrier number in the system. This relationship was introduced to describe the $1/f$ noise in homogenous bulk materials, and α_H can be used to compare $1/f$ noise in different systems regardless of the specific device parameters and measurement conditions.[2,28,29] For bulk materials α_H is typically on the order of 10^{-3}. By using Eq. (1) and the expression of the gate capacitance, the inverse of A can be expressed as[13]

$$\frac{1}{A} = \frac{C_g L}{e\alpha_H}|V_g - V_{\text{th}}|. \tag{4}$$

Figure 5(a) shows $1/A$ vs $(V_g - V_{\text{th}})$ calculated from the gate dependence of the noise amplitude [Fig. 3(a)]. α_H can be determined from a linear fit [solid line in Fig. 5(a)] to the data according to Eq. (4). By using the abovementioned device parameters, α_H is estimated to be 5×10^{-3} for the ZnO NW FET device. Figure 5(b) shows the Hooge's constant of the ZnO NW FETs, compared with previously published data of poly-silicon gate/HfO_2,[30] metal gate/HfO_2,[31] and single-wall nanotube FET devices.[12,13] The dash-dotted line shows the ITRS requirement on α_H for the 45 nm technology node.[32,33] As can be seen in Fig. 5(b), the Hooge's constant of our device is similar to values reported recently for carbon nanotube FETs.[12,13] Despite the nanowires' much higher surface-to-volume ratio, the obtained α_H is also comparable to that of future type CMOS FETs with high-k materials, such as HfO_2 as gate dielectrics.[30,31] This comparison of NW FET noise data with that measured in other emerging device technologies supports the concept that, from the point of view of device noise properties, NWs can be used as device components for beyond CMOS electronic applications.

C. Noise characteristics in oxygen

Several groups have previously reported the oxygen sensing properties of ZnO NWs.[20–22] In order to investigate the change of the noise characteristics of ZnO NW FETs under the oxygen environment, we have performed noise measurements in a dry oxygen environment. The devices that were originally tested in vacuum were left in dry oxygen under a pressure of 900 Torr for 2 days before the measurements to ensure that oxygen molecules occupy the majority of the surface vacancy sites of the ZnO NWs. Figure 6(a) shows typical device I_d-V_g characteristics before and after the introduction of the dry O_2. Compared to the vacuum data, the threshold voltage shifted from 0.05 to 0.87 V under the

oxygen environment. This observation agrees with previously published reports that showed ZnO NW FETs' oxygen sensing properties.[21,22] It has been proposed that O_2 molecules can be absorbed at surface vacancy sites of the metal-oxide nanowires and then accept electrons to form O_2^-.[17,21] These chemisorbed O_2^- lead to the observed threshold voltage shift and deplete surface electron states; thus, at a given voltage, the channel carrier concentration is reduced and there is an accompanying decrease of the conductivity.[21] Due to the threshold voltage shift, the carrier concentration in the channel has been reduced from 5.2×10^7 cm^{-1} (under vacuum) to 4.5×10^7 cm^{-1} (in dry O_2) at a gate bias of 6 V if we assume that the average dielectric constant is the same for both cases. The mobility has also slightly decreased by ~6%. Figure 6(b) shows the device noise amplitude as a function of drain current at various gate biases under different environments. As it reveals, the device noise level in the dry oxygen environment is nearly an order of a magnitude larger than that in vacuum. Measurements of the ZnO NW FETs in dry nitrogen environment did not show a significant noise amplitude change compared to the vacuum data. The higher noise level in the oxygen environment can be elucidated by considering Hooge's empirical law [Eq. (3)]. A similar fit to the oxygen noise data according to Eq. (4) gives a Hooge's constant of 4×10^{-2} for ZnO NW FETs under the oxygen environment. Compared to the observed α_H of 5×10^{-3} in vacuum, α_H in the oxygen environment is almost eight times larger. We propose that the microscopically dynamic impact of the surface bound O_2^- species on the charge transport[22] significantly increased the carrier number fluctuations related to electron trapping/detrapping events and accompanied scattering fluctuations in the device channel, which was reflected as an increased Hooge's constant under the oxygen environment. This is similar to the situation in traditional planar MOSFET devices, where the increase of fixed charges by, for example, bias stressing or ionizing irradiation results in a shift of threshold voltage and an elevated noise level.[28,34] The interactions between the O_2^- species and carriers increased both number fluctuations and mobility fluctuations in the channel and therefore generated a larger noise amplitude for the ZnO NW FETs in the oxygen environment.

IV. CONCLUSIONS

In conclusion, we carried out noise characterizations of ZnO NW FETs, and the obtained noise spectra displayed a classical $1/f$ frequency dependence. Examination of the gate dependence of the noise amplitude gave a Hooge's constant of 5×10^{-3} for the ZnO NW FETs, which is within the range of reported values of bulk materials or CMOS FETs with high-k dielectrics, supporting the feasibility of utilizing nanowires for future beyond-CMOS electronic applications. Measurements of the devices in dry O_2 environment exhibited a higher noise level, which could be attributed to the increased channel fluctuations associated with O_2^- bound at the ZnO surface. This study also suggests that the changes of the noise characteristics under different environments could be utilized as a sensitive method for sensing applications.

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[1] C. M. Lieber, MRS Bull. **28**, 486 (2003).
[2] F. N. Hooge, Phys. Lett. **29A**, 139 (1969).
[3] P. Dutta and P. M. Horn, Rev. Mod. Phys. **53**, 497 (1981).
[4] M. J. Buckingham, *Noise in Electronic Devices and Systems* (Wiley, New York, 1983).
[5] W. Hong, Microelectron. Reliab. **43**, 585 (2003).
[6] B. K. Jones, Adv. Electron. Electron Phys. **87**, 201 (1994).
[7] H. W. C. Postma, T. F. Teepen, Z. Yao, and C. Dekker, *Proceedings of the XXXVI Rencontre De Moriond* (EDP Sciences, France, 2001).
[8] P. G. Collins, M. S. Fuhrer, and A. Zettl, Appl. Phys. Lett. **76**, 894 (2000).
[9] E. S. Snow, J. P. Novak, M. D. Lay, and F. K. Perkins, Appl. Phys. Lett. **85**, 4172 (2004).
[10] P.-E. Roche, M. Kociak, S. Gueron, A. Kasumov, B. Reulet, and H. Bouchiat, Eur. Phys. J. B **28**, 217 (2002).
[11] F. Liu, M. Bao, H. Kim, K. L. Wang, C. Li, X. Liu, and C. Zhou, Appl. Phys. Lett. **86**, 163102 (2005).
[12] Y.-M. Lin, J. Appenzeller, J. Knoch, Z. Chen, and Ph. Avouris, Nano Lett. **6**, 930 (2006).
[13] M. Ishigami, J. H. Chen, E. D. Williams, D. Tobias, Y. F. Chen, and M. S. Fuhrer, Appl. Phys. Lett. **88**, 203116 (2006).
[14] A. Vijayaraghavan *et al.*, J. Appl. Phys. **100**, 024315 (2006).
[15] S. Reza, G. Bosman, S. Islam, T. I. Kamins, S. Sharma, and R. S. Williams, IEEE Trans. Nanotechnol. **5**, 523 (2006).
[16] V. E. Henrich and P. A. Cox, *Surface Science of Metal Oxides* (Cambridge University Press, Cambridge, 1996).
[17] Y. Zhang, A. Kolmakov, S. Chretien, H. Metiu, and M. Moskovits, Nano Lett. **4**, 403 (2004).
[18] D. C. Look, J. W. Hemsky, and J. R. Sizelove, Phys. Rev. Lett. **82**, 2552 (1999).
[19] Z. L. Wang, J. Phys.: Condens. Matter **16**, R829 (2004).
[20] Y. W. Heo, L. C. Tien, D. P. Norton, B. S. Kang, F. Ren, B. P. Gila, and S. J. Pearton, Appl. Phys. Lett. **85**, 2002 (2004).
[21] Z. Fan, D. Wang, P. Chang, W. Tseng, and J. G. Lu, Appl. Phys. Lett. **85**, 5923 (2004).
[22] J. Goldberger, D. J. Sirbuly, M. Law, and P. Yang, J. Phys. Chem. B **109**, 9 (2005).
[23] M. H. Huang, Y. Wu, H. Feick, N. Tran, E. Weber, and P. Yang, Adv. Mater. (Weinheim, Ger.) **13**, 113 (2001).
[24] S. C. Lyu, Y. Zhang, H. Ruh, H. Lee, H. Shim, E. Suh, and C. J. Lee, Chem. Phys. Lett. **363**, 134 (2002).
[25] G. Ghibaudo, Electron. Lett. **24**, 543 (1998).
[26] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[27] D. Wang, Y. Chang, Q. Wang, J. Cao, D. B. Farmer, R. G. Gordon, and H. Dai, J. Am. Chem. Soc. **126**, 11602 (2004).
[28] L. K. J. Vandamme, X. Li, and D. Rigaud, IEEE Trans. Electron Devices **41**, 1936 (1994).
[29] F. N. Hooge, IEEE Trans. Electron Devices **41**, 1926 (1994).
[30] C. Claeys, E. Simoen, A. Mercha, L. Pantisano, and E. J. Young, J. Electrochem. Soc. **152**, F115 (2005).
[31] B. Min, S. P. Devireddy, Z. Çelik-Butler, F. Wang, A. Zlotnicka, H. Tseng, and P. J. Tobin, IEEE Trans. Electron Devices **51**, 1979 (2004).
[32] International Technology Roadmap for Semiconductors, http://www.itrs.net/
[33] M. von Haartman, Ph.D. dissertation, Royal Institute of Technology, Stockholm, Sweden, 2006.
[34] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, IEEE Trans. Electron Devices **41**, 1953 (1994).