Automated Parameter Extraction Software for High-Voltage, High-Frequency SiC Power MOSFETs

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Abstract*-Previously developed IGBT Model Parameter extrACtion Tools (IMPACT) are extended to include the material parameters and device structures of SiC power devices. These software tools extract the data necessary to establish a library of SiC power device component models and provide a method for quantitatively comparing different device types and establishing performance metrics for device development. In this paper, the SiC--IMPACT parameter extraction sequence is demonstrated using several 10 kV SiC power MOSFET device design types and the results are compared with results for 2-kV SiC Power MOSFETs and for commercial Silicon power MOSFETs with voltage blocking capabilities of 55 V, 400 V, and 1 kV.

NOMENCLATURE

A	Device active area (cm^2)
A_{ds}	Drain-body junction area (cm^2)
A_{gd}	Gate-drain overlap area (cm^2)
C_{dsj}	Drain-source junction capacitance (F)
C_{gd}	Gate-drain capacitance (F)
C_{gi}	Gate-inversion layer capacitance (F)
C_{gdj}	Gate-drain junction capacitance (F)
C_{gs}	Gate-source capacitance (F)
C_{oxd}	Gate-drain overlap oxide capacitance (F)
dV_{Tl}	Low current threshold voltage differential (V)
ε_{semi}	Semiconductor dielectric constant (F/cm)
F_{xjbe}	Fraction depletion charge at gate-drain overlap edge
F_{xjbm}	Fraction depletion charge at gate-drain overlap middle
I_{mos}	MOSFET channel current (A)
I_{mosl}	Low current region component of I_{mos} (A)
I_{mosh}	High current region component of I_{mos} (A)
k	Boltzmann's constant (J/K)
K_f	Linear region transconductance factor
K_{fl}	Low current region transconductance factor
K_p	Saturation region transconductance (A/V^2)
K_{psat}	Extracted saturation region transconductance (K_p), (A/V^2)
K_{plin}	Extracted linear region transconductance ($K_f K_p$), (A/V^2)
μ_n	Bulk electron mobility ($cm^2/V{\cdot}s$)
N_b	Base dopant density (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
P_{vf}	Pinch-off voltage factor
q	Fundamental electronic charge (C)
R_b	Epitaxial layer resistance (Ω)
R_s	Series drain resistance (Ω)
T	Chip surface temperature (K)
θ	Transverse electric field parameter (V^{-1})
V_{bi}	Built-in junction potential (V)
V_{bigd}	Built-in potential of gate-drain overlap region (V)
V_{dds}	Drain-source terminal voltage (V)
V_{ds}	MOSFET channel voltage (V)
V_{gs}	Gate-source voltage (V)
V_{Td}	Gate-drain overlap depletion threshold (V)
V_{Tdi}	Gate-drain overlap inversion threshold voltage (V)
$V_{Tdiedge}$	V_{Tdi} at body edge of gate-drain overlap (V)
V_{Tl}	Low current MOSFET channel threshold voltage (V)
V_{Th}	High current MOSFET channel threshold voltage (V)
W	Quasineutral drift region width (cm)
W_b	Metallurgical drift region width (cm)
W_{dsj}	Drain-body depletion width (cm)
y	Pinch-off voltage exponent

* Contribution of NIST; not subject to copyright. The devices discussed in this paper were produced by Cree Inc. under a DARPA WBST HPE Phase 1 contract managed by John Zolper (DARPA) and monitored by Harry Dietrich (ONR).

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I. INTRODUCTION

Recent breakthroughs in Silicon Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10-kV, 20-kHz power switching capability [1]. With the emergence of this new SiC device technology, various industry and government programs have been established to investigate future high voltage power conversion systems enabled by these devices [2, 3]. In addition, circuit simulator models have been developed to simulate the performance of SiC power devices in future high voltage power conversion systems [4, 5]. The purpose of this paper is to develop and demonstrate the model parameter extraction tools necessary to extract parameters for the SiC power MOSFET models.

Previously, a software package called IGBT Model Parameter extrACtion Tools (IMPACT) was introduced to provide a method to extract the 20 physical and structural parameters for the Hefner IGBT model as described in [5, 6]. In this work, the IMPACT software tools have been extended to include the material parameters and device structures of SiC power devices. The new software tools are called SiC--IMPACT. In addition, high-voltage electronic instrumentation hardware has been developed and interfaced with the parameter extraction tools to enable measurement of the device capacitance characteristics up to 5 kV and the capacitance-voltage extraction sequence has been extended due to the importance of the output capacitance for high-voltage SiC devices.

The new SiC--IMPACT software tools provide the capability to extract the data necessary to establish a library of SiC power device component models. The extracted parameters also provide a method for quantitatively comparing different device types and establishing performance metrics for device development. In this paper, the parameter extraction sequence is demonstrated using several 10 kV SiC power MOSFET device design types from the DARPA WBST HPE Phase 1 program [7] and the results are compared with results for 2-kV SiC Power MOSFETs and for commercial silicon power MOSFETs with voltage blocking capabilities of 55 V, 400 V, and 1 kV.

II. PARAMETER EXTRACTION USING SIC-IMPACT

The IMPACT software package consists of five programs: LFTMSR, BETAMSR, SATMSR, LINMSR, and CAPMSR [6]. In this paper, the software tools will be demonstrated using MOSFETs because SiC IGBTs are at an early stage of development. For the power MOSFET devices, only three of the programs are necessary (SATMSR, LINMSR, and CAPMSR) because the bipolar conductivity modulation is not present. Table 1 provides the power MOSFET model equations [5,8]; and Table 2 provides a list of MOSFET model parameters, the name of the automated extraction program that implements the extraction step, and the electrical characteristics that are used to extract each parameter [5, 6]. To perform the parameter extraction, the material type is first selected as demonstrated in Fig.1, and then the extraction steps are performed in the order that they are listed in Table 2.

In the first extraction step in Table 2, the device active area is extracted by visual inspection of the chip size. Three basic types of electrical measurements are used to extract the remaining model parameters: 1) the saturation current versus gate voltage (V_{GS}) is used to extract the MOSFET threshold voltage (V_T) and channel transconductance ($K_P = K_{Psat}$) parameters including high and low current effects (SATMSR). 2) The on-state voltage versus V_{GS} characteristic is used to extract the linear region transconductance (K_{Plin}), the drain series resistance (R_S), the drift region dopant density (N_B), the MOSFET channel specific resistance ($R_{SPmos} = R_{SP\_channel}$), and the epitaxial-layer specific on-resistance (R_{SPepi}) parameters (LINMSR). 3) The gate-charge and gate-drain charge characteristics are used to extract the gate-source capacitance (C_{GS}), the gate-drain overlap oxide capacitance (C_{OXD}), the gate-drain area (A_{GD}), and the gate-drain overlap depletion threshold (V_{TD}). The following subsections demonstrate and discuss each of the three extraction programs.

A. Saturation Region Parameter Extraction (SATMSR)

Fig.2 shows the SATMSR front panel. In SATMSR, the saturation current versus V_{GS} is used to extract V_T, K_P, low current transconductance factor (K_{FL}), low current threshold voltage differential (dV_{TL}), and the temperature coefficients of threshold voltage (V_{TI}) and transconductance (K_{PI}) [8].

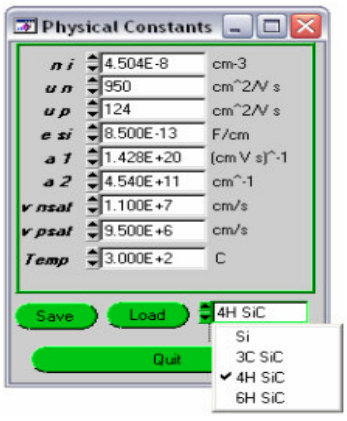

Fig. 1: Temperature dependent material parameters for 4H-, 6H-, and 3C-SiC added to IMPACT extraction tools.

Table 1. Power MOSFET Equations

MOSFET Channel Currents

$$I_{mos} = I_{mosh} + I_{mosl}$$

$$V_{Th} = V_T + \frac{K_{fl}}{1 - K_{fl}} dV_{Tl}$$

$$V_{Tl} = V_T - dV_{Tl}$$

Linear Region:

$$y = \frac{K_f}{K_f - \frac{P_{vf}}{2}}$$

$$I_{mosl} = \frac{K_{fl} K_f K_p \left[(V_{gs} - V_{Tl}) V_{ds} - {P_{vf}}^{y-1} V_{ds}^{y} (V_{gs} - V_{Tl})^{2-y} \right]}{(1 + \theta (V_{gs} - V_{Tl}))}$$

$$\text{for} \quad V_{ds} \le \frac{V_{gs} - V_{tl}}{P_{vf}}$$

$$I_{mosh} = \frac{(1 - K_{fl}) K_f K_p \left[(V_{gs} - V_{Th}) V_{ds} - {P_{vf}}^{y-1} V_{ds}^{y} (V_{gs} - V_{Th})^{2-y} \right]}{(1 + \theta (V_{gs} - V_{Th}))}$$

$$\text{for} \quad V_{ds} \le \frac{V_{gs} - V_{th}}{P_{vf}}$$

Saturation Region:

$$I_{mosl} = \frac{K_{fl} K_p (V_{gs} - V_{Tl})^2}{2(1 + \theta (V_{gs} - V_{Tl}))} \qquad \text{for } V_{ds} > \frac{V_{gs} - V_{tl}}{P_{vf}}$$

$$I_{mosh} = \frac{(1 - K_{fl}) K_p (V_{gs} - V_{Th})^2}{2(1 + \theta (V_{gs} - V_{Th}))} \qquad \text{for } V_{ds} > \frac{V_{gs} - V_{th}}{P_{vf}}$$

On-State Equations

$$V_{dds} = V_{ds} + I_d (R_b + R_s)$$

$$R_b = \frac{W}{qAN_b\mu_n} \qquad \text{where} \qquad W = W_b - W_{dsj}$$

$$\mu_n(T) = \frac{947}{1 + \left(\frac{N_b}{1.94 \cdot 10^{17}} \right)^{0.61}} \cdot \left(\frac{T}{300K} \right)^{-2.15}$$

Transient Equations

$$W_{dsj} = \sqrt{\frac{2\varepsilon_{semi}(V_{ds} + V_{bi})}{qN_b}}$$

$$C_{dsj} = A_{ds}\varepsilon_{semi} / W_{dsj} \quad \text{where} \quad A_{ds} = A - A_{gd}$$

$$W_{gdj} = \sqrt{\frac{2\varepsilon_{semi}(V_{dg} + V_{Td})}{qN_b}}$$

$$C_{gdj} = A_{gd}\varepsilon_{semi} / W_{gdj}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for } V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd} C_{gdj} / \left(C_{oxd} + C_{gdj} \right) & V_{ds} > V_{gs} - V_{Td} \end{cases}$$

$$C_{gi} = \begin{cases} C_{oxd} & \text{for } V_{gs} \le V_{Tdi} \\ C_{oxd} \left(\frac{V_{gs} - V_{Tdiedge}}{V_{Tdi} - V_{Tdiedge}} \right) & V_{gs} < V_{Tdiedge} \,\&\, V_{gs} > V_{Tdi} \end{cases}$$

$$V_{Tdi} = V_{Td} - V_{bigd} - \frac{F_{xjbm} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b (V_{bigd} + V_{ds})}$$

$$V_{Tdiedge} = V_{Td} - V_{bigd} - \frac{F_{xjbe} A_{gd}}{C_{oxd}} \sqrt{2\varepsilon_{semi} q N_b (V_{bigd} + V_{ds})}$$

Table 2: Parameters, Extraction Programs, and Characteristics

Parameter symbol	Parameter name	Program name	Characteristic
A	Device active area		Chip size
V_T	Threshold voltage	SATMSR	Saturation current vs. V_{GS}
$K_P = K_{Psat}$	Saturation region transconductance		Saturation current vs. V_{GS}
θ	Transverse field transconductance factor		High saturation current vs. V_{GS}
K_{FL}	Low current transconductance factor		Low saturation current vs. V_{GS}
dV_{TL}	Low current threshold voltage differential		Low saturation current vs. V_{GS}
K_{Plin}	Linear region transconductance	LINMSR	On-state voltage vs. V_{GS}
R_S	Drain series resistance		On-state voltage vs. V_{GS}
N_B	Drift region dopant density		On-state voltage vs. V_{GS}
$R_{SPmos} = R_{SPchannel}$	MOSFET channel specific resistance		On-state voltage vs. V_{GS}
R_{SPepi}	Epitaxial-layer specific on-resistance		On-state voltage vs. V_{GS}
C_{GS}	Gate-source capacitance	CAPMSR	Gate charge
C_{OXD}	Gate-drain overlap oxide capacitance		Gate charge
A_{GD}	Gate-drain area		Gate-drain charge
V_{TD}	Gate-drain overlap depletion threshold		Gate-drain charge

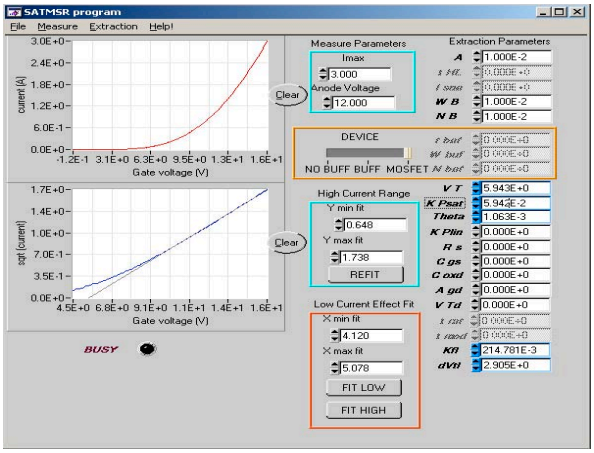

Fig. 2: SATMSR front panel demonstrating extraction of K_{Psat}, V_T, K_{FL} and dV_{TL}.

To perform the extraction, the MOSFET saturation current (I_{mos}^{sat}) is measured as a function of V_{GS} (upper graph in Fig.2), and the resulting square root of I_{mos}^{sat} versus V_{GS} (lower graph in Fig.2) is used to extract the model parameters. The square root of I_{mos}^{sat} is a linear function of V_{GS} as shown in (1).

$$\sqrt{I_{mos}^{sat}} = \sqrt{\frac{K_{Psat}}{2}}(V_{GS} - V_T) \qquad (1)$$

The program extracts K_{Psat} and V_T by linear interpolation of (1) and the resulting K_{Psat} and V_T are displayed on the user interface parameter value list. The user can then extract the high-current parameter (θ) and refine the extracted value of K_{Psat} using the "Refine K_{Psat} and θ" button in the extraction pull-down menu. Next, the "FIT LOW" and "FIT HIGH" buttons are used to extract K_{FL} and dV_{TL}. These buttons perform a least-squares fit to the saturation region's low- and high-current equations (I_{mosl} and I_{mosh}) shown in Table 1.

Table 3 gives the parameters extracted from the SATMSR program for the Silicon and SiC power MOSFETs with different blocking voltages (BV_{DS}) and continuous current rating (I_M). For Silicon power devices, the transconductance density (K_P/A) is generally chosen to decrease with increasing BV_{DS} so that it minimizes device on-state voltage without unnecessarily increasing the short circuit saturation current. The K_P/A = 3 for the 10 kV device type C is in the optimal range for this trade-off, although 2 kV SiC MOSFETs could benefit from an increased K_P. The temperature coefficient K_{P1} is negative for Silicon due to decreasing mobility and positive for SiC due to decreasing interface charge with increasing temperature.

To prevent channel leakage current for V_{GS} = 0, the value of V_T - dV_{TL} must be greater than zero for the device temperature range. The value of V_T - dV_{TL} has been improved for the HPE Phase 2 devices [9] resulting in low leakage up to 200 C.

B. Linear Region Parameter Extraction (LINMSR)

Fig.3 shows the front panel of the LINMSR extraction program. In this program, on-state voltage versus V_{GS} for a constant current is used to extract K_{Plin}, K_{Plin1}, R_S, N_B, R_{SPmos}, and R_{SPepi}. The values of K_{Plin}, K_{Plin1}, R_S, and N_B parameters are calculated from the model equations (Table 1) that are valid for the linear region, in which the values of the parameters extracted from the SATMSR program are used as known values in the equations.

The value of $R_{SP\_channel}$ is the product of A and Vds/Imos, which can be derived by using:

$$I_{mos} = \frac{K_{Plin}(V_{GS} - V_T)V_{ds}}{1 + \theta(V_{GS} - V_T)} \qquad (2)$$

The value of R_{SPepi} can be extracted using a subtraction or extrapolation method. The extrapolation method uses:

$$R_{SPepi} = (R_b + R_S)A \qquad (3)$$

where R_S is the extracted value and the epitaxial layer resistance (R_b) is calculated from the On-State Equations section in Table 1 using the extracted parameters. On the other hand, the subtraction method uses:

$$R_{SPepi} = R_{SP\_Total} - R_{SP\_Channel} \qquad (4)$$

where the extracted value R_{SP_Total} is obtained from the slope of the lower curve of Fig.3.

Table 4 gives parameters extracted from the LINMSR program. The R_{SPepi} increases rapidly with voltage blocking requirement BV_{DS}, but is generally much lower for SiC than for Silicon. The value of K_{Plin} is generally a

Table 3: Saturation Region Parameters Extracted from SATMSR Program.

	BV_{DS}, I_M	A (cm^2)	V_T (V)	K_P (A/V^2)	dV_{TL} (V)	K_{FL} (A/V^2)	V_{T1} (V)	K_{P1}
Si MOSFETS								
IRF1010	**55V, 85A**	**0.250**	**3.286**	**15.08**	**0.470**	**0.132**	**-0.006**	**-1.618**
IRF710	**400V, 2A**	**0.040**	**3.853**	**0.903**	**0.669**	**0.122**	**-0.005**	**-1.210**
IRFBG20	**1kV, 1.4A**	**0.100**	**3.798**	**1.243**	**0.607**	**0.120**	**-0.007**	**-2.257**
SiC MOSFETS								
Medium Voltage	**2kV, 3A**	**0.028**	**6.243**	**0.059**	**2.693**	**0.195**	**-0.023**	**0.984**
HPE-Phase 1 Type A	**10kV, 1.5A**	**0.05**	**1.049**	**0.038**	**1.631**	**0.145**	**-0.013**	**1.357**
HPE-Phase 1 Type C	**10kV, 1.5A**	**0.05**	**2.411**	**0.142**	**1.097**	**0.179**	**-0.015**	**0.988**

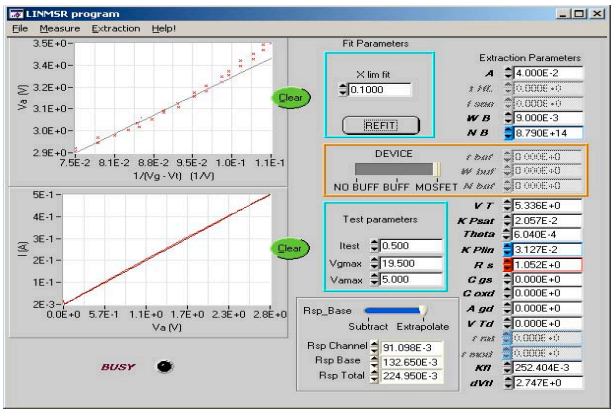

Fig. 3: LINMSR front panel demonstrating extraction of K_{Plin}, K_{Plin1}, N_B, R_S, $R_{SPchannel}$, and R_{SPepi}.

factor of two larger than K_P for low doped drain MOSFETs in both Silicon and SiC. The temperature coefficient of K_{Plin1} is positive for SiC similarly to K_{P1}. As discussed above, R_{SPmos} is chosen to be a small fraction of R_{SPepi} for Silicon and is currently determined by technology limitations for the 2 kV SiC MOSFETs.

C. Dynamic Parameters Extraction (CAPMSR)

The CAPMSR program measures gate and gate-drain charge characteristics for negative and positive gate voltages to extract C_{GS}, C_{OXD}, A_{GD}, and V_{TD}. Fig.4a shows the front panel for the CAPMSR program, Fig.4b shows the gate-charge curve calculated from the measured data, and Fig.4c shows the measured drain voltage dependence of gate-drain overlap threshold voltage.

1) Gate-Charge Capacitances: The gate capacitance extraction procedure uses the gate voltage waveform generated from a relatively constant gate current pulse as shown in the top graph in Fig.4a, where a high-valued drain resistance of approximately 10 k Ω is used for a 5 A device. To minimize noise, a 100 V pulse with a large gate resistor (in the range of 5 k Ω for a 5 A device) is used to produce the gate current pulse.

The "Calc" button in the blue box in Fig.4a is used to calculate the capacitance curve in the lower graph using:

$$C(V) = \frac{I}{dV / dt}. \qquad (5)$$

This curve is used to extract the values of C_{GS} and C_{OXD} by aligning the horizontal blue and green lines with the bottom and top plateau regions, respectively. Then, the user clicks on the "Cgs =" and "Cgs+Coxd" buttons to calculate the values of C_{GS} and C_{OXD}.

2) Gate-Drain Capacitances: To perform the gate-drain capacitance extraction, the user selects the "Plot V/Q" button in the green box of Fig.4a to integrate the data in the top curve of Fig.4a to obtain the gate charge curve in the pop-up window of Fig.4b. This is performed at different drain voltages (V_{dd}) to determine the drain voltage dependence of the gate charge curve.

The gate-charge sub-panel of Fig.4b has eight cursors that are aligned by the user to define the four intervals used to extract different model parameters. The user then clicks on the "Plot Extr" button to plot two linear extrapolation lines: (red) between the horizontal red and blue cursors and (green) between the horizontal green and black cursors. The intersection of the extrapolation lines indicates the intermediate value of V_{Tdi} and $V_{Tdiedge}$ shown in yellow. The user then clicks on the "Extract" button to accept the extrapolation lines and perform the extractions of Q_{gd}, C_{gs}, C_{oxd1}, C_{oxd2}, and V_T parameters.

The value of C_{gs} is extracted from the slope of the linear extrapolation line between the horizontal red and blue cursors of Fig. 4b. The values of C_{oxd1} and C_{oxd2} are extracted from the slope of the linear extrapolation lines between the horizontal green and black and the vertical green and black cursors, respectively. The value of V_T is extracted by averaging the gate voltage values within the gate-drain charge region (the interval between the vertical red and blue cursors).

To perform the extractions of V_{TD} and A_{GD}, the user needs at least two different values of V_{Tdi} obtained for different values of V_{dd}. Once there are at least two values of V_{Tdi}, the user can click on the "Extract Vtd" button in the green box of Fig.4a to display the V_{Tdi} versus the square root of V_{dd} + V_{bigd} as shown in Fig.4c. Each blue data point on the graph indicates one value of V_{Tdi} extracted from the previous steps at a particular value of V_{dd}. The red line represents the linear extrapolation line that is used to extract the values of V_{TD} and A_{GD} from the slope and intercept of the V_{tdi} equation in Table 1, where V_{dd}=V_{dds}.

Table 4: Linear Region Parameters Extracted from LINMSR Program.

	BV_{DS}, I_M	A (cm^2)	R_{SPepi} ($m.\Omega.cm^2$)	$R_{SPchannel}$ ($m.\Omega.cm^2$)	K_{Plin} (A/V^2)	K_{Plin1}
Si MOSFETS						
IRF1010	**55V, 85A**	**0.250**	**1.462**	**0.571**	**31.06**	**-1.57**
IRF710	**400V, 2A**	**0.040**	**97.94**	**8.028**	**1.009**	**-2.27**
IRFBG20	**1kV, 1.4A**	**0.100**	**769.5**	**13.52**	**1.384**	**-3.02**
SiC MOSFETS						
Medium Voltage	**2kV, 3A**	**0.028**	**4.305**	**16.19**	**0.125**	**0.943**
HPE-Phase 1 Type A	**10kV, 1.5A**	**0.05**	**121.2**	**26.84**	**0.082**	**1.66**
HPE-Phase 1 Type C	**10kV, 1.5A**	**0.05**	**105.8**	**12.61**	**0.232**	**1.68**

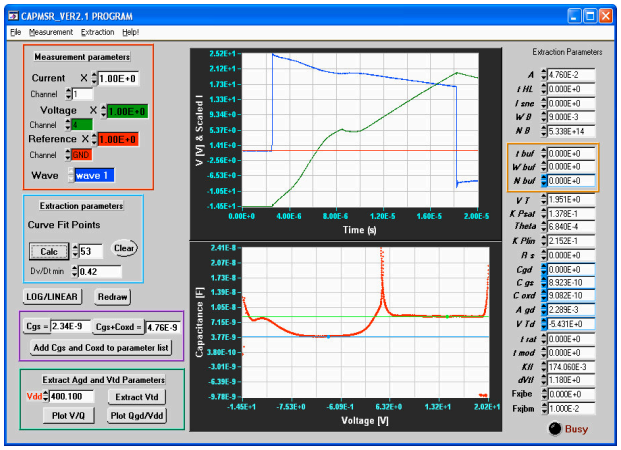

Fig. 4a: CAPMSR front panel demonstrating the extraction of C_{GS}, C_{OXD}, A_{GD}, and V_{TD}.

Fig. 4b: Voltage vs. charge plot sub-panel demonstrating the extraction of C_{GS}, C_{OXD}, V_T, and V_{Tdi}.

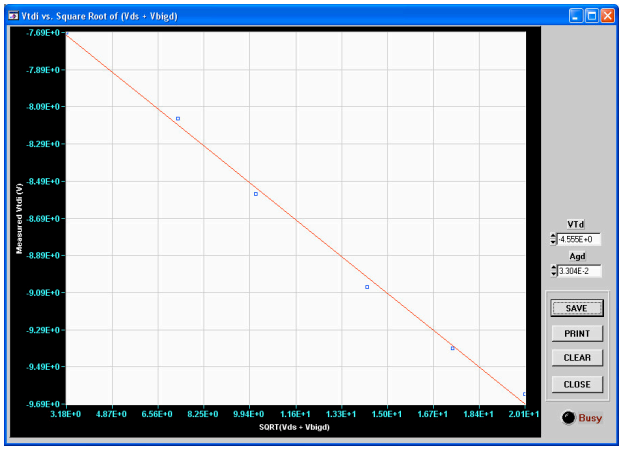

Fig.4c: Vtdi vs. square root of Vds+Vbigd sub-panel demonstrating the extraction of V_{TD} and A_{GD}.

3) High-voltage drain depletion capacitance: For a given blocking voltage requirement, SiC devices have a higher blocking layer dopant density than Silicon devices and thus have a higher output capacitance. Therefore, a new output (MOSFET drain) depletion capacitance extraction procedure has been added to the CAPMSR program. This procedure uses a capacitance meter with high voltage (up to 5 kV) applied to the MOSFET drain terminal where the high voltage is isolated from the capacitance meter. An additional power supply is used to bias the gate-to-source voltage.

The High Voltage (HV) drain depletion capacitance measurement circuit is shown in Fig.5a. There are five critical components in the circuit including the SiC Device Under Test (DUT), the gate and drain biasing isolating resistors (R_G and R_D) and the gate and drain coupling capacitors (C_G and C_D). The time constants R_GC_G and R_DC_D determine the gate and drain delay of the circuit, respectively. A 600 V, 35 A diode-bridge with ability to withstand a high current capacitor discharge current pulse in the event of DUT failure is used to protect the terminals of the LCR Meter. The protection diodes are reverse biased in order to reduce their junction capacitance and minimize impact on the DUT capacitance measurement.

All of the power supplies and the LCR meter are interfaced with the computer using the IEEE 488 bus and controlled by the CAPMSR gate-drain capacitance (C_{GD}) measurement sub-panels shown in Figs.5b and 5c. The graph in Fig.5b is an example of a high voltage capacitance versus drain voltage curve. For the circuit of Fig.5a, the DUT C_{GD} terminal capacitance is given by:

$$C_{GD}(V_{DS}) = \frac{C_G C_D C_{MSR}}{C_G C_D - (C_G + C_D) C_{MSR}} \qquad (6)$$

where C_{MSR} is the value measured from the LCR Meter. Both of the coupling capacitors, C_G and C_D, are equal to 0.1 uF and the resistors R_G and R_D are equal to 3 MΩ for the measurement in Figs.5b.

To perform the HV drain depletion capacitance measurements, the user first needs to set up the attributes by selecting the "Attributes" option on the menu bar of Fig.5b which opens the sub-panel shown in Fig.5c. From this sub-panel, the user can set up the LCR small signal parameters and the gate step and/or drain voltage sweep values. Additional delay parameters are included to enable the coupling capacitors to be charged after changing the bias voltages.

4) CAPMSR Extraction Results: Table 5 gives the parameters extracted from the CAPMSR program. The value A_{GD}/A is similar for all of the devices (except for the 55-V Silicon MOSFET that is made with a trench gate design) and represents the fraction of the high voltage drain depletion capacitance that is coupled to the gate. The oxide capacitances (C_{GS} and C_{OXD}) per unit area are several times larger for the SiC devices than for the mature silicon devices. As a result, the SiC devices have relatively higher gate drive current requirements.

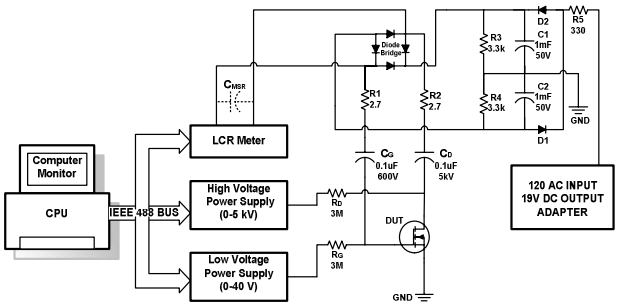

Fig. 5a: Circuit diagram for the high voltage drain depletion capacitance measurement.

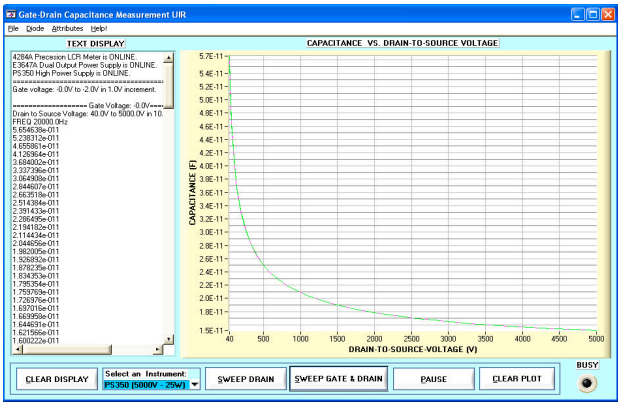

Fig.5b: HV drain depletion capacitance measurement front-panel.

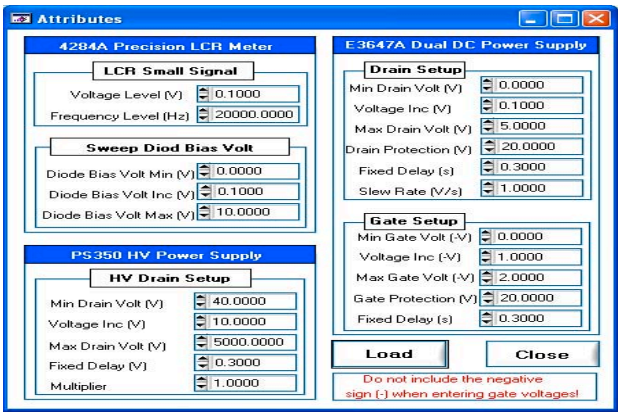

Fig.5c: HV drain depletion capacitance measurement sub-panel.

III. Conclusion

New SiC--IMPACT extraction tools have been presented for SiC power MOSFETs. The SiC--IMPACT parameter extraction sequence is demonstrated using several 10 kV SiC power MOSFET device design types and the results are compared with results for 2-kV SiC power MOSFETs and with commercial Silicon power MOSFETs with voltage blocking capabilities of 55 V, 400 V, and 1 kV. In addition, a high voltage drain depletion capacitance measurement circuit and graphical user interface have been developed and interfaced with the CAPMSR program to enable measurement of capacitances for drain voltages up to 5 kV.

References

[1] A. Hefner, R, Singh, and J.S. Lai, "Emerging Silicon-Carbide Power Devices Enable Revolutionary Changes in High Voltage Power Conversion," IEEE Power Electronics Society NEWSLETTER, Fourth Quarter 2004, pp. 10-12.

[2] S. Beerman-Curtin, et al., "Development of SiC high power electronics for naval aircraft carriers," in *30th GOMACTech Conf.*, pp. 218-221, Las Vegas, NV, April 2005.

[3] Defense Advanced Research Projects Agency (DARPA), Microelectronic Technology Office (MTO), Wide Bandgap Semiconductor Technology High Power Electronics Program (WBG-HPE): http://www.darpa.mil/mto/solicitations/ BAA # 06-30.

[4] T. McNutt, A. Hefner Jr., A. Mantooth, J. Duliere, D. Berning, and R. Singh, "Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator," IEEE Trans. Power Electronics, Vol. 19, No. 3, pp. 573-581, May 2004.

[5] T. McNutt, A. Hefner, A. Mantooth, J. Duliere, D. Berning, S-H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," Conf. Rec. of IEEE Power Electronics Specialists Conf. (PESC), pp. 217-226, (2003).

[6] A. Hefner and S. Bouché, "Automated Parameter Extraction Software for Advanced IGBT Modeling, "*Proceedings of The 7th Workshop on Computers in Power Electronics* (COMPEL), Blacksburg, VA, July 2000.

[7] S-H. Ryu, S. Krishnaswami, M .O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. Hefner, "10 kV, 123 mΩ-cm2 4H-SiC Power DMOSFETs," IEEE Electron Dev. Lett., Vol. 25, No. 8, p. 556.

[8] A. Hefner, "A Dynamic Electro-Thermal Model for IGBT," in IEEE Transactions on Industry Applications, vol.30, no. 2, (1994).

[9] A. Hefner, S-H Ryu, B. Hull, D. Berning, C. Hood, J.M. Ortiz-Rodríguez, A. Rivera-Lopez, T. Duong, A. Akuffo, and M. Hernandez-Mora, "Recent advances in high-voltage, high-frequency silicon-carbide power devices," to appear in Recs. 41st IEEE Ind. Apps. Conf., Tampa, FL, October 2006.

Table 5: Dynamic Parameters Extracted from CAPMSR Program.

	BV_{DS}, I_M	A (cm^2)	A_{GD} (cm^2)	C_{GS} (nF)	C_{OXD} (nF)	V_{TD} (V)
Si MOSFETS						
IRF1010	**55V, 85A**	**0.250**	**0.250**	**2.11**	**3.55**	**-1.08**
IRF710	**400V, 2A**	**0.040**	**0.015**	**0.174**	**0.268**	**-4.57**
IRFBG20	**1kV, 1.4A**	**0.100**	**0.019**	**0.462**	**1.037**	**-5.69**
SiC MOSFETS						
Medium Voltage	**2kV, 3A**	**0.028**	**0.002**	**0.544**	**0.450**	**-3.56**
HPE-Phase 1 Type A	**10kV, 1.5A**	**0.05**	**0.010**	**0.878**	**0.657**	**-5.86**
HPE-Phase 1 Type C	**10kV, 1.5A**	**0.05**	**0.010**	**0.978**	**0.769**	**-6.36**