Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Devices*

Allen Hefner[1], Sei-Hyung Ryu[2], Brett Hull[2], David Berning[1], Colleen Hood[1], Jose M. Ortiz-Rodriguez[1], Angel Rivera-Lopez[1], Tam Duong[1], Adwoa Akuffo[1], and Madelaine Hernandez-Mora[1]

[1]National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899
[2]Cree Inc., Durham, NC 27703

***Abstract*—The emergence of High-Voltage, High-Frequency (HV-HF) Silicon-Carbide (SiC) power devices is expected to revolutionize commercial and military power distribution and conversion systems. The DARPA Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is spearheading the development of HV-HF SiC power semiconductor technology. In this paper, some of the recent advances in development of HV-HF devices by the HPE program are presented and the circuit performance enabled by these devices is discussed.**

I. INTRODUCTION

Recent breakthroughs in Silicon-Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize commercial and military power distribution and conversion by extending the use of switch-mode power conversion to high voltage applications.

Currently, there are significant efforts underway to accelerate the development and application insertion of the new HV-HF SiC devices. The goal of the ongoing Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is to develop 10 kV, 100 A, 20 kHz class power semiconductor devices to enable future electric ships, more electric aircraft, and all electric combat vehicles [1,2,3]. DARPA is particularly interested in developing the power electronics device technology deemed necessary to enable 2.7 MVA Solid State Power Substations (SSPS) for future Navy warships.

The purpose of this paper is to describe some of the recent progress in devices being developed in Phase 2 of the DARPA HPE program. In reference [4], performance metrics and measurement equipment needed to evaluate HV-HF device and package performance were introduced. Currently, these device and package performance metrics developed at the National Institute of Standards and Technology (NIST) along with the wafer-level performance metrics developed at the Naval Research Laboratory (NRL) are being used to assess progress toward meeting the HPE Phase 2 goals.

* Contribution of the National Institute of Standards and Technology, not subject to copyright. The devices shown in this paper were produced by Cree Inc. under the DARPA WBST HPE Phase 2 program sponsored by Sharon Beermann-Curtin and monitored by Harry Dietrich.

II. SiC POWER DEVICE DEVELOPMENT

Wide bandgap semiconductors such as SiC have long been envisioned as the material of choice for next generation power devices [5]. Although wide bandgap semiconductor materials have superior properties, the realization of power device quality substrates and fabrication technologies required overcoming many technical challenges. The rapid advances in single crystal SiC over the last decade have ushered in a new era of wide bandgap power semiconductor devices. In 2002, Dr. Calvin Carter of Cree Inc. received the U.S. National Medal of Technology from President George W. Bush for: *"his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide bandgap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems."*

The primary advantage of the 4H-SiC material for power devices is that it has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and a higher temperature capability than conventional Silicon materials [6].

The higher breakdown electric field allows the design of SiC power devices with thinner (0.1 times that of Silicon devices) and more highly doped (more than 10 times higher) voltage-blocking layers. For majority carrier power devices such as power Schottky diodes or MOSFETs, the combination of 0.1 times the blocking layer thickness with 10 times the doping concentration can yield a SiC device with a factor of 100 advantage in on-resistance compared to that of Silicon majority carrier devices.

For minority carrier conductivity modulated devices such as PiN diodes or IGBTs, the blocking layer of 0.1 times the thickness of a Silicon device can result in a factor of 100 faster switching speed. This is possible because the diffusion length, L, required to modulate the conductivity of the blocking layer can also be reduced to 1/10th the value required for Si, thus permitting the reduction of the lifetime, τ, by a factor of 100 according to $L = \sqrt{D\,\tau}$, where D is the diffusion coefficient.

Because the SiC material provides a much lower on-resistance than Silicon, conductivity modulated Silicon devices can also be replaced by majority carrier SiC devices with faster switching speed [7]. For example, new SiC Schottky diode commercial products have recently been introduced [8, 9] to replace slower conductivity modulated Silicon PiN diodes. Although these first commercial SiC power device product offerings have been low voltage (300 V to 1200 V) Schottky diodes, the HV-HF devices discussed in this paper exceed the Silicon voltage capability limit and are expected to be a key enabling technology in the future.

III. HV-HF Power Conversion Applications

Over the last two decades, switch-mode power conversion technology, with its superior efficiency and control capability, has changed the way power is converted in almost all low and medium voltage power conversion applications from 100 V to 6.6 kV. Due to fundamental limitations of Silicon devices, the on-resistance increases and switching speed decreases as the blocking voltage requirement is increased. The switching speeds in low voltage power supplies are as high as several MHz and decrease to several kHz for high power traction. The higher on-resistance and slower switching speed increase loss and limits applicability of switch-mode power conversion for high power and electrical power utility applications.

The developments of Silicon IGBTs over the 1990s have enabled high-frequency power conversion to be used at increasingly higher power levels. The recently introduced SiC power Schottky diode commercial products have also increased switching frequency by reducing diode reverse recovery loss. It is expected that SiC power devices will continue to aid the evolution of switch-mode power conversion to higher frequency and higher power levels in the power supply and motor control areas as SiC Schottky diode and MOSFET products with higher voltage and current ratings are introduced.

Because SiC devices have the potential to increase the voltage beyond that of Silicon into the 10 kV through 25 kV range with much higher switching speed for a given blocking voltage, they provide the potential to extend high frequency switch-mode power conversion into the important application area of electrical power utility transmission and distribution. This new area is referred to as HV-HF power conversion [10].

Recent Electric Power Research Institute (EPRI) reports (1001698, 1002159 – see [11] for EPRI abstracts) concluded that a solid-state distribution transformer, referred to as the Intelligent Universal Transformer (IUT), would add significant new functional capabilities and power quality enhancements to those available from conventional copper and iron transformers. The IUT is expected to be a cornerstone device in advanced distribution automation (ADA). A more recent EPRI report (1009516) identified SiC power devices as the solution for the HV-HF semiconductor devices needed for the IUT and estimated that HV-HF power conversion could represent a relatively large segment of the power semiconductor market.

DARPA recently announced the WBST HPE Phase 3 program to perform innovative research in the area of high-voltage, high-frequency switch-mode power conversion [12]. The goals and benefits of this research are described in the DARPA Broad Area Announcement (BAA-06-30) as follows:

"In November of 2004, a Memorandum of Agreement was signed by the Navy and DARPA to develop a silicon carbide-based, high frequency, SSPS for future Naval Aircraft Carriers. The electrical distribution system being designed for the next generation of Aircraft Carriers employs 13.8 kV AC power distribution that is stepped down to 4,160 V AC or 465 V AC by using large (5,500 kg and 10 m^3) 2.75 MVA 60 Hz conventional transformers. The desired advanced power electronic system under this effort will demonstrate a silicon carbide based SSPS that converts the distributed 13.8 kV AC power down to 465 V AC at the same total power level (2.75 MVA) as the current system.

The component level benefit of using a high frequency solid state transformer over the conventional transformer is a significant reduction of weight and volume. System benefits of the high frequency, solid state topology include, but are not limited to, voltage regulation, over-current protection, power factor correction, improved power quality, frequency regulation and frequency changing, overload and surge protection, and potential removal of circuit breakers, which currently add weight and take up space, allowing the system to sag during power faults."

As an example of the need for HV-HF semiconductors, Fig. 1 shows a three level [13] solid state transformer indicating various secondary output options (EPRI report 1001698). The transformer consists of, from left to right, a high voltage active front end (AFE) rectifier stage, a three level dc link, a high voltage inverter, a high-voltage high-frequency transformer, low voltage rectifiers, and various output modules such as a DC/DC converter, 400 Hz AC inverter, and various voltage level 60 Hz AC inverter outputs. The AFE rectifier stage provides a flexible electrical utility interface with power factor correction. The high voltage inverter provides high frequency AC required to reduce transformer size and provides power quality voltage regulation functions. Both the AFE rectifier and high voltage inverter require HV-HF semiconductors.

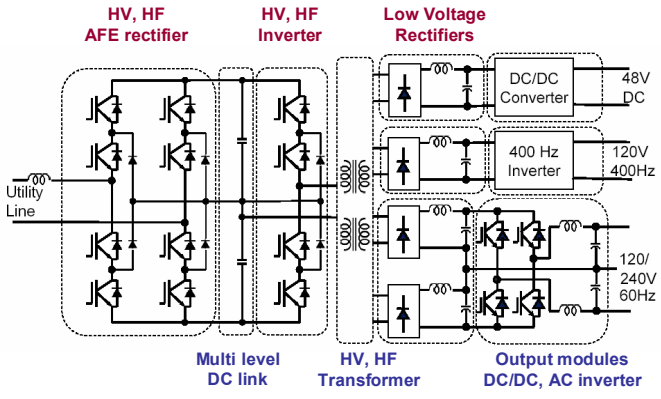


Fig. 1. Example of three-level, single-phase, solid-state transformer schematic.

IV. RECENT HV-HF SIC DEVICE DEVELOPMENTS

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. The DARPA HPE Phase 1 program completed in 2004 developed the underlying material and fabrication technology necessary for HV-HF SiC devices. The HPE Phase 2 program is currently developing the device and package technology necessary for the SSPS system in Phase 3.

Table 1 lists the basic semiconductor device goals for the HPE Phase 2 program as stated in the Phase 2 BAA. The devices being developed include diodes, switching devices, and half bridge modules. The diode requirements include 10 kV, 45 A single-die PiN diodes or equivalent Junction Barrier Schottky (JBS) or Merged PiN Schottky (MPS) diodes. The switching device requirements include a 10 kV, 18 A single-die MOSFET or equivalent IGBT for higher blocking voltages. The half-bridge module goals require paralleling the single-die diode and switch devices to produce voltage isolated modules with currents in the range of 110 A. This device and package technology is expected to be operated up to 20 kHz and 200 ºC.

Table 1. DARPA WBST HPE Phase 2 Device Goals

	PiN Diode (single die)	**MOSFET** (single die)	*IGBT (single die)*	**Half-Bridge Module**
BV (V)	**10 kV**	**10 kV**	*15 kV*	**10 – 15 kV**
I_{ON} (A)	**45 A**	**18 A**	*25 A*	**110 A**
T_J (°C)	**200 °C**	**200 °C**	*200 °C*	**200 °C**
f_{SW} (Hz)	**20 kHz**	**20 kHz**	*20 kHz*	**20 kHz**

The following subsections describe some of the progress that had been made midway through Phase 2 in development of 10 kV SiC MOSFETs and PiN diodes and in eliminating the forward bias degradation that has been observed in the past for minority carrier type devices such as PiN diodes, BJTs, GTOs, and IGBTs.

A. 10 KV SIC MOSFET

Substantial progress has been made thus far in HPE Phase 2 in demonstrating 10 kV SiC MOSFET characteristics that are generally suitable for 20 kHz hard switching applications such as the SSPS [14,15]. Major achievements include lower internal gate resistance leading to faster switching, higher transconductance leading to lower on-state voltage and lower gate voltage requirements, and higher threshold voltages resulting in the channel being fully off at Vgs = 0 V for temperatures up to 200 ºC.

MOSFET Static Characteristics: Table 2 summarizes some of the key parameters that influence the static performance of the SiC power MOSFETs. These parameters are extracted using the IGBT Model Parameter Extraction tools (IMPACT) described in [16,17,18]. The rows labeled HPE-1A and HPE-1C are two types of MOSFETs from HPE Phase 1 and the row labeled HPE-2 is for typical 10 kV MOSFETs from the first half of HPE Phase 2.

Table 2. MOSFET Static Performance parameters

	I_{ON} (A)	A (cm^2)	K_P (A/V^2)	K_P/A ($A/V^2/cm^2$)	K_{P1}	V_T (V)	dV_{TL} (V)	V_{T1} (mV/°C)
HPE-1A	**1.0**	**0.048**	**0.038**	**0.8**	**1.36**	**1.0**	**1.6**	**-13**
HPE-1C	**1.5**	**0.048**	**0.142**	**3.0**	**0.99**	**2.4**	**1.1**	**-15**
HPE-2	**5**	**0.15**	**0.323**	**2.1**	**0.99**	**4.5**	**1.6**	**-11**

The column in Table 2 labeled I_{ON} has the values for the continuous current rating determined as described below and the column labeled A has the values for the active area. The next three columns in Table 2 have the values for the transconductance parameter (K_P), the transconductance per unit area (K_P/A), and the negative temperature exponent of transconductance (K_{P1}). The final three columns have the values for the MOSFET channel threshold voltage (V_T), the voltage width of the threshold region (dV_{TL}), and the threshold voltage temperature coefficient (V_{T1}).

In general, the threshold voltage and transconductance parameters influence the continuous and pulsed current capability as well as the channel leakage current at high temperatures. The value of K_P/A is a figure of merit that must be high enough to obtain the required maximum pulsed current density determined by:

$$I_{Peak} = \frac{K_P}{2}(Vgs - V_T)^2 \qquad (1)$$

The pulsed current density capability is greater than 100 A/cm^2 for the Phase 2 devices at Vgs = 15 V and a temperature of 25 ºC, but is reduced substantially at higher temperatures. The leakage current at high temperatures is influenced by the low current threshold voltage temperature dependence:

$$V_{TL}(T) = V_T - dV_{TL} + V_{T1}(T - 25°C)\,. \qquad (2)$$

V_{TL} must be greater than zero for the full temperature range of operation to provide "normally off" behavior and prevent excessive channel leakage. For the Phase 2 devices, V_T has been increased to the point where the devices are "normally off" ($V_{TL} > 0$) for temperatures approaching 200 ºC.

Figure 2 shows the semi-log scale voltage blocking characteristics [19] of an early HPE Phase 2 MOSFET for different temperatures indicating that the MOSFET is fully off for all gate voltages less than 0 V and temperatures less than 175 ºC (i.e., leakage current is the same for all curves with Vgs ≤ 0). At each temperature the gate voltage is increased until the channel current increases the leakage current. For example, at 25 ºC, the channel is fully off for Vgs = 1 V but results in additional current through the MOSFET channel for Vgs = 2 V. Similarly, at 175 ºC the MOSFET channel is fully off for Vgs = 0 V but results in an increased current for Vgs = 1 V. Figure 3 shows similar forward blocking characteristics on both a linear

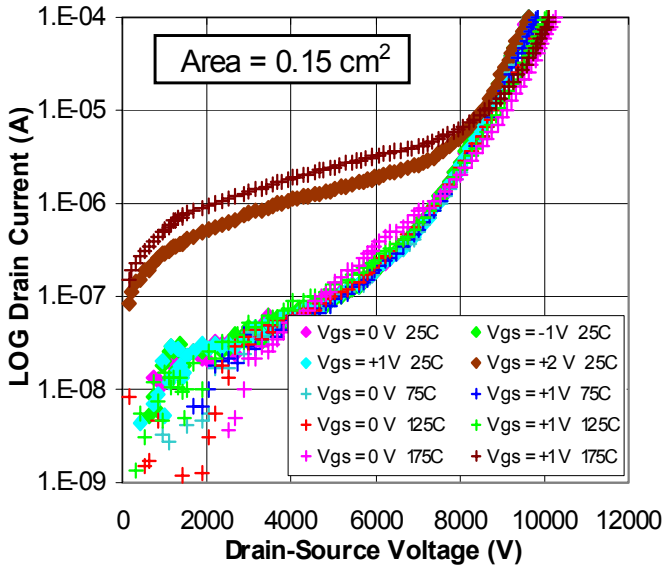


Fig. 2. Forward blocking characteristics of an early HPE Phase 2 MOSFET on semi-log scale at different temperatures and different gate voltages.

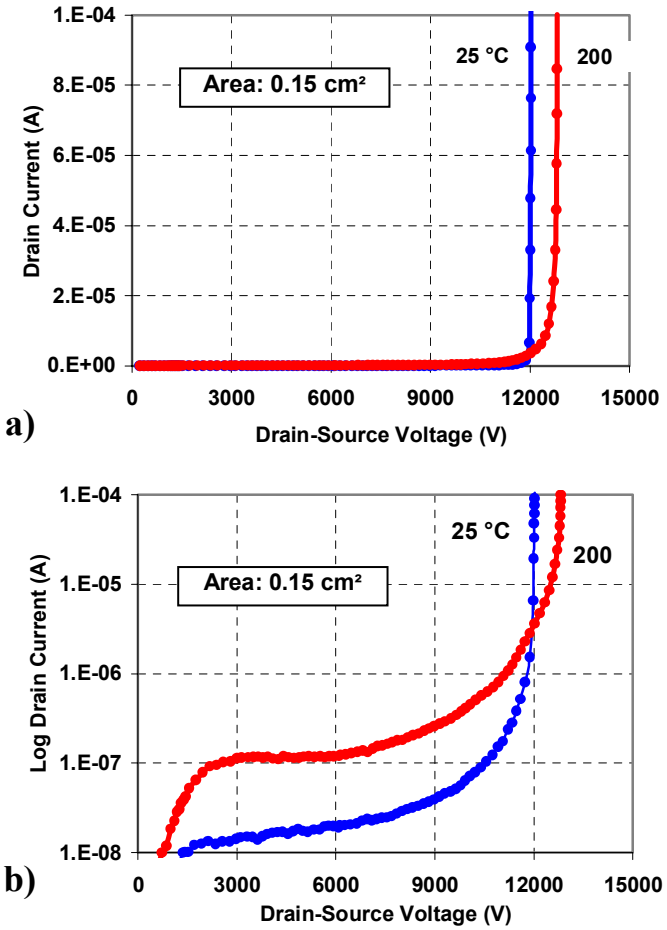


Fig. 3. Forward blocking characteristics of a mid-term HPE Phase 2 MOSFET at different temperatures and Vgs = 0 V on linear scale **(a)** and semi-log scale **(b)**.

and a semi-log scale for a mid-term HPE Phase 2 device with lower junction and channel leakage. For this device, the leakage current is below 1 μA for all drain voltages less than 11 kV, Vgs ≤ 0 V, and temperatures less than 200 ºC.

The MOSFET on-state voltage and continuous current capability are determined by the resistance of the voltage blocking layer and the resistance of the channel. Figure 4 shows the output characteristics at (a) 25 ºC and (b) 200 ºC for an HPE Phase 2 MOSFET with gate voltages from 0 V through 20 V in steps of 2 V. These figures indicate that the MOSFET is fully on at 8 A for gate voltages from 16 V to 20 V. Figure 5 shows the Vgs = 20 V curve (on-state characteristic) for temperatures from 25 ºC to 200 ºC in steps of 25 ºC indicating the 300 W/cm^2 power dissipation level. This indicates that the device can operate continuously at 4.5 A (30 A/cm^2) for the entire temperature range with less than 300 W/cm^2 heat removal requirement for the package. For the Phase 2 devices, the value of K_P/A is greater than 2 A/(V^2 cm^2) and the channel resistance at Vgs = 15 V is much less than the voltage blocking layer resistance. Hence, the devices approach the theoretical conduction capability of the SiC material. In the remainder of Phase 2, the area and current will be scaled to 18 A for single die and 110 A for the parallel die in the half-bridge module.

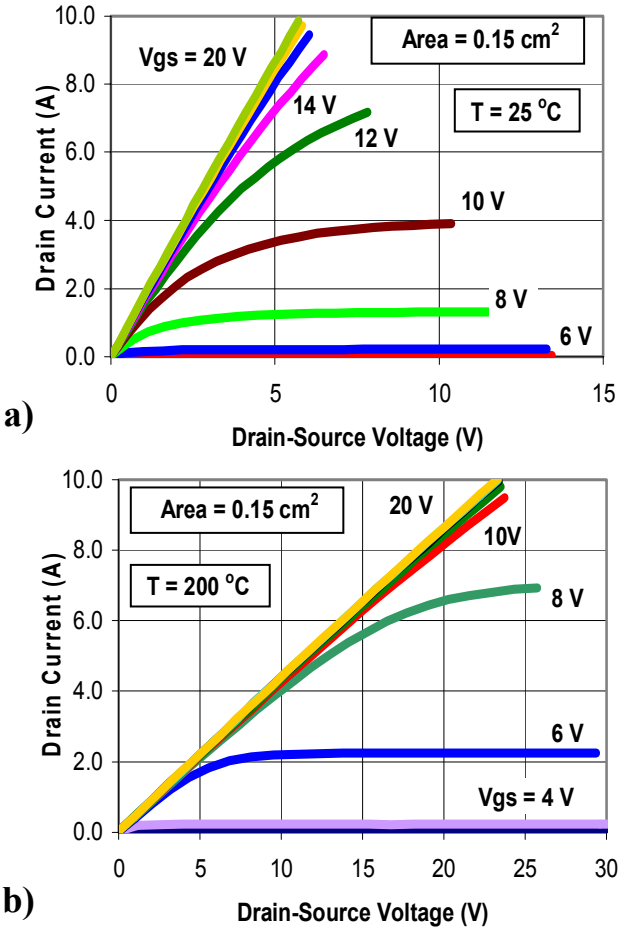


Fig. 4. Forward conduction characteristics of a 10-kV SiC MOSFET at **(a)** 25 °C and **(b)** 200 °C with gate voltages from 0 V to 20 V in 2 V steps.

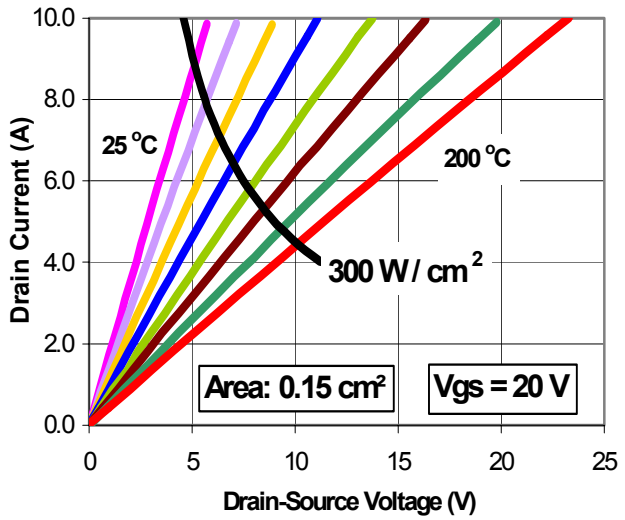


Fig. 5. On-state characteristics for Vgs = 20 V at temperatures from 25 °C to 200 °C in steps of 25 °C.

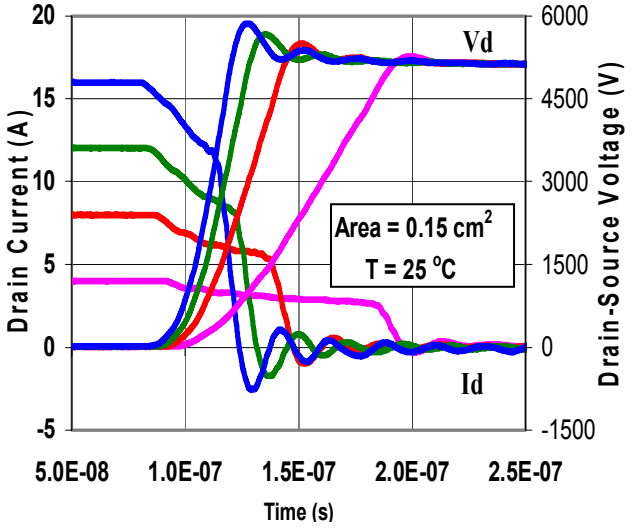


Fig. 6. Inductive load turn-off switching current and voltage waveforms for inductor currents of 4, 8, 12, and 16 A at 25 °C.

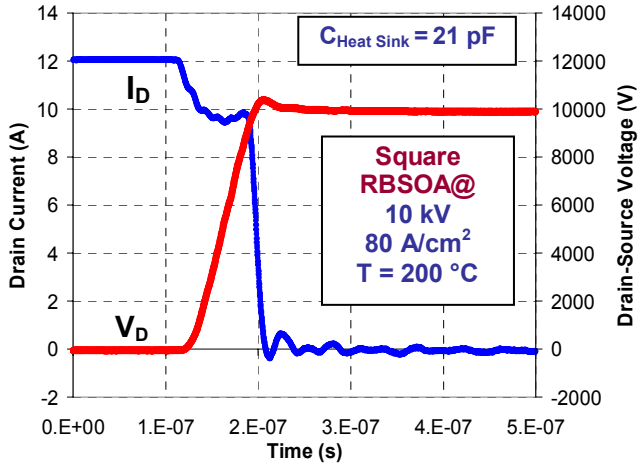


Fig. 7. RBSOA inductive load turn-off at 100 % blocking voltage and 2.7 times the continuous current rating at 200 °C.

MOSFET Dynamic Characteristics: Figure 6 shows clamped inductive load turn-off waveforms [19] for different load currents, a clamp voltage of 5 kV, and a gate resistance of 4 Ω. For the 4 Ω gate resistance, the drain voltage rise-time is determined by the load current charging the MOSFET output capacitance for drain currents less than 10 A but is influenced by the gate current charging the gate-drain Miller capacitance for larger drain currents. This extremely fast switching speed of 30 ns for the 16 A case and 80 ns for the 4 A case, is significantly faster than HPE Phase 1 devices that had a higher series gate resistance. Figure 7 shows the inductive load turn-off for a clamp voltage of 10 kV and drain current of 12 A (80 A/cm^2). This indicates a rugged device with a "square" Reverse Bias Safe Operating Area (RBSOA) of 100 % of the blocking voltage and 2.7 times the continuous current rating at 200 °C.

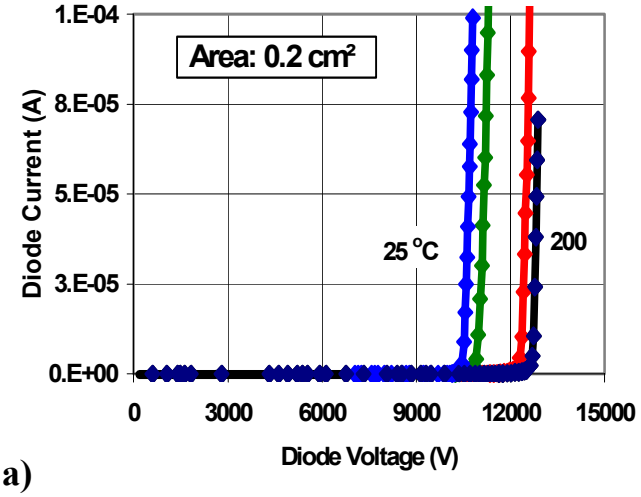
B. 10 KV SiC PiN Diode

Substantial progress has been made thus far in HPE Phase 2 in demonstrating PiN diodes with excellent breakdown voltage and leakage current characteristics, improved on-state voltage, and improved forward bias degradation performance [20]. Progress has also been made in increasing the speed of the PiN diode, although further improvement is required to enable 20 kHz hard switching at 200 °C.

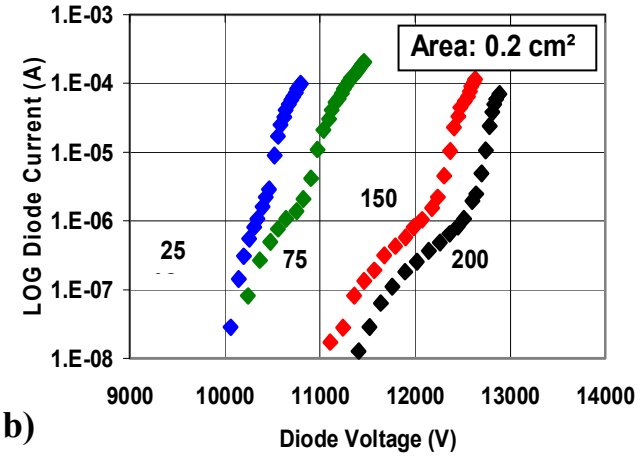
PiN Diode Static Characteristics: Figure 8 shows the reverse leakage current and breakdown characteristics [19] for a 0.2-cm^2 PiN diode produced in HPE Phase 2. The characteristics of Figure 8 demonstrate a sharp breakdown voltage above 12 kV (1 mA/cm^2) with extremely low leakage current below 10 kV (less than 10 nA) for all temperatures from 25 °C to 200 °C. The positive temperature coefficient of breakdown voltage suggests uniform avalanche multiplication across the chip. The individual voltage and current pulse waveforms (not shown) are also repeatable and do not have the sporadic oscillations and momentary faults seen in previous devices.

Figure 9 shows the forward conduction characteristics of a HPE Phase 2 PiN diode for temperatures from 25 °C to 200 °C indicating the 300 W/cm^2 power dissipation level. This indicates that the device can operate continuously at 20 A (100 A/cm^2) with a package capable of dissipating 300 W/cm^2. The device has a small negative temperature coefficient of –1.4 mV/°C at 20 A. This should provide reasonable ability to parallel multiple chips.

PiN Diode Reverse Recovery Characteristics: Figure 10 shows the temperature dependence of an HPE Phase 2 PiN diode reverse recovery switching waveform. Although the reverse recovery time is much faster than high voltage Silicon PiN diodes, further improvement is needed to enable 20 kHz hard switching at 200 °C. (A reverse recovery time of 50 to 100 ns is necessary to prevent excessive switching loss in the complementary MOSFET switch.) Figure 11 shows a comparison of the reverse recovery waveforms at 200 °C for two different PiN diode designs. The reverse recovery time is determined with a dI/dt that results in a peak reverse recovery current approximately equal to the forward current. The reverse recovery time has been improved from 500 ns for device (a) to 300 ns for device (b).



a)

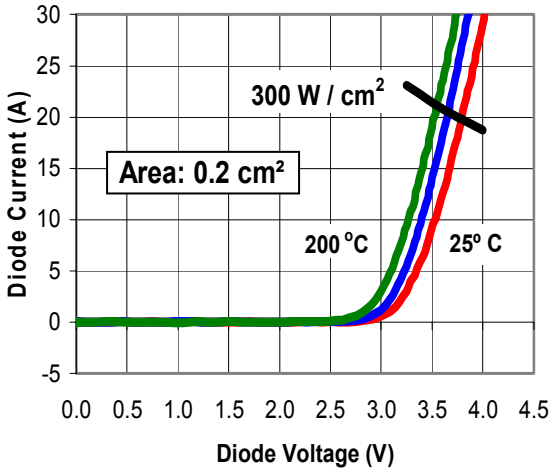


b)

Fig. 8. Reverse leakage current versus voltage for a SiC PiN diode at different temperatures **(a)** linear and **(b)** semi-log.

PiN Diode Forward Bias Degradation: A major concern with SiC PiN diodes in the past has been forward bias degradation. This is generally recognized to be due to stacking fault growth nucleated at defects originating in the starting wafer and from process induced defects [21,22,23]. These stacking faults reduce the device conduction area and degrade thermal performance [4,24]. Recently progress has been made in eliminating these nucleation sites resulting in devices that do not degrade after many hours of operation [25,26,27]. It is important to eliminate forward bias degradation to enable future PiN diode, BJT, IGBT, and GTO devices in SiC.

Figure 12 shows the forward voltage measured at 20 A for two HPE Phase 2 diodes (A and B) versus stress time where the stress is also performed at 20 A. The figure also numbers the points where current uniformity images are taken for each device. Device A only degrades by 0.1 V after 1000 hours of stress while device B degrades 0.5 V. Figures 13 and 14 show the current uniformity images for the two devices at the indicated degradation times on Fig. 12. The current uniformity images of degraded devices are generated using a custom high-speed thermal-imaging microscope system [28,4,29].



Fig, 9. Forward conduction characteristics of a 10-kV SiC PiN diode at 25 °C, 100 °C, and 200 °C.

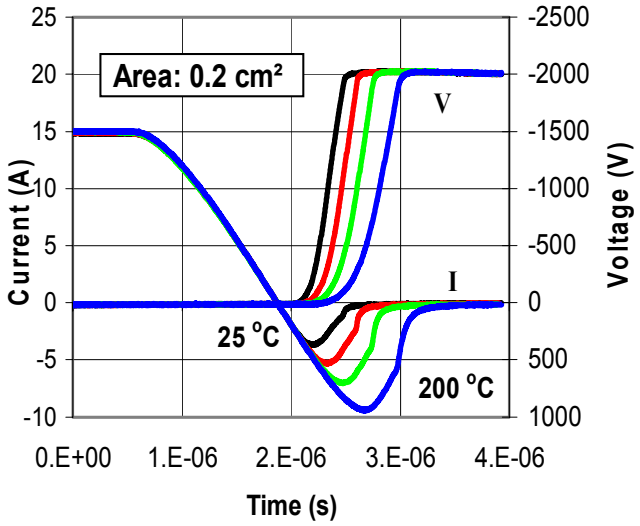


Fig. 10. Reverse recovery characteristics for a 10 kV SiC PiN diode at 25, 75, 125, and 200 °C.

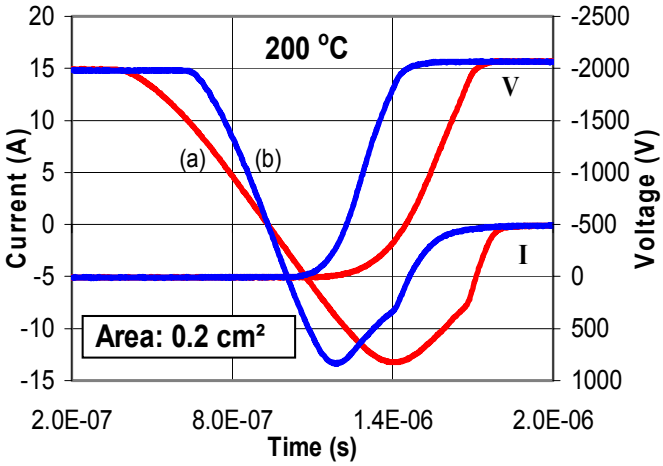


Fig. 11. Reverse recovery time for two different 10 kV SiC PiN diodes at 200 °C.

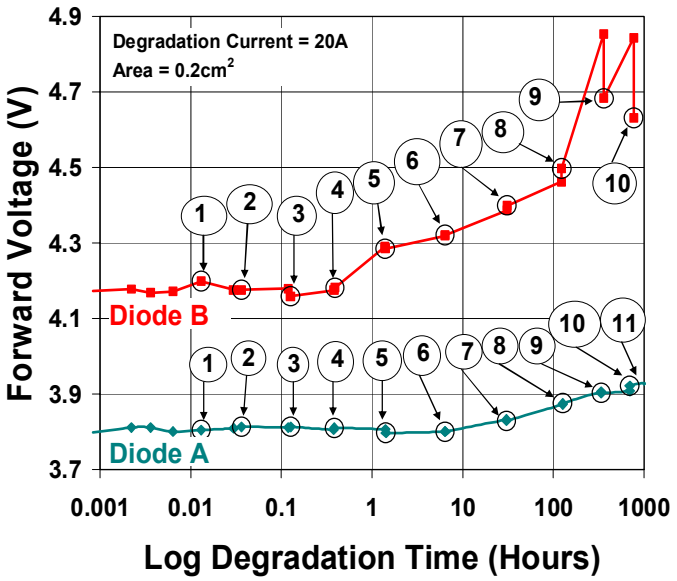


Fig.12. Forward voltage at 20 A versus log of degradation time for PiN diode A and B. The numbers indicate the points where current uniformity images are taken.

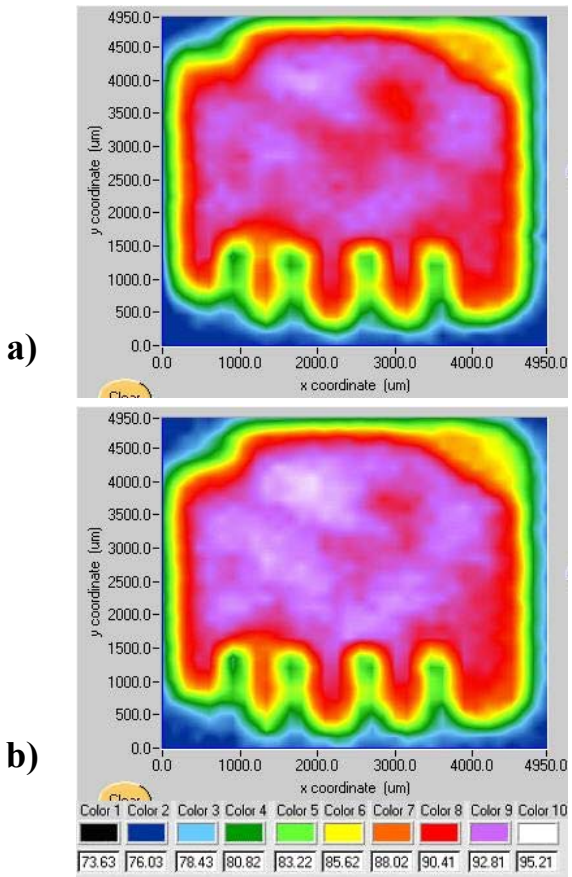


Fig. 13. Current uniformity image of PiN diode A **(a)** before forward bias stress (point 1 in Fig. 12) and **(b)** after 1000 hours of forward bias stress (point 11 in Fig. 12).

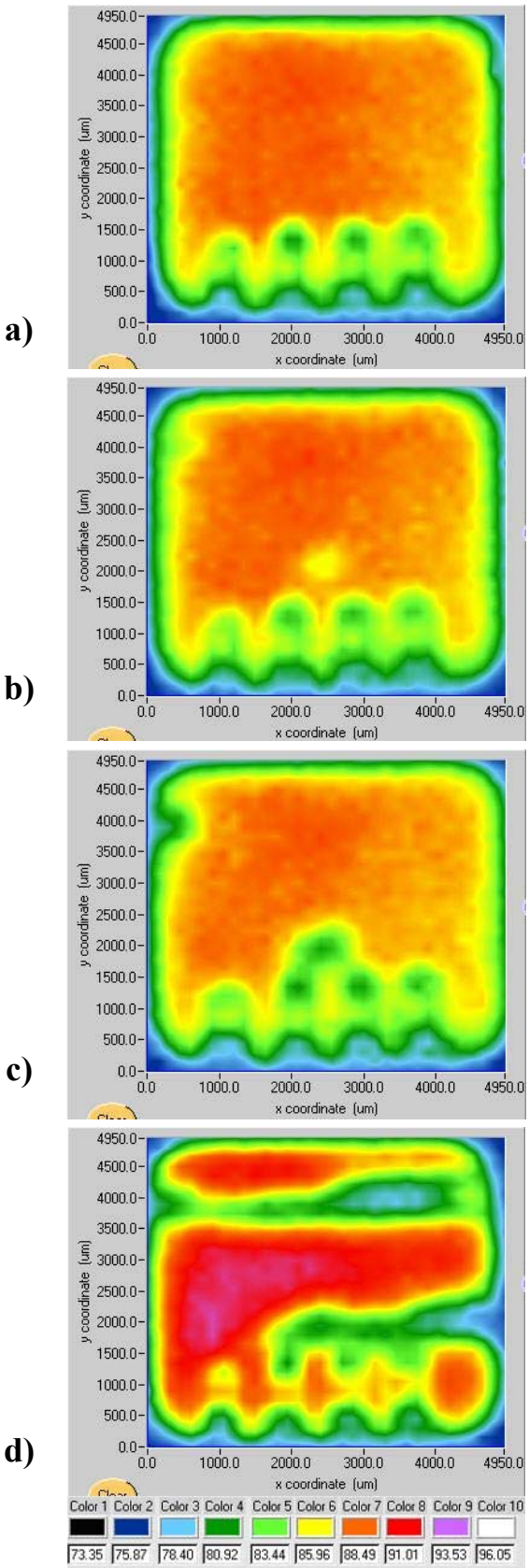


Fig. 14. Current uniformity image of PiN diode B before stress **(a)** point 1 in Fig. 12, and after stress **(b)** point 3 of Fig. 12, **(c)** point 4 of Fig. 12, and **(d)** point 5 of Fig. 12.

Device A in Fig. 13 shows no detectable current uniformity degradation after 1000 hours (the structure at the bottom of each figure is due to the wire bond shadows). On the other hand, device B in Fig. 14 has uniform conduction initially (a), but rapidly looses conduction area as the device is stressed (b-d). The current uniformity image of Fig. 14(b) has two obvious yellow spots that were not present in Fig. 14(a) at point (y=4000 um, x=700 um) and (y=2100 um, x=2400 um). These spots rapidly grow into larger regions with no current conduction. It should be noted that area reduction is evident before any degradation is detectable on the forward voltage curve of Fig. 12. Although the results indicate that the forward bias degradation problem still exists, there has been rapid improvement in the last two years increasing the reliable operation time by several orders of magnitude.

V. CONCLUSION

Although HPE Phase 2 is in the early stages, significant progress has been demonstrated in improved breakdown voltage and leakage current characteristics, lower on-state voltage, and higher switching speeds. Rugged SiC MOSFETS with a wide RBSOA have been demonstrated. Substantial improvements have also been made in overcoming device reliability concerns such as PiN diode forward bias voltage degradation and MOSFET gate leakage.

REFERENCES

[1] Sharon Beerman-Curtin, et. al., "Development of SiC High Power Electronics for Naval Aircraft Carriers," GOMACTech 2005, pp. 218-221.

[2] J.C. Zolper, "Emerging Silicon Carbide Power Electronics Components," IEEE Applied Power Electronics Conference Proceedings, March, 2005, pp. 11-17.

[3] Sharon Beerman-Curtin, et.al, "SiC: The Future of High Power Electronics," GOMACTech 2006, pp. 195-197.

[4] A.R. Hefner, "Metrology for High-Voltage, High-Speed Silicon Carbide Power Devices," GOMACTech 2005, pp. 226-229.

[5] K. Shenai, R. S. Scott, B. J. Baliga, "Optimum Semiconductors for High Power Electronics," *IEEE Transactions on Electron Devices*, vol. 36, no. 9, (1989), pp. 1811 – 1823.

[6] R. Singh, K. G. Irvine, D. Craig Capell, J. T. Richmond, D. W. Berning, A. R. Hefner, and J. W. Palmour, "Large Area, Ultra-high Voltage 4H-SiC p-i-n Rectifiers," IEEE Trans. on Electron Devices, vol. 49, no. 12, (2002), pp. 2308-2316.

[7] A. R. Hefner, R. Singh, J. S. Lai, D. W. Berning, S. Bouche, and C. Chapuy, "SiC Power Diodes Provide Breakthrough Performance for a Wide Range of Applications," in *IEEE Transactions on Power Electronics*, vol. 16, (2001), pp. 273 – 280.

[8] R. Singh, J. A. Cooper, M. R. Melloch, T. P. Chow, J. W. Palmour, "SiC Power Schottky and PiN Diodes," *IEEE Transactions on Electron Devices*, vol. 49, no. 4, (2002), pp. 665 –672.

[9] D. Stephani, "Status, prospects and commercialization of SiC power devices," *Proc. 59th Device Research Conference*, June 25-27 (2001), pp. 14.

[10] A. R. Hefner, R. Singh, and J.S. Lai, "Emerging Silicon-Carbide Power Devices Enable Revolutionary Changes in High Voltage Power Conversion," IEEE PELS Newsletter, Fourth Quarter 2004.

[11] Electric Power Research Institute (EPRI), 3412 Hillview Avenue, Palo Alto, California 94304, http://www.epri.com

[12] Defense Advanced Research Projects Agency (DARPA), Microelectronic Technology Office (MTO), Wide Bandgap Semiconductor Technology High Power Electronics Program (WBG-HPE): http://www.darpa.mil/mto/solicitations/ BAA # 06-30.

[13] J. Rodriguez, J-S. Lai, F. Z. Peng, "Multilevel Inverters – A survey of topologies, controls and applications," ***IEEE Transactions on Industrial Electronics***, vol. 49, no. 4, (2002), pp. 724 –738.

[14] S. Ryu, S. Krishnaswami, M .O'Loughlin, J. Richmond, A. Agarwal, J. Palmour, and A. R. Hefner, "10 kV, 123 mΩ-cm^2 4H-SiC Power DMOSFETs," *IEEE Electron Device Letters*, Vol. 25, No. 8, pp 556.

[15] S. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, "10 kV, 5 A 4H-SiC Power DMOSFET," Proceedings of the 18th International Symposium on Power Semiconductor Devices & IC's, (2006), pp. 265 – 268.

[16] A. Hefner and S. Bouché, "Automated Parameter Extraction Software for Advanced IGBT Modeling," Workshop on Computers in Power Electronics (COMPEL), (2000), pp. 10-18.

[17] T. H. Duong, A. R. Hefner, and D. W. Berning, "Automated Parameter Extraction Software For High-Voltage, High-Frequency SiC Power MOSFETs," to appear in Workshop on Computers in Power Electronics (COMPEL06), July 2006.

[18] T. McNutt, A. Hefner, A. Mantooth, D. Berning, S.H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," Conf. Rec. of IEEE Power Electronics Specialists Conf. (PESC), June 2003, pp. 217-226.

[19] D. Berning, A. Hefner, J. M. Ortiz-Rodriguez, C. Hood, and A. Rivera "Generalized Test Bed for High-Voltage, High-Power SiC Device Characterization," to appear in Conference Record IAS 2006.

[20] B. A. Hull, M. K. Das, J. T. Richmond, J. J. Sumakeris, R. Leonard, J. W. Palmour, and S. Leslie, "A 180 Amp/4.5 kV 4H-SiC PiN Diode for High Current Power Modules," Proceedings of the 18th International Symposium on Power Semiconductor Devices & IC's, (2006), pp. 277 – 280.

[21] J. Bergman, H. Lendenmann, P. Nilsson, U. Lindefelt, P. Skytt, "Crystal Defects as Source of Anomaluos Forward Voltage Increase of 4H-SiC Diodes," Mat. Science Forum, vols. 353-356, 2001. p. 299.

[22] A. Galeckas, L. Linnros, and P. Pirouz, "Recombination-Enhanced Extension of Stacking Faults in 4H-SiC p-i-n Diodes under Forward Bias," Applied Physics Letters, vol. 81, (2002), pp. 883-885.

[23] R. Stahlbush, et al., "Propagation of Current-Induced Stacking Faults and Forward Voltage Degradation in 4H-SiC PiN Diodes," Materials Science Forum, vols. 389-393, (2002), pp. 427-430.

[24] A.R. Hefner et. al. "Characterization of SiC PiN Diode Forward Bias Degradation," IAS 2004, pp.1252 - 1260.

[25] Mrinal K.Das, et. al., "Drift-Free, 50 A, 10 kV 4H-SiC PiN Diodes with Improved Device Yields," *ECSCRM 2004*.

[26] J.J. Sumakeris, et al, "Approaches to Stabilizing the Forward Voltage of Bipolar Devices," International Conference on Silicon Carbide and Related Materials (ICSRM), (2003).

[27] J.J. Sumakeris, et. al.,"Techniques for Minimizing the Basal Plane Dislocation Density in SiC Epilayers to Reduce Vf Drift in SiC Bipolar Power Devices," ICSRM 2005.

[28] A. Hefner, D. Berning, D. Blackburn, C. Chapuy, and S. Bouché "A High-Speed Thermal Imaging System for Semiconductor Device Analysis," in the conf. rec. IEEE Semiconductor Thermal Measurement and Management Symposium, (2001), pp. 43-49.

[29] A. Hefner, "Status of High-Voltage, High-Frequency Silicon-Carbide Power Devices," GOMACTech 2006, pp. 232-235.