NIST Sampling System for Accurate AC Waveform Parameter Measurements

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***Abstract*—This paper summarizes efforts at the National Institute of Standards and Technology (NIST) to develop a waveform sampling and digitizing system with accuracy comparable to that of an ac–dc thermal transfer standard for ac voltage measurements over the frequency range of 10 Hz to 1 MHz. In the frequency range from 1 kHz to 1 MHz, the sampler's gain flatness is better than that available from the best commercial digital multimeter. In ac–ac comparisons referenced to 1 kHz, the system agrees with a NIST-calibrated thermal transfer standard to within 17 μV/V from 20 Hz to 100 kHz for measurements made at both 1 and 0.1 V. The sampler's excellent dynamic linearity and flat input impedance are also discussed.**

***Index Terms*—Analog-to-digital conversion (ADC), frequency response, gain measurement, Markov processes, measurement standards, signal sampling.**

I. Introduction

IMPROVEMENTS in the determination of ac quantities at power frequencies using sampling and digitizing techniques have been reported in [1] and elsewhere. Toward this end, as well as for higher frequency applications, the National Institute of Standards and Technology (NIST) has recently improved its electronic voltage sampling and digitizing system [2] for accurate determination of ac quantities over the frequency range of 10 Hz to 1 MHz. The work described in this paper is motivated in part by the desire to verify ac–dc difference measurements with a method that is independent of thermal voltage converters. In addition, waveform parameters other than root mean square (rms) can be determined since the instrument produces a sampled data record of the measured signal with excellent dynamic linearity. In comparison with a NIST-calibrated commercial thermal transfer standard, ac–ac differences of the sampling system referenced to 1 kHz differ from ac–ac differences of the thermal standard by no more than 17 μV/V from 20 Hz to 100 kHz for measurements made at both 1 and 0.1 V.

This paper describes recent design improvements to the existing NIST Sampling Waveform Analyzer (SWA) system and presents selected ac parametric and measurement performance results.

II. NIST SWA

The NIST SWA consists of a mainframe unit, a remote sampling comparator probe, and software for data acquisition and processing. The measurement scheme is that of a 16-bit successive approximation analog-to-digital converter (ADC) that samples in equivalent time, i.e., the system samples below the Nyquist rate to measure repetitive waveforms—a process, hereafter, referred to as undersampling. Fig. 1 illustrates the arrangement. At least one commercially available instrument has used this technique, packaging the comparator and companion circuitry neatly in a pencil-type probe [3]. The NIST SWA improves upon the commercial instrument with a set of sampling probes [4], [5] that offer better gain flatness and a timebase having better linearity and lower jitter.

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A. Mainframe Unit

In the legacy SWA system, the mainframe unit comprises a precision digital-to-analog converter (DAC), a custom-designed timebase circuit, and a state machine logic all under the control of an embedded computer. The timebase is triggered either directly by the signal being measured or by a signal that is synchronous with the signal being measured to produce a sequence of strobe pulses occurring at progressively increasing delays after each trigger instant. A similar sampling instrument is described in [6], where timing is derived not from programmable delays but from locked frequency synthesizers with frequencies chosen to allow one frequency to undersample the other.

We have redesigned the SWA mainframe to consolidate the hardware, combining architectural aspects of both of these sampling systems. Like the system described in [6], the new SWA eschews a dedicated timebase circuit in favor of undersampling via locked synthesized timing signals. However, for measuring low-frequency signals, including signals at power frequencies, the system can switch from undersampling to sampling well above the Nyquist rate and thereby achieve a significant reduction in data acquisition time. In either sampling mode, the most significant bit (MSB) is sampled first for all sampling instants on the waveform. Then, the next MSB for each data point is sampled, and so on, down to the least significant bit (LSB). The new SWA also retains a key design feature of the old SWA, namely, an averaging feature based on Markov estimation [7]. This averaging mode is invoked following the successive approximation process and works by allowing noise at the sampler's input to increase or decrease the DAC reference value in accordance with the comparator decision at each sampling instant. The amount by which the DAC reference is increased or decreased is typically set equal to the LSB of the successive approximation process. By averaging the dithered reference values over L sampling instants, this sampling process achieves the same effective reduction in noise as would be achieved if L 16-bit data samples were collected.

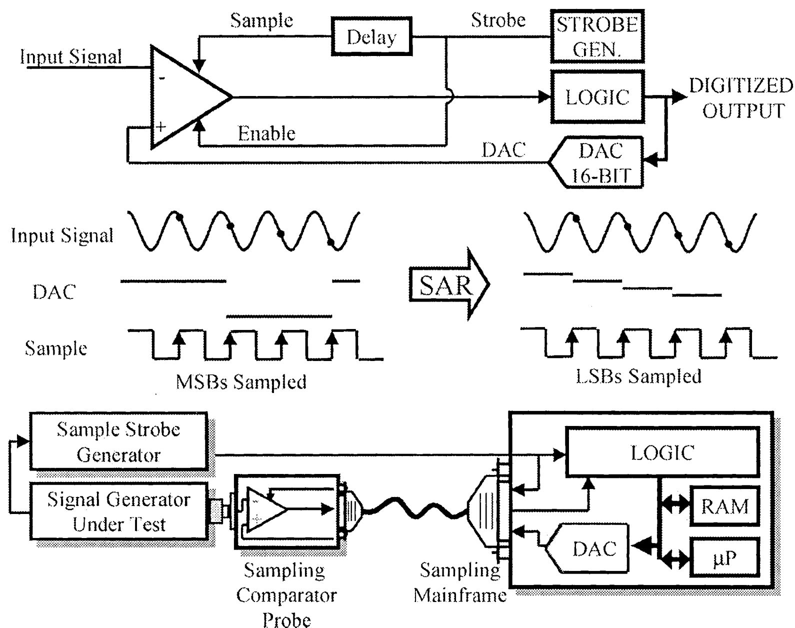

Fig. 1. (Top) Functional block diagram of sampling and digitizing instrument. (Middle) Equivalent time, successive approximation digitization. (Bottom) Equipment hookup showing comparator probe connecting to mainframe unit through umbilical harness.

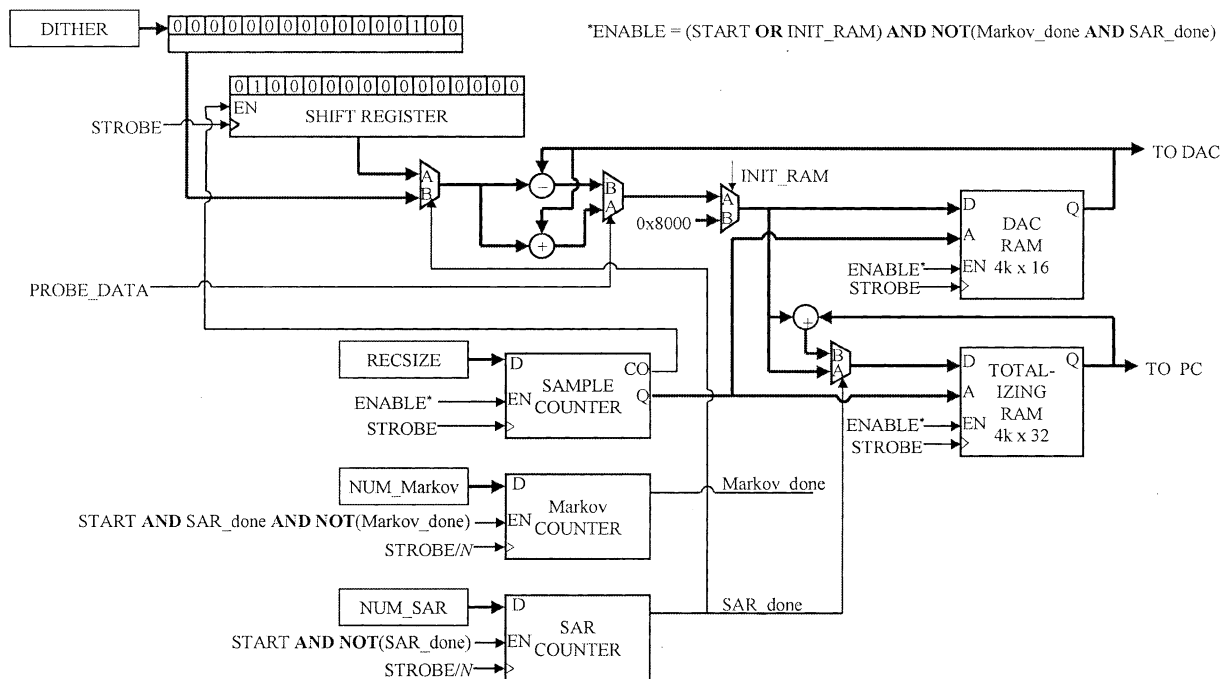

Fig. 2. Simplified block diagram of the system logic design. At each sampling instant, the probe data bit determines whether the current binary weight stored in the shift register (SAR mode) or dither value (Markov mode) is added or subtracted from the running value of the data sample. SAR results are stored in the DAC RAM. Markov averages are stored in the totalizing ram.

1) Description of the Circuit: The successive approximation digitization and Markov averaging algorithm has been written in a synthesizable hardware description language and programmed into a single programmable logic device (PLD) chip. Aside from isolation circuitry and a laptop–computer interface, the system has been reduced to two chips—the PLD and a precision 16-bit DAC.

Fig. 2 shows a block diagram of the logic design. Four parameters stored in on-chip registers govern the system operation. These parameters set the size of the data record to be acquired, the number of successive approximation steps to be taken, the number of Markov averages to be acquired, and the magnitude of the Markov dither. The sampling comparator strobe signal is the clock for the sample counter, successive

approximation register (SAR), and random access memories (RAMs). All logic operations occur synchronously with this strobe. The RAMs are capable of updating the current sample data and fetching the DAC value for the next sample on the same clock edge. The sample counter addresses the RAMs and enables the SAR. An externally derived clock whose frequency is f_s/N, where N is the data record size, clocks the SAR and Markov counters. The Markov mode begins when the SAR counter reaches its terminal count, and data acquisition ends when the Markov counter reaches its terminal count.

2) Sample Timing: As described in [6], a signal with frequency f_i can be coherently [8] undersampled when f_i and the sampling frequency f_s are defined by the relation

$$f_s = \frac{M}{M+1} f_i \tag{1}$$

where M is the number of samples to be taken in one period of the signal. With the signal and strobe frequencies so selected, M uniformly spaced phases of the input signal will be sampled over $M+1$ periods of the input signal.

Practical considerations limit the maximum real-time sample rate f_{smax} of the system. One constraint is the settling time requirement of the 16-bit DAC, which limits f_{smax} to approximately 200 kHz. However, a signal with frequency $f_i^{(n)}$, where

$$f_i^{(n)} = f_i + n f_s \tag{2}$$

and n is an integer greater than zero, will appear as an alias of f_i and produce the same samples as a signal with frequency f_i. Signals with frequencies higher than f_{smax} can therefore be sampled at a sample rate determined by combining (1) and (2) so that

$$f_s = \frac{M}{M(1+n)+1} f_i^{(n)} \tag{3}$$

where

$$n = \mathrm{int}\left(\frac{f_i^{(n)}}{f_{\mathrm{smax}}}\right) \tag{4}$$

and $\mathrm{int}(x)$ produces the integer part of x.

B. Sampling Probe

The sampling probe [4] forms the comparator portion of the SWA ADC. The comparator's simple track/latch circuit structure yields an inherently flat gain versus frequency response. In the frequency range from 1 kHz to 1 MHz, the sampler's flatness is better than that available from the best commercial digital multimeters.

By design, the probe exhibits a finite impulse response through the use of an enabling switch that keeps the comparator's front-end circuitry powered off (no bias) until 800 ns prior to sampling. While minimizing signal-induced thermal errors, the enabling feature also limits the probe's memory to the duration for which the comparator is energized before each sample is taken. The effect is illustrated in Fig. 3 in which the response to a step indicates a distinct knee at the enable time. Since this response is linear and time invariant and since the impulse response is essentially zero for all time after 800 ns, a step response measurement of the probe over a waveform epoch of 800 ns is sufficient to characterize fully the probe's frequency response from dc to an arbitrary maximum frequency of interest. With the best commercially available reference-step generators, uncertainty of 100 μV/V in the magnitude response at 1 MHz is achievable. Calibrating the probe in this manner provides a means to measure the rms value of an ac waveform accurately and independent of thermal converters.

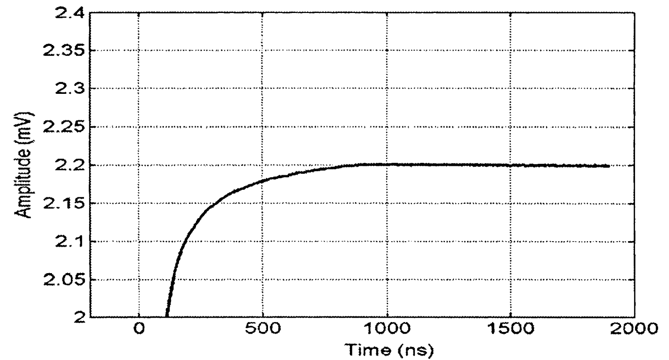

Fig. 3. Settled region of the sampling probe step response. The reference-step generator had a pulse amplitude of −0.5 V and a transition duration of approximately 15 ps.

III. Results

This section presents examples of the SWA's performance in terms of gain flatness, dynamic linearity, and input impedance flatness.

A. Comparison With a NIST-Calibrated Thermal Transfer Standard

Sampling probe gain flatness was measured against a commercial thermal transfer standard. Results of comparisons at 0.1 and 1 V are presented in Figs. 4 and 5. The frequencies selected were those for which the transfer standard had NIST calibration corrections available. The 0.1-V measurement was performed on the 0.22-V range of the transfer standard. The 1-V measurement was performed on the 2.2-V range of the transfer standard. The residual discrepancy between the SWA and the transfer standard, each with its own corrections applied, is on the order of the measurement uncertainty of 15 μV/V ($k = 2$) for the transfer standard.

B. Dynamic Linearity

An example of dynamic linearity performance of the system is illustrated in Fig. 6. To ensure adequate spectral purity of the test signal, an analog low-pass filter was used. The attenuation

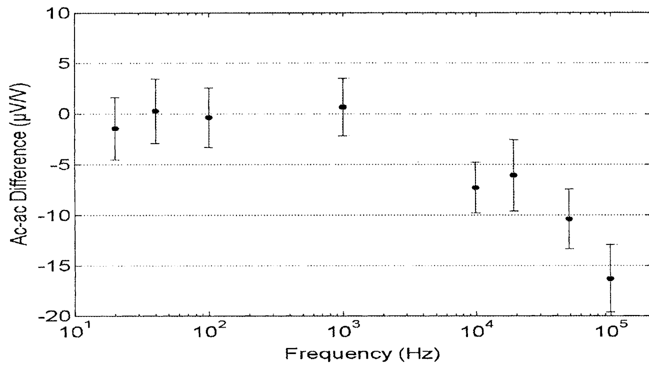

Fig. 4. AC–AC differences for the NIST sampling system measured against a commercial thermal transfer standard at 1 V. The reference frequency was 1 kHz. The uncertainty bars indicate ± 2 standard deviations of the mean of 20 repeated measurements at each frequency. The transfer standard uncertainty $(k = 2)$ is 15 μV/V.

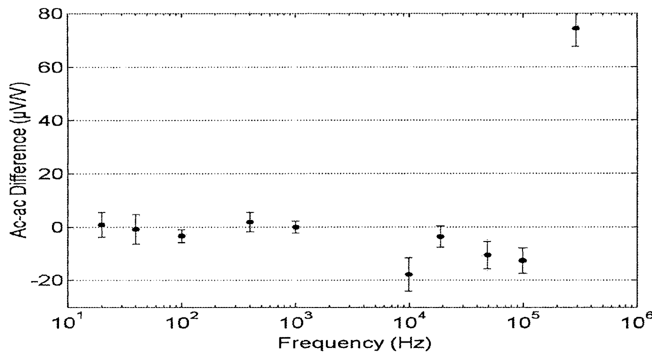

Fig. 5. AC–AC differences for the NIST sampling system measured against a commercial thermal transfer standard at 0.1 V. The reference frequency was 1 kHz. The uncertainty bars indicate ± 2 standard deviations of the mean of 20 repeated measurements at each frequency. The transfer standard uncertainty $(k = 2)$ is 15 μV/V.

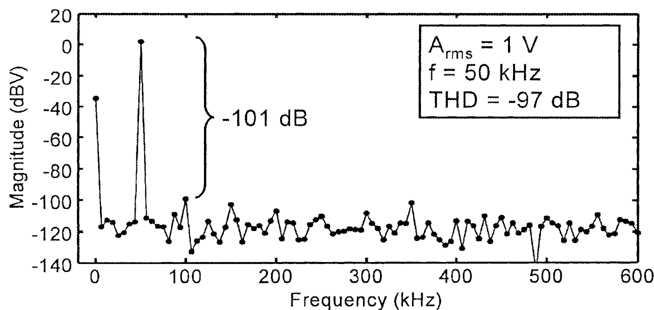

Fig. 6. Magnitude spectrum of sampled data for an input signal of 1 V at 50 kHz.

of the filter was -83 dB at 100 kHz. The specified harmonic and spurious signal levels of the signal generator were better than -60 dBc. The spectrum of a sampled data record for an input signal with a level of 1 V at 50 kHz is shown. The second harmonic power level is -101 dBc, and the total harmonic distortion is -97 dB.

C. Sampling Probe Input Impedance

The probe's input impedance was measured using a commercial LCR meter. The resistive part of the impedance based on a

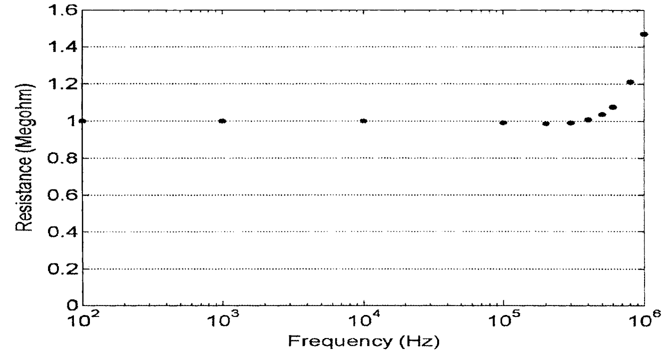

Fig. 7. Sampling probe input resistance. The applied measurement voltage was 100 mV. Parallel input capacitance was approximately 6 pF from 100 Hz to 1 MHz.

parallel RC model is plotted in Fig. 7. Over the frequency range of 100 Hz to 400 kHz, the input resistance is flat to within 1%. The input capacitance is approximately 6 pF.

IV. Additional Considerations

With an input impedance of 1 MΩ, the sampling probe is amenable to the use of a frequency-compensated resistive attenuator to allow operation at higher voltage levels. We have developed attenuators calibrated up to 100 V using a digital filtering process to achieve flatness within 20 μV/V from 100 Hz to 100 kHz.

Nonlinear error in the sampler has been investigated using phase-plane techniques [9]. An analytic error model that describes the sampler's nonlinear error behavior—harmonic distortion as well as zeroth-order (offset) and first-order (gain and phase) distortion—has been developed. The model is used to correct nonlinear error in the probe when signal amplitudes exceed 2 V.

V. Conclusion

A brief overview of a newly redesigned voltage waveform sampling system has been presented. The system offers a combination of excellent gain flatness, input impedance flatness, and dynamic linearity not achievable with any commercially available sampling instrument. For ac rms measurements, agreement with a NIST-calibrated thermal transfer standard is close to the measurement uncertainty of the transfer standard. Additional future plans for the sampling system are to support NIST measurement services for pulse settling parameters and harmonic power.

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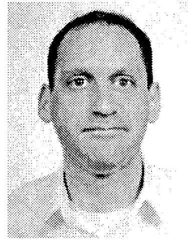

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