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10 kV, 5A 4H-SiC Power DMOSFET

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Abstract- **In this paper, we report 4H-SiC power DMOSFETs capable of blocking 10 kV. The devices were scaled up to 5 A, which is a factor of 25 increase in device area compared to the previously reported value. The devices utilized 100 μm thick n-type epilayers with a doping concentration of 6 x 10^{14} cm^{-3} for drift layers, and a floating guard ring based edge termination structure was used. The gate oxide layer was formed by thermal oxidation at 1175°C, followed by an NO anneal. A peak effective channel mobility of 13 cm^2/Vs was extracted from a test MOSFET with a W/L of 150 μm / 150 μm, built adjacent to the power DMOSFETs. A 4H-SiC DMOSFET with an active area of 0.15 cm^2 showed a specific on-resistance of 111 mΩ-cm^2 at room temperature with a gate bias of 15 V. The device shows a leakage current of 3.3 μA, which corresponds to a leakage current density of 11 μA-cm^{-2} at a drain bias of 10 kV.**

INTRODUCTION

High critical field in 4H-silicon carbide (4H-SiC) enables high voltage majority carrier devices with very low drift layer resistance (two orders of magnitude lower than that of a silicon device). Resulting devices can demonstrate low loss, high speed switching performances [1,2] because they do not depend on conductivity modulation for on-state conduction, which is the case with silicon devices with comparable blocking capabilities. This concept can be applied to extremely high voltage (≥10 kV) devices, with switching frequencies greater than 20 kHz, which is beyond the audible frequency range. Recently, a 10 kV, 123 mΩ-cm^2 4H-SiC DMOSFET was demonstrated [3]. However, the active area of the device was only 4.24x10^{-3} cm^2, and the device was capable of flowing a drain current of 200 mA, which is insufficient for any power applications. Efforts have been made to increase the current rating, and in this paper we present a 5A 4H-SiC DMOSFET with a blocking voltage of 10 kV.

DEVICE FABRICATION

A simplified cross-section of the 4H-SiC DMOSFET is shown in Fig. 1. A cell pitch of 14 μm was used. A 100 μm thick n-type drift epilayer with 8 x 10^{14} cm^{-3} doping concentration was grown on an n^+ 4H-SiC substrate with an 8° offcut angle. Heavy dose nitrogen implantations were performed to form n^+ source regions, and then the p-wells with retrograde profile were formed by aluminum

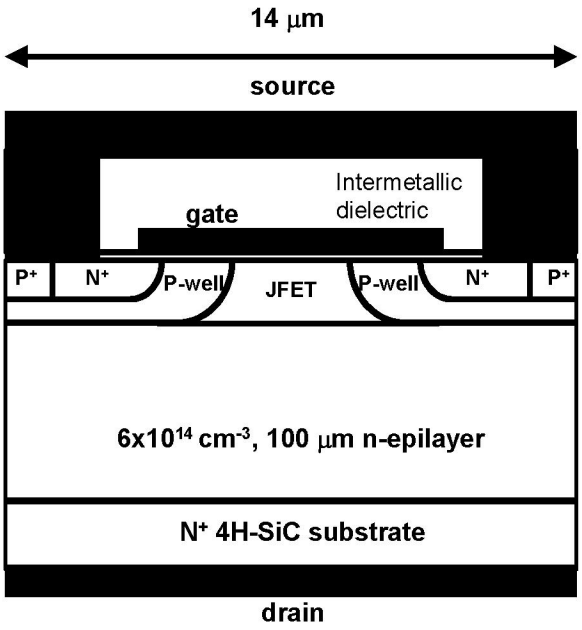


Fig. 1. Simplified cross-section of a 4H-SiC power DMOSFET cell.

implantation. The MOS channel length, which is defined by the distance between the edges of n^+ source regions and the p-wells, was 0.5 μm. Heavy dose aluminum implantations formed p^+ contacts to the p-wells as well as the floating guard ring based edge termination structure. 65 floating guard rings were used, and the total length of the edge termination structure was 550 μm. Then, the JFET regions, defined as the region between the adjacent p-wells, were implanted with nitrogen to a doping concentration of 5 x 10^{15} cm^{-3}. All the implants were activated at 1600 °C in silicon overpressure. A 0.7 μm thick PECVD oxide layer was then deposited and patterned as the field oxide. A 500 Å thick gate oxide layer was thermally grown at 1175°C in dry O_2, then nitrided at 1175°C in NO [4,5]. A degenerately doped polysilicon layer was deposited and patterned as gate electrode. The ohmic contacts to source, drain and p^+ regions were formed with alloyed Ni. An LPCVD oxide layer (0.7 μm thick) was then deposited as an inter-metallic dielectric layer, and via holes were opened. A 4 μm aluminum overlayer was deposited and patterned using a wet-etching technique to form electrodes. A layer of photosensitive polyimide was applied to the front surface as the final passivation, and a 1 μm thick Ti/TiW/Au

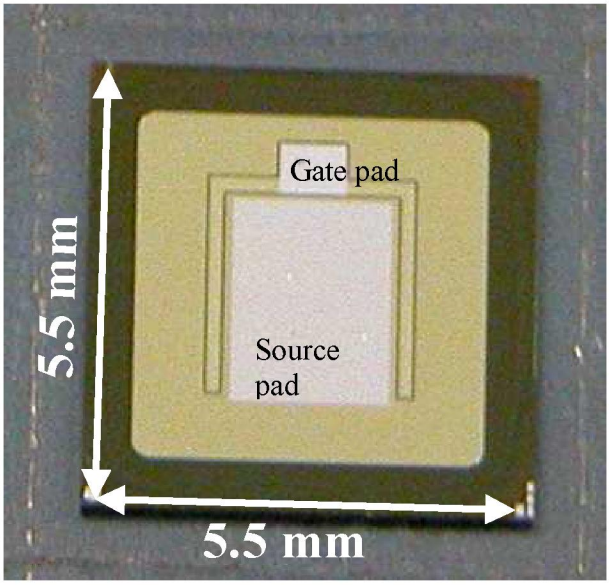


Fig. 2. Photograph of a 5.5 mm x 5.5 mm 4H-SiC DMOSFET. The active area is 0.1545 cm^2.

was deposited on the backside. A photograph of a 5.5 mm x 5.5 mm (active area = 0.1545 cm^2) 4H-SiC DMOSFET is shown in Fig. 2.

EXPERIMENTAL RESULTS

Figure 3 shows I_D vs. V_{GS} characteristics of the 4H-SiC DMOSFET. A drain bias (V_{DS}) of 50 mV was used. A threshold voltage of 3.5 V was extracted from the linear portion of the curve, and a subthreshold swing of 200 mV/dec was observed. It should be noted that even though the threshold voltage is 3.5 V, gate biases of less than 2.3 V was required to completely turn off the device (I_D < 1 μA). However, these devices are expected to be used in a very

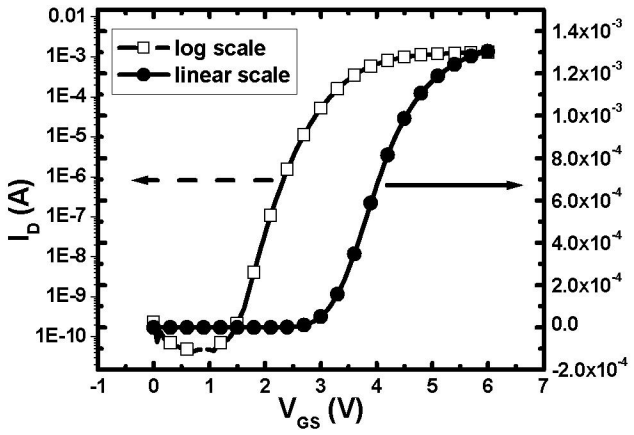


Fig. 3. I_D vs. V_{GS} measurements from the 4H-SiC DMOSFET. A V_{DS} of 50 mV was used.

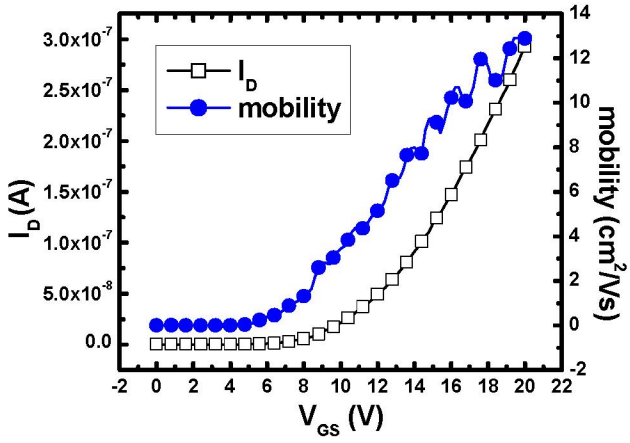


Fig. 4. I_D vs. V_{GS} measurements from a 150 μm / 150 μm test MOSFET on a p-well. A V_{DS} of 50 mV was used.

noisy environment (high voltage and high frequency switching applications). A greater noise margin is required to minimize the probability of erroneous turn-on's of the device, hence, a more positive threshold voltage is desired. A peak effective channel mobility (μ_{eff}) of 13 cm^2/Vs was measured from a test MOSFET with a W/L of 150 μm / 150 μm built on a p-well (see Fig. 4).

Figure 5 shows the room temperature on-state I-V characteristics of the 4H-SiC DMOSFET. The gate oxide field was limited to 3.0 MV/cm. With a V_{gs} of 15 V (E_{ox} = 3.0 MV/cm), a forward voltage drop of 3.76 V was measured at a drain current of 5 A, which corresponds to a current density of 32 A/cm^2. The specific on-resistance ($R_{on,sp}$), measured at a V_{DS} of 0.15 V, and a V_{GS} of 15 V, was approximately 111 mΩ-cm^2. An 11% reduction in $R_{on,sp}$ was achieved compared to previously reported value [3]. This is mainly due to the use of thinner drift epilayer (115 μm thick drift layer was used in

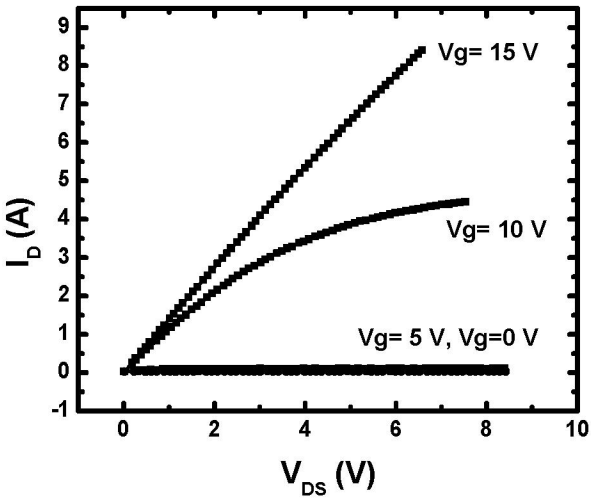


Fig. 5. Room temperature on-state IV characteristics of the 4H-SiC DMOSFET. The measurement was performed using Tektronix 371A curve tracer.

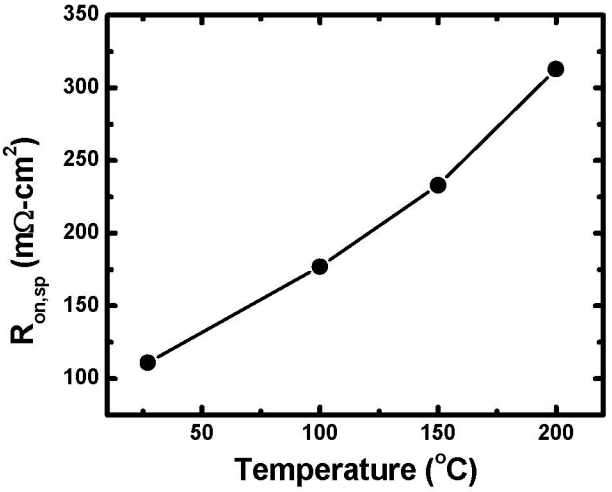


Fig. 6. Specific on-resistance of the 4H-SiC power DMOSFET as a function of temperature.

[3]), in addition to using shorter MOS channel length and tighter cell pitch structure. Fig. 6 shows the specific on-resistance of the device as a function of junction temperature. Drift layer resistance is the dominant on-resistance component for this device. The specific on-resistance increases with the temperature, and a specific on-resistance of 313 mΩ-cm^2 was measured at a junction temperature of 200 °C. This is due to decrease in bulk electron mobility at elevated temperatures, which increases JFET and drift resistances of the DMOSFET. Fig. 7 shows the off-state characteristics of the DMOSFET at room temperature. The device was immersed in Flourinert oil to prevent arcing in air during the measurement. The device was able to support a drain voltage of 10 kV with a leakage

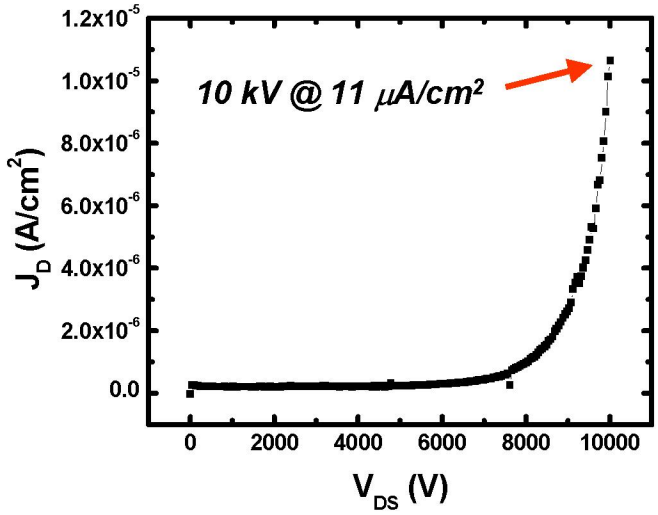


Fig. 7. Room temperature off-state IV characteristics of the 4H-SiC DMOSFET. Gate electrode was shorted to the Source electrode, and the sample was immersed in Flouinert during the measurement.

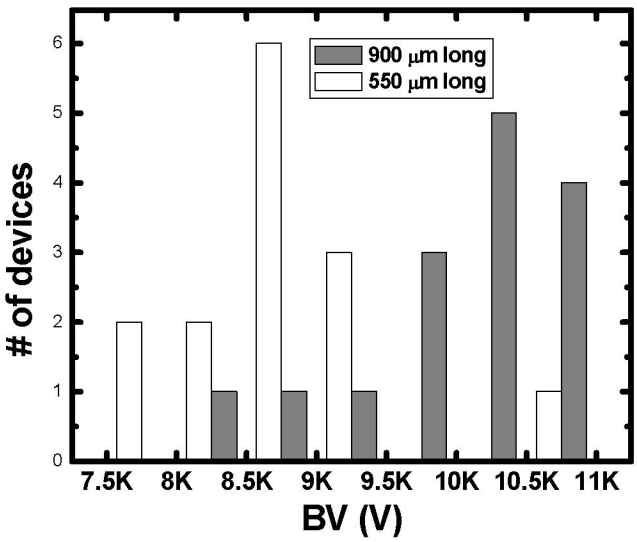
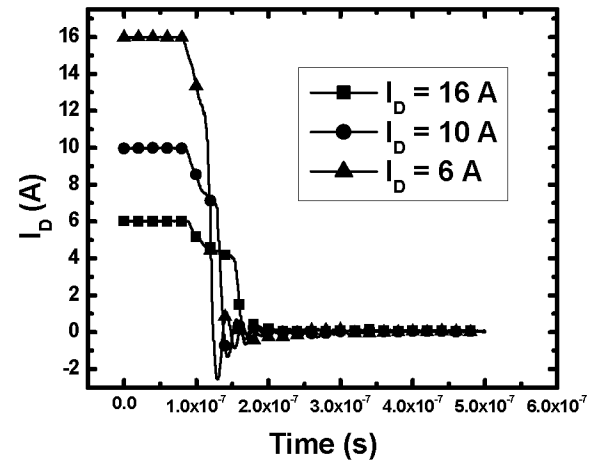


Fig. 8. Distribution of test diode blocking voltages. The diodes were built on 8x10^{14} cm^{-3} doped, 100 μm thick epi layer.

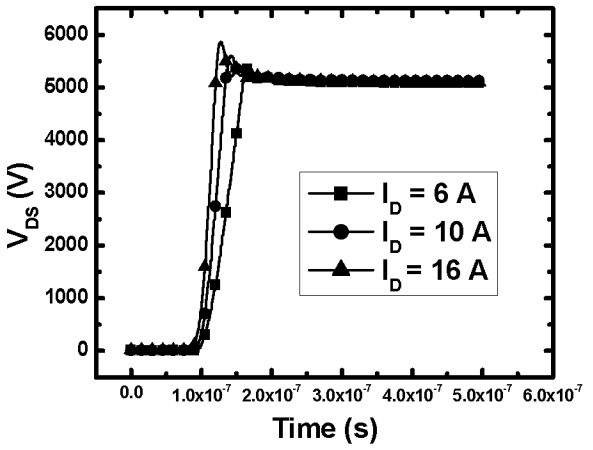
current of 3.3 μA, which corresponds to a leakage current density of 11 μA/cm^2 with gate electrode shorted to the source electrode. The theoretical parallel plate E-field calculated for this structure is 1.55 MV/cm. However, peak E-field within the device is much higher, especially at the edge of the device due to field crowding, caused by non-ideal edge termination structure.

Figure 8 shows the blocking voltage distribution of test PiN diodes built on a 100 μm thick, 8x10^{14} cm^{-3} doped n-type epilayer. Two termination structures were implemented. One is 550 μm long with 65 rings, and other is 900 μm long with 102 rings. The leakage current density was limited to 0.2 mA/cm^2. The distribution of blocking voltages of the diodes with 550 μm long termination had a peak at around 8.6kV. Calculated parallel plate peak E-field for this voltage is approximately 1.58 MV/cm. This value agrees well with the value calculated for the 10 kV DMOSFETs. It should be noticed that the blocking voltage distribution of the diodes with 900 μm long termination had a peak at around 10.3 kV, which corresponds to a theoretical parallel plate peak E-field of 1.73 MV/cm. This suggests that it is possible to fabricate 10 kV DMOSFETs on a higher doped (8x10^{14} cm^{-3}) drift epilayer, if a 900 μm long termination structure is implemented. This will result in approximately 30% reduction in drift resistance over the device presented in this paper.

Figure 9 shows the inductive load turn-off characteristics of the 4H-SiC DMOSFET. A supply voltage of 5 kV, a gate resistance of 4 Ω, and a clamp diode with 15 pF capacitance were used for the measurement. A V_{gs} of 20 V was used to turn-on the device, and a V_{gs} of 0 V was used to turn-off the device. The measurements were repeated with different drain currents, and Fig. 9 shows the results with I_D = 6 A, I_D = 10 A, and I_D = 16 A. The switching time, which includes the current fall time and the voltage rise time, was approximately 70 ns



(a)



(b)

Fig. 9. Inductive load switching characteristics of the 10 kV DMOSFET. 4 Ω gate resistor was used. (a) drain current, and (b) drain voltage wave forms

with an I_D of 6 A. The turn-off time decreases with increasing drain current, and a turn-off time of 40 ns was observed with an I_D of 16 A. The DMOSFET turn-on measurement was not performed due to lack of a fast turn-off diode at the time of measurement. The switching measurements indicate that this device can enable high frequency (> 20 kHz) switching applications provided that a diode with sufficient speed can be paired with the device.

SUMMARY

10 kV, 5 A 4H-SiC DMOSFETs have been presented. This result represents a factor of 25 increase in the current capability over the previously published result. A threshold voltage of 3.5 V and a specific on-resistance of 111 mΩ-cm^2 were measured. An effective channel mobility of 13 cm^2/Vs was measured from a test MOSFET built adjacent to the DMOSFET. An 11% reduction in specific on-resistance, compared to the previously reported value, was achieved by using a thinner drift layer. Significant increase in the specific on-resistance was observed at elevated temperature, and an $R_{on,sp}$ of 313 mΩ-cm^2 was measured at 200 °C. This is due to decrease in electron mobility with the temperature. The device was able to block 10 kV with a leakage current density of 11 μA/cm^2 with a V_{gs} of 0 V. It was experimentally shown that the drift layer resistance can be further reduced by improving the performance of the edge termination structure. Fast switching characteristics were demonstrated, and a switching time of 70 ns was measured when the device was flowing a drain current of 6 A. When paired with a diode with sufficient speed, the 4H-SiC DMOSFET can enable high speed (> 20 kHz), high voltage switching applications.

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