RF, Analog and Mixed Signal Technologies for Communication ICs - An ITRS Perspective

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Abstract — **The International Technology Roadmap for Semiconductor (ITRS) Radio Frequency and Analog/Mixed-Signal (RF and AMS) Wireless Technology Working Group (TWG) addresses device technologies for wireless communications covering both silicon and III-V compound semiconductors. In this paper, we discuss the roadmap and the figures of merit (FoM) used to characterize both active and passive devices critical for typical radio front end designs. We review the trends, challenges and potential solutions and address the intersection of silicon and III-V compound semiconductors.**

Introduction

RF and AMS technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Recognizing wireless applications as a new system driver, ITRS formed the RF and AMS Wireless TWG in 2003.

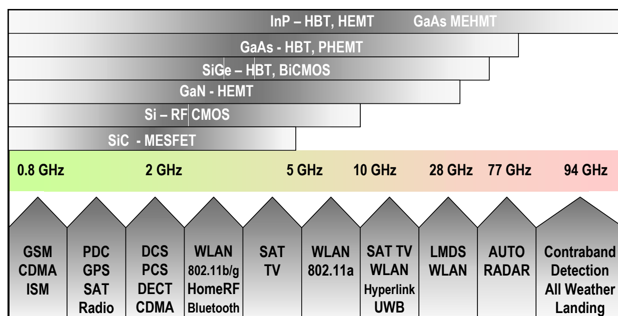

Fig. 1. Wireless communication application spectrum.

Figure 1 presents the interplay among commercial wireless communication applications, available spectrum, and the kinds of elemental and compound semiconductors likely to be used. The boundary between silicon and III-V semiconductors has been moving to higher frequencies with time. Today, Si and SiGe dominate below 10 GHz and III-V compound semiconductors dominate above 10 GHz products. In future years, it is expected that the frequency axis in Fig. 1 will lose its significance in defining the boundaries among technologies. Instead, the future boundaries will be dominated more by such parameters as noise figure, output power, power added efficiency, linearity and ultimately cost. Some of this is already true for power amplifier (PA) applications. The consumer portions of wireless communications markets are very sensitive to cost. With the different technologies capable of meeting the technical requirements, time-to-market and overall system cost will govern technology selection.

Figures of Merit

The wireless communication circuits considered as application drivers may be classified into AMS circuits including analog-to-digital and digital-to-analog converters, RF transceiver circuits including low noise amplifiers (LNAs), frequency synthesizers, voltage controlled oscillators (VCOs), driver amplifiers, PAs and filters. The device FoM tracked by the RF and AMS roadmap such as transit frequency at unity current gain f_T, maximum frequency of oscillation f_{MAX} at unit power gain, noise, voltage gain, mismatch, linearity, power, power added efficiency, breakdown, quality factor, and the like are chosen based on their impact to the performance of these key RF and AMS circuits. A more detailed description of the relation between circuit and device FoM can be found in [1].

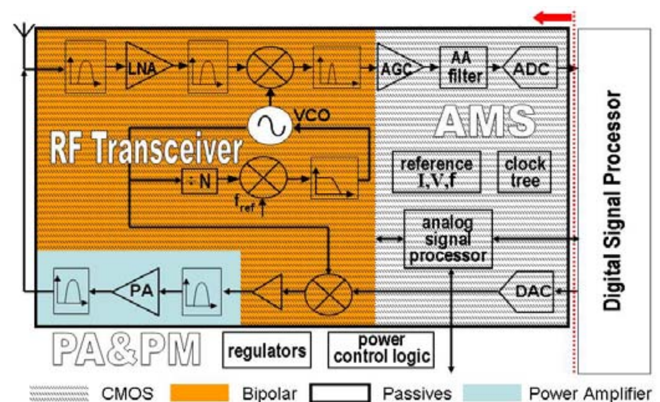

Fig. 2. Circuit functions of a typical wireless communication system and RF and AMS roadmap device partition.

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The 2005 RF and AMS chapter was divided into five main sections [2]. Four sections focused on CMOS, Bipolar, Passives and PAs for the 0.8 to 10 GHz applications, while the last section, mm-Wave, covered the 10 to 100 GHz applications. The application frequencies in this context refer to the nominal carrier frequencies for the communications system and are not necessarily the clock or operating frequencies of the individual devices and circuits. Fig. 2 illustrates the typical radio circuit functions and how the roadmap partitions the different device sections to cover these functions.

CMOS

The trends of higher integration and the cost of technology development drove the need to align the RFCMOS roadmap with the logic platform (ITRS Process, Integration, Devices, and Structures roadmap). The Low-STandby Power (LSTP) CMOS roadmap which was targeted for portable applications was selected as the basis. The RF and AMS CMOS roadmap was delayed by one year compared to the logic LSTP roadmap to reflect the additional time needed to stabilize the technology for RF mixed signal products and allow time to introduce a mature RF analog design kit. Scaling digital CMOS performance (gate length and gate dielectric) results in an aggressive roadmap for device f_T, f_{MAX} (Figs. 3 and 4) and noise. A detailed description of device f_T, f_{MAX} and noise scaling can be found in [3]. The improved f_{MAX} compared to the 2004 roadmap is due to device layout optimization and improved data analysis obtained with complete de-embedding. The challenge for designers will be how to effectively use the increased f_{MAX} for higher frequency applications as supply voltage continues to scale down and the margin for model inaccuracies decreases [4].

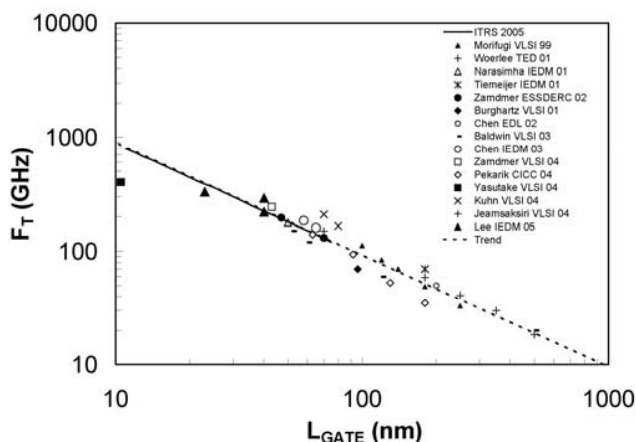

Fig. 3. NFET f_T versus L_{GATE} .

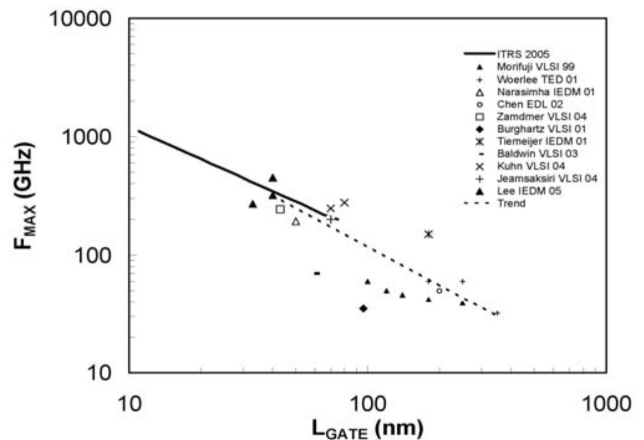

Fig. 4. NFET f_{MAX} versus L_{GATE} .

The requirement of low standby power limits the rate of gate oxide scaling relative to gate length scaling and, for conventional device structures, drives ever increasing doping concentration and non-uniform channel doping. These trends degrade voltage gain (Gm/G_{ds}) and increase the threshold mismatch. In the case of Gm/G_{ds} scaling for the logic LSTP device, the roadmap saturates at 30, which is considered the minimum requirement for analog design (Fi.g 5). New gate electrode materials that enable threshold control via workfunction modulation, double gate structures or asymmetric doping profiles will mitigate this trend. However, it is possible that a unique device design for high gain may be required, supplementing the standard LSTP logic device.

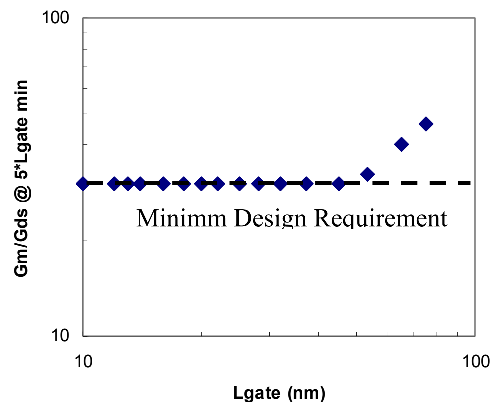

Fig. 5. ITRS 2005 Gm/G_{ds} versus L_{GATE} .

Overall, the long-term prediction of device RF and noise performance becomes more uncertain with the introduction of metal gate electrodes (2009), high permittivity (high-K) gate dielectrics (2009), and new device structures such as fully depleted and/or double-gated SOI (2015) [5]. The introduction of metal gates may reduce threshold mismatch due to variations in gate doping and should increase

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device f_{MAX} due to decreased gate resistance. The introduction of high-K gate dielectrics and channel strain increases uncertainty in device 1/f noise scaling. Fully-depleted, dual-gate SOI has low channel doping relative to conventional CMOS structures and so may have reduced mismatch. Finally, the introduction of multiple threshold voltages for digital power-delay optimization will also offer design options for mixed-signal and RF applications and possibly elevate some of the demands on individual devices as predicted by the roadmap.

In addition to the LSTP logic CMOS device, the RF and AMS roadmap added a thick-oxide device optimized for higher voltage precision analog designs and for driving RF signals off-chip. This device is often used as a second or a third input/output (I/O) transistor for logic applications to support interfaces to the outside world. The mixed-signal supply voltage scaling continues to lag that of digital by two or more generations driven by the need to maintain signal-to-noise ratios and low signal distortion in analog designs. The challenge in supporting this device comes as the LTSP logic CMOS device moves towards a new device structure such as fully depleted and/or double-gated SOI. The fabrication of the conventional precision analog device may require separate process steps resulting in higher wafer/die cost. The increased die cost may drive more interests in SiP/module solutions as opposed to the integrated SoC solutions. On the design research front, new architectures are being introduced that make use of the increased digital processing capabilities allowing more signal treatments to be done in the digital domain and enabling the potential replacement of most analog functions [6]. In addition, research in software defined radios to support low cost multi-mode multi-band applications will drive different technology requirements [7].

SiGe Bipolar

RF and AMS bipolar devices are most frequently used in RF transceiver blocks including LNAs, synthesizers and sometimes PA drivers or PAs. Technology requirements for bipolar devices used in wireless communications are driven by the need for lower power consumption, lower noise, and lower cost much in the same way as CMOS devices. Reduced power consumption and lower noise for bipolar devices are achieved through higher f_T and , f_{MAX} lower base resistance and base collector capacitance. Silicon bipolar devices have undergone strong performance gains since the introduction of SiGe [8]. The SiGe epitaxy process enabled use of bandgap engineering plus aggressive scaling of the base width and base doping. Bipolar scaling also benefits from lithography advances. By scaling the emitter width, device f_{MAX} increases, while noise and power consumption decreases.

In the near-term, the major challenge for scaling the BiCMOS technology is the cost of the technology and the increased difficulty with integrating bipolar devices in aggressively scaled CMOS with conflicting thermal budget requirements. In the 2005 roadmap, three separate bipolar technology requirements are monitored: 1) a high-speed bipolar devices where the device f_T and f_{MAX} continue to improve, challenging III-V technologies in mm_wave applications (Fig. 1); 2) a RF low-cost medium performance device suitable for <10Ghz mobile phone and connectivity solutions; 3) and finally, a high-voltage device optimized for PA drivers and PAs. All three bipolar devices may not be integrated in the state of the art CMOS technologies. The most cost effective solution may be to stay at a relative large geometry BiCMOS platform with the optimized bipolar device for increased frequency [9,10] or power [11] applications.

A more detailed discussion on the different SiGe bipolar device requirements for the emerging mm-wave and PA applications can be found in the following sections.

mm-Wave

The scope of this section includes both low-noise and power transistors that are based on several competing technologies: GaAs MESFET, GaAs PHEMT, InP HEMT, GaAs MHEMT, GaN HEMT, InP HBT and SiGe HBT. Today, compound semiconductors dominate the 10 to 100 GHz applications. The device types most commonly used for analog mm-wave applications are HEMT, PHEMT, and MHEMT while the device types most commonly used for mixed-signal and high-speed applications are predominately MESFET and HBT. There is great diversity in the nature and performance of these devices because device properties are critically dependent on the selection of materials, thickness and doping in the stack, which are proprietary to the manufacturer. Performance trends are driven primarily by a combination of “bandgap engineering” of the epitaxial layer stack in concert with shrinking lithography. Compound semiconductors do not enjoy the long-term heritage of silicon-based devices, nor do they follow Moore’s Law. The biggest challenge facing compound semiconductors is production cost. Uniformity, reproducibility and yield metrics for compound semiconductors in general lag behind Si-based technologies. As production volume in a particular compound technology rises, unit costs decrease similar to that of silicon. In addition, the compound semiconductor wafer diameter needs to be within one or two generations of the silicon industry to take advantage of the advances in lithography and processing equipment. This is particularly challenging as silicon transitions from 200-mm to 300-mm wafers.

Recent advances in SiGe device performance enabled Si technology to venture into application frequencies that had been dominated by III-V compound semiconductors. Transceiver circuits for 60 GHz wireless personal area

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networks (WPAN) [12] and 77 Ghz automotive radar applications [13,14] using SiGe bipolar already show promising results. Figure 6 shows the projected roadmap for these high frequencies devices. The SiGe devices achieve comparable device f_T at a lower BV_{CEO}. However, the lower BV_{CEO} did not impose design limit since in actual design the base is never floating and a more relevant design parameter is device BV_{CBO} [15]. Collector-base breakdown for these fast SiGe devices is projected to be in 5.5 to 4.5 V range. f_{MAX} of these devices are projected to be between 250 to 450 GHz and associated noise figures (NFmin) at 77 Ghz between 5.5 and 3.5 dB. These projections are in line with recently reported performance for a 300 GHz f_T / f_{MAX} device with measured NFmin of 1.4dB at 24 GHz and extrapolated NFmin of ~ 3.5 dB at 60 GHz [9].

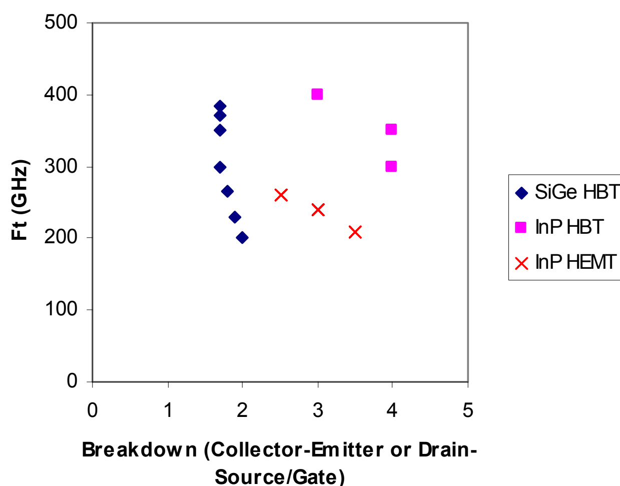

Fig. 6. ITRS 2005 mm_wave device breakdown versus f_T.

The SiGe bipolar processes offer relatively higher level of integration flexibility compared with III-V processes. The III-V device parameters depend heavily on the selection of materials, thickness and doping which makes it difficult to offer more than one device type on the same semiconductor wafer. On the other hand, more than one SiGe bipolar can be offered on the same Si wafer. Multiple SiGe bipolar devices optimized for higher f_T, higher f_{MAX} and lower noise or for higher breakdown [10] are commonly supported with one process flow. The multiple devices enable a higher level of design optimization. As reported in literature, comparable SiGe:C technology yielded a 77 GHz VCO with total output power of 18.5 dBm and phase noise of -97 dBc/Hz at 1-MHz offset [13] and a 77 GHz LNA with noise figure less than 5.5 dB and gain of 8.9 dB [14]. In addition, the CMOS devices in a BiCMOS process allow a high level of chip integration as reported recently for 60 GHz receiver and transmitter integrated circuits [12].

The challenge in designing mm-wave circuits using these high performance bipolar devices on Si is how to handle the lossy Si substrate. Careful layout optimization of the transmission line elements [16] and modeling of backend routing metal are critical at these frequencies. Extra attention in design and layout is also needed to maintain signal isolation. Integration of multi-channels receiver and transmitter will be more of a challenge in terms of ensuring signal integrity across the substrate and routing metal [17].

While SiGe devices have shown capability in mm-wave range, it is unlikely to replace III-V devices in applications where either ultra low noise or high power gain are required. For front end and output stages with challenging requirements, it is likely that III-V technologies such as PHEMT, MHEMT or even the evolving GaN HEMT technology will predominate. For example, InP HEMTS and MHEMTs consistently deliver less than 3 dB noise figure at 60 GHz [18]. GaN based HEMTs show similar excellent noise performance [19] with the added advantage of very high breakdown voltages on the order of 40 Volts. The high breakdown voltage of GaN will result in outstanding linearity and robustness along with low noise figure. Power results are also impressive, with single chip MHEMT MMICs on the order of 4 watts at 40 GHz [18] and for GaN, 8 watts at 30 GHz [20].

Power Amplifier

Wireless communications require both portable (handset) and fixed (base station) transmitters and receivers to form a connected network. Since the PA requirements are very different between the handset and base station, the ITRS RF and AMS roadmap has separate requirement tables for these applications. The PA section covers both III-V and Si-based technologies. The key driving forces for the PA applications are integration of components and cost. A cost parameter is included in the PA tables; Cost/mm^2 for handset PA and Cost/watt for base station PA.

Handset Power Amplifiers

In 2005, the bulk of the consumer market for PA technologies continues to be RFICs and modules for cellular subscriber handsets. Both cellular and connectivity applications typically have very strict performance specifications and are extremely sensitive to price/performance trade-off. This trade-off continuously drives the industry towards highly integrated low-cost system solutions. In the cellular subscriber area, the market for PAs is increasingly migrating away from packaged single die with RFIC to multi-band multi-mode integrated modules that deliver a complete amplifier solution. These RF modules typically integrate all or most of the matching and bypassing networks, and may also provide power detection, power management, filtering and RF switches for both

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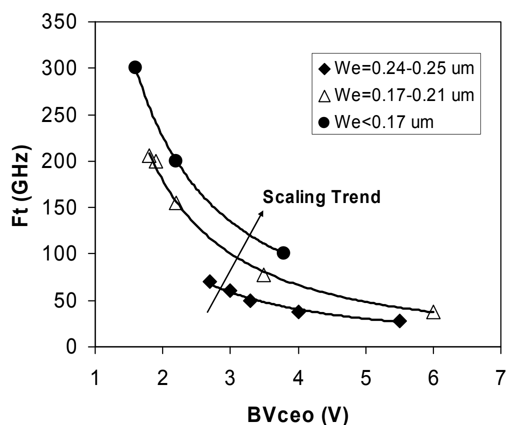
transmit/receive and band selection. Contrary to 2004 predictions, we continue to see the proliferation of 3V-based systems and believe that the 3V systems will remain through the next two to three years. In terms of migrating towards a Si-based solution, the SiGe multi-band cellular PAs are being sampled but they are not yet present in any significant volumes. CMOS PAs are being discussed and sampled, but demonstrations of a viable and rugged PA is still not published.

The biggest advantage for Si-based PA applications is lower die cost (Fig. 7) and the potential for integration. The CMOS controller typically packaged in a front-end PA module today can be included in the same Si die, which reduces total system cost.

	LDMOS	SiGe HBT	GaAs HBT	GaAs FET
PA Die Size (mm^2)	6	2.5	2.5	4
Cost / mm^2 ($$)	0.08	0.12	0.35	0.25
Product Cost ($$)	0.48	0.30	0.875	1.00

Fig. 7. ITRS projected PA die cost for 2006.



Fi.g 8. f_T of SiGe devices as a function of BVceo extracted from the literature for different ranges of emitter width [3]. Generally, more advanced geometry can result in improved f_T and breakdown.

SiGe devices are well suited for PA applications as they can support higher voltage levels for a given level of performance (f_T) vs. CMOS devices. Supporting high voltages is required in a PA despite the lower battery voltages because large antenna mismatch conditions can reflect RF power back into the device causing the collector voltage of a common emitter amplifier to swing to high levels. Figure 8 shows the evolution of breakdown and f_T for SiGe devices. It shows that each new generation of technology has improved both the speed and breakdown voltage simultaneously. This differs from CMOS where the thinner gate oxides required in more advanced nodes make it difficult to improve speed and breakdown simultaneously.

Today, SiGe devices are used extensively in lower power standards such as WLAN and are now being commonly integrated with the rest of the transceiver in applications where output powers levels are in the range of 20dBm [3]. For higher power standards used for cellular applications that require 2 to 3W, SiGe has not yet significantly penetrated the market which is dominated today by GaAs HBTs and, to a lesser extent, discrete RF LDMOS devices. Some benchmark of SiGe and GaAs PA performance have been recently published [21] showing comparable performance levels at 900MHz with better performance for GaAs at 2GHz for a linear CDMA 28dBm PA application.

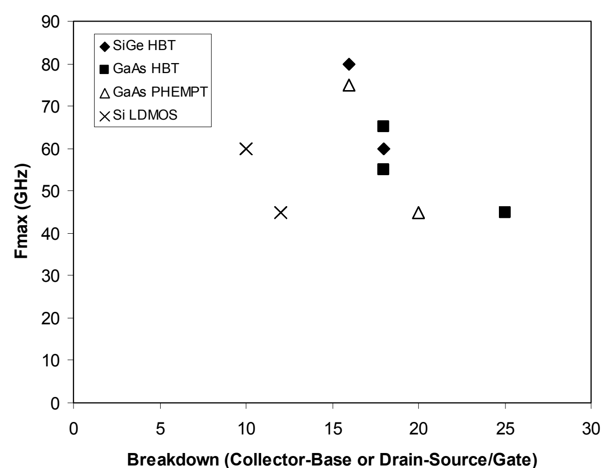


Fig. 9. ITRS 2005 PA device breakdown versus f_{MAX}

Figure 9 compares device f_{MAX} and breakdown voltage of the different PA technologies. However, as noted in earlier publication [3,21], PA performance cannot be extrapolated based purely on device parameters such as f_T, f_{MAX} and breakdown voltage. A PA design needs to be maximized for output power and power added efficiency (PAE) while passing ruggedness specifications from handset vendors. Recent advances in ruggedness protection circuitry and advances in SiGe PA technology is helping to close the performance gap making the reality of SiGe PAs in the cellular market more likely.

Base Station Power Amplifiers

The base station transmitter provides the outgoing data link to the cellular phone. Relatively high RF power (600 W) is required to achieve the desired cellular phone coverage. The major challenges for base station PAs include fabrication with a low amount of individual tuning. Silicon LDMOS transistors are now the technology of choice for cellular

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systems at 900 MHz and at 1900 MHz because of their technological maturity and low cost. Applications are moving from 2 GHz and below to higher frequencies, such as WiMAX at 3.5 GHz and from saturated power amplifiers to more linear power amplifiers for CDMA and WCDMA.

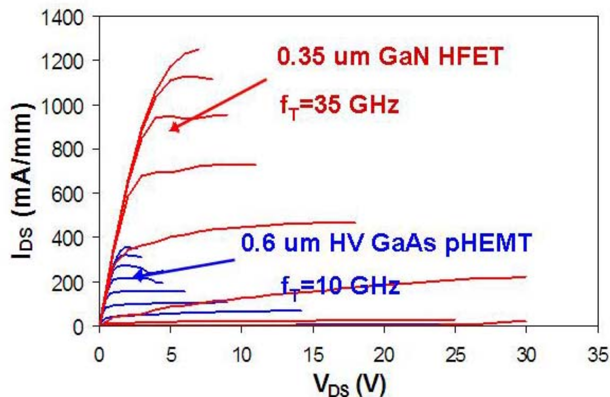

Fig. 10. Comparing GaN to GaAs. GaN device provides 3X higher in current density, 5X higher in breakdown voltage and 5-10X higher microwave power density than GaAs or Si devices.

As frequencies increase, LDMOS will experience challenges from GaAs FET and SiC MESFET. Gallium arsenide devices are more expensive, but offer higher efficiency than Si LDMOS. Gallium nitride is another technology coming over the technological horizon. Gallium nitride has power densities four times larger than silicon LDMOS or gallium arsenide due to the higher device breakdown voltage and current density (Fig. 10) [22]. The major challenge for GaN technology is demonstrating device reliability.

In spite of this move to higher frequencies, device cost as measured by dollars per RF Watt is still projected to steadily decrease from about \$0.70/W today to less than \$0.50/W by 2008.

Passives

Passive devices including capacitors, resistors, varactors, inductors, transformers and transmission lines are frequently used for impedance matching, resonance circuits, filters and bias circuits. The performance of these devices often plays a key role in determining RF and AMS circuits performance. For instance, the critical parameters of a VCO such as frequency tuning range, power consumption and phase noise are primarily determined by the tuning range of the varactor and the quality factor of the inductor and varactor. The biggest challenge for integrating passive elements into a digital CMOS process is the tradeoff between processing cost and device performance. When incorporating passives into a standard CMOS process, there are some additional processing steps and possibly new materials required. In addition, capacitors and inductors generally occupy more silicon area than active devices which effectively increase total die cost. Both the SoC implementation where passive elements move from the board level to chip level and SiP implementation where passives are integrated into the package or module are being used and are dependent on the final system cost.

The long-term challenges for passive elements include the need to integrate new materials in a cost-effective manner to realize high-density, low leakage and high linearity metal-insulator-metal (MIM) capacitors, high density and high quality factor (Q) inductors, high temperature-linearity resistor and high tuning ratio varactor.

In order to achieve high capacitance density for RF MIM capacitors, various high-k dielectrics including Ta_2O_5 and HfO_2 are being explored. The key challenge is to keep the leakage current and voltage nonlinearity low as the film thickness is reduced. The 2005 roadmap is predicting a much slower scaling of the MIM capacitor density compared to the previous roadmap (Fig. 11) to account for the device need to meet all requirements including linearity and leakage and being integrated on a copper backend with no stacking.

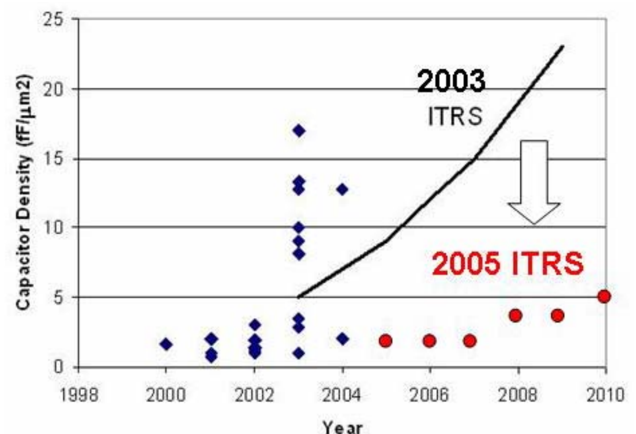

Fig. 11 MIM capacitor scaling.

One way to solve this tradeoff is to use multi-layered structures where the capacitance density and voltage linearity can be separately optimized. A low-cost alternative to the MIM capacitor is the inter-digitated lateral metal-oxide-metal capacitor using the standard multi-layer metal backend. As feature size scales, the unit capacitance of the inter-digitated, MOM capacitor can be close to or exceed that of the standard MIM capacitor. The MOM capacitor will have worse parasitic coupling with the Si substrate and proper layout and structure design is essential to achieve competitive mismatch performance. Nonetheless, the MOM capacitor requires no extra processing and is a good example of tradeoff between performance and cost.

Above-passivation inductors offer high Q-factors and resonant frequencies, but require special processing. On the other hand, improvements in inductance density are difficult

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to realize. Solutions of stacking inductors have been proposed, but add significant cost and jeopardize the resonant frequency. The use of magnetic materials has received some attention in recent publications. However, more research in this area is needed to render a practical solution.

In terms of resistor performance, increasing CMOS complexity makes it more difficult to produce stable, highly manufacturable front-end-of-line (FEOL) resistors. One solution to this problem is to provide high-resistance BEOL resistors comparable to the common p-type polysilicon resistors. However to address the concern with the thermal effect, new materials that provide good thermal control at high currents are needed.

Passives scaling is also directly affected by CMOS device scaling as in the case of MOS capacitors and varactors. The switch to high-k dielectrics in a CMOS device and subsequently the MOS varactors may affect the VCO phase noise. Research is needed to determine the effect on CMOS 1/f noise and MOS varactor Q.

Summary

An overview of the ITRS RF and AMS Wireless roadmap was discussed. Even though not included in the requirement tables today, the technology working group recognized the importance of signal isolation especially as demands for multi-mode, multi-in/multi-out integrated radio increase. Recent publication of a single chip radio [23] showed promising results that substrate crosstalk is manageable. The intention of the working group is to define a FoM for isolation in future roadmaps. Other elements under consideration for inclusion in the roadmap include above-IC integrated MEMs and BAW technologies [24] commonly used for filters and transmit receive (T/R) switch.

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