Precise Alignment of Single Nanowires and Fabrication of Nanoelectromechanical Switch and Other Test Structures

Qiliang Li, *Member, IEEE*, Sang-Mo Koo, *Member, IEEE*, Curt A. Richter, *Senior Member, IEEE*, Monica D. Edelstein, *Member, IEEE*, John E. Bonevich, Joseph J. Kopanski, *Senior Member, IEEE*, John S. Suehle, *Senior Member, IEEE*, and Eric M. Vogel, *Senior Member, IEEE*

***Abstract*—The integration of nanowires and nanotubes into electrical test structures to investigate their nanoelectronic transport properties is a significant challenge. Here, we present a single nanowire manipulation system to precisely maneuver and align individual nanowires. We show that a single nanowire can be picked up and transferred to a predefined location by electrostatic force. Compatible fabrication processes have been developed to simultaneously pattern multiple aligned nanowires by using one level of photolithography. In addition, we have fabricated and characterized representative devices and test structures including nanoelectromechanical switches with large ON/OFF current ratios, bottom-gated silicon nanowire field-effect transistors, and both transfer-length-method and Kelvin test structures.**

***Index Terms*—Contact resistance, nanoelectromechanical switch, nanowire alignment, SiNW FET, transfer length method.**

I. Introduction

NANOWIRES AND nanotubes are being intensively investigated as the active medium for applications in nanoelectronics. There are two primary nanowire device fabrication approaches being considered. In the top-down approach, nanowires are defined in a designed location by etching of patterns created by advanced optical or electron-beam lithography (EBL) [1], [2]. In a bottom-up approach, nanowires are assembled by atom-by-atom growth techniques, such as the chemical-vapor-deposition (CVD) of silicon nanowires from an Au catalyst. These "self-assembled" nanowires are then assembled to construct devices. As top-down lithography is beginning to reach fundamental physical and economic limitations, bottom-up approaches are being considered for fabricating high-density and low-cost circuits and devices. One of the critical issues in the research of bottom-up nanowires is the positioning of the nanowires with respect to the other device features, such as contact to fabricate simple test structures to characterize the electronic properties of these bottom-up grown nanowires. There have been a variety of rather complicated approaches for integrating these nanomaterials to produce test structures for simple electrical characterization. These approaches include: atomic force microscopy (AFM) manipulation of individual nanotubes [3], fluidic alignment of nanowires with electrode defined by EBL [4], electric field-induced *in situ* growth of nanowires [5], [6] and nanotubes [7], [8], electric field-induced assembly of nanowires or nanotubes [9]–[11], and manipulating nanowires/nanotubes with holographic optical traps [12].

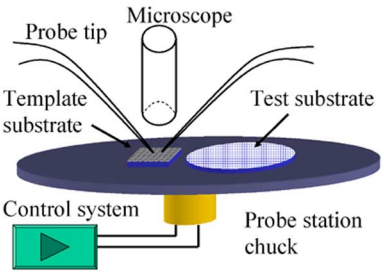


Fig. 1. Schematic of single nanowire manipulation system.

In this paper, we have developed a single nanowire manipulation system (SNMS) to manipulate and align individual CVD grown nanowires via electrostatic force. Compatible fabrication processes have been developed to fully integrate the nanowires into test devices for electrical characterization. Although various methods for assembling nanowires and manipulation of nanowires via electrostatic force have been previously reported, our approach has the following advantages: 1) The manipulation and alignment of nanowires are performed easily and precisely by utilizing the noninvasive inspection capabilities of a high-magnification optical microscope. 2) No advanced lithographic tools [e.g., EBL or focus ion beam (FIB)] are needed. The integration of nanowires into devices and test structures is implemented by conventional photolithography. 3) A large number of nanowire devices having varying structures can be efficiently processed with one level of photolithography. We have used the SNMS to fabricate traditional transfer length method (TLM) and Kelvin test structures that are used to extract the resistance of the nanowires and the contact resistance. In

Manuscript received November 10, 2006. This work was supported in part by the NIST Office of Microelectronics Programs and NIST Semiconductor Electronics Division. The review of this paper was arranged by Associate Editor Y. Lu.

Q. Li, C. A. Richter, M. D. Edelstein, J. J. Kopanski, J. S. Suehle, and E. M. Vogel are with the Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899 USA (e-mail: Qiliang.Li@NIST.GOV; Curt.Richter@NIST. GOV).

S.-M. Koo is with Semiconductor Electronics Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899 USA and also with the Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea.

J. E. Bonevich is with the Metallurgy Division, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2007.891827

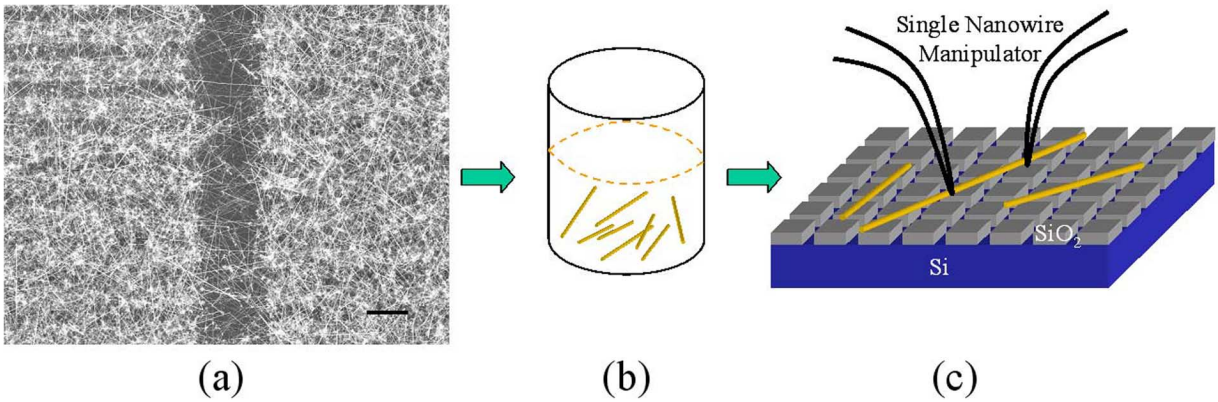


Fig. 2. (a) SEM image of Si nanowires grown from patterned Au catalyst on a silicon wafer. (b) Nanowires were removed into a suspension of DI water. A drop of the nanowire solution was dispersed on a template substrate and evaporated under a vacuum of 100 mtorr for 4 h. (c) Schematic of manipulator tips picking up a nanowire from a template substrate.

addition, nanowire field-effect transistors (FET) and nanoelectromechanical switches were fabricated to further illustrate the strength and flexibility of this approach. Compared to other techniques, the SNMS is an attractive approach for fabricating research devices from self-assembled nanowires because it is a simple and flexible technique which leverages the vast infrastructure of traditional metal-oxide-semiconductor (MOS) fabrication technology.

II. Sample Fabrication

A. Overview

Silicon nanowires were grown via a CVD on a silicon wafer and removed into a suspension of de-ionized (DI) water. A drop of nanowire solution was dispersed on a template substrate and evaporated. The SNMS (schematically shown in Fig. 1) was used to pick up selected nanowires and transfer them to predefined locations on a photolithographically patterned device substrate. The nanowires were further precisely aligned to the device substrate as needed. Finally, top metal contacts were patterned via traditional photolithography to form devices and test structures. The details of the SNMS and associated processing steps are discussed as follows.

B. Preparation of Nanowire for Manipulation

Silicon nanowires (SiNWs) were grown on Si(100) wafers by using CVD with thin Au films ($\sim$1–2 nm) as the catalyst at 450 °C via a vapor–liquid–solid mechanism [13]–[15]. Diluted SiH_4 (10% in N_2) at a pressure of 350 mtorr was used to grow the SiNW. Nanowires of 20–300 nm in diameter and 2–150 μm in length were obtained. Fig. 2(a) shows a scanning electron microscopy (SEM) image of SiNWs grown on an Si wafer from a patterned gold catalyst. The SiNWs were removed into a suspension of DI water by sonication (1 min), as shown schematically in Fig. 2(b). The SiNW solution was dispersed onto a template substrate and dried for 4 h under vacuum at 100 mtorr. Generally, nanowires adhere tightly to a flat surface because of the electrostatic force of the substrate, and the nanowires cannot be picked up if the electrostatic force of the substrate (F_{Sub}) is larger than that of manipulator probe tips (F_{Tip}). In order to avoid the electrostatic force from the template substrate, a template substrate containing a grid structure was used to decrease the contact area between the nanowire and the surface. The template substrate has a matrix of 10×5 μm rectangular solids of SiO_2 (200 nm in thickness) fabricated by etching thermal oxide on silicon substrates under a defined grid-like photoresist pattern. The probes can readily pick up nanowires from this template substrate, as shown in Fig. 2(c).

C. SNMS

The SNMS, schematically shown in Fig. 1, is based upon a commercial probe station (Cascade Microtech semi-automated femtoguard)[1] on a vibration isolation table consisting of a high-magnification optical microscope, precise probe manipulators with titanium probe tips (less than 100 nm in diameter). (**Note**: The commercial probe tips were modified in-house in order to create the small-diameter probe tips necessary for the SNMS, and a chuck control system (Cascade Microtech Nucleus Software) was used in this work.) An automated chuck control system, which can be used to control and store the position, rotation, and height of the chuck, greatly increases the efficiency of the SNMS. Both a nanowire coated template substrate and a device substrate with alignment features (described later) are loaded together into the probe station (Fig. 1). A nanowire can be picked up from the template substrate by the unbiased probe tips via the electrostatic force and then transferred onto the device substrate by controlling the chuck position or moving the manipulators. The SNMS with this setup can easily align nanowires $\geq$ 60 nm in diameter. We believe SNMS can manipulate smaller nanowires with a sharper probe tip and higher magnification optical microscope.

D. Alignment and Integration of Nanowires

Two methods (I & II) have been used for the integration of nanowires into device structures, as shown in the left and right of Fig. 3, respectively. In step 1, the nanowires are transferred from the template substrate to device substrates. For method I, the device substrate is a conventional planar substrate patterned

[1]Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is neither intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

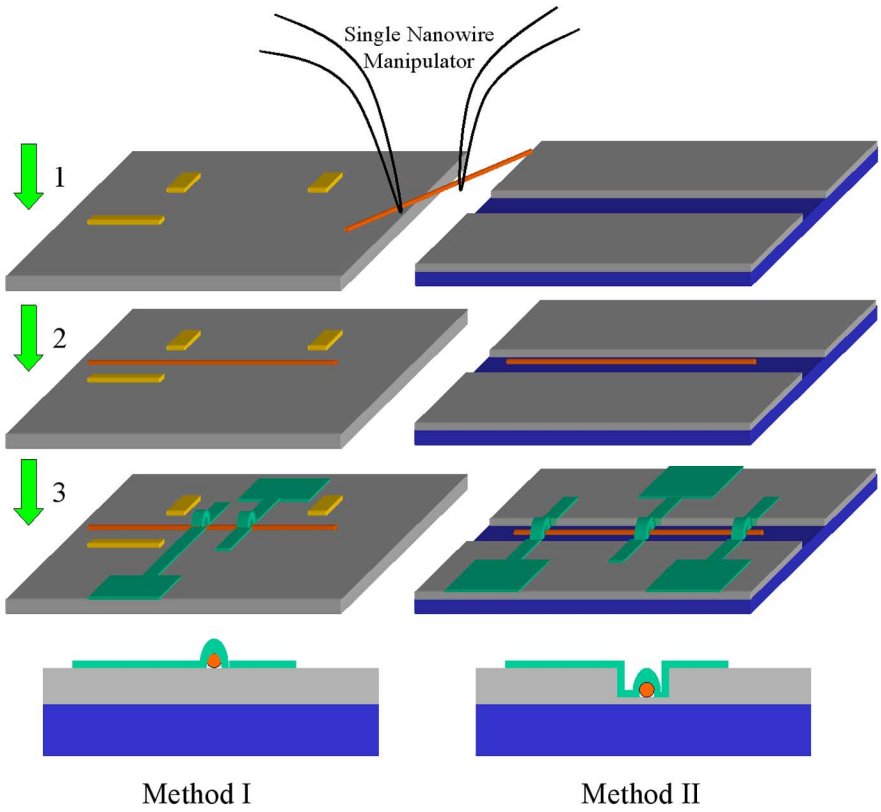


Fig. 3. Two methods (I on the left side and II on the right side) used to align the nanowires. Step 1: placing a single nanowire on a flat (method I) or trench (method II) substrate. Step 2: precision alignment of the nanowire with the substrates. Step 3: formation of metal contacts.

with metal alignment marks patterned on SiO_2. One set of these alignment marks is used for aligning the nanowires to the right location, while a second set is used in the later photolithography step to define metal contacts to the nanowires. In method II, a trench has been used to maintain the nanowires in the pattern during the subsequent multilevel processes (e.g., photoresist spinning, wet cleaning/etching, metal deposition, and lift-off). The trench is obtained by dry-etching 400 nm of a 600-nm thermal oxide. In addition to the set of trench patterns that act as both the alignment marks to position the nanowires and a location to hold the nanowires, a second set consisting of conventional photolithographic alignment marks to define the position of the metal contacts to the nanowires is simultaneously patterned. Typical dimensions of the trenches used in this work are 4 μm in width, 100 μm in length, and 400 nm in depth. Fabrication results indicate that the success rate of integration by method II is over 90% while the success rate for method I is about 75% without using a trench. In step 2, the nanowires are manipulated and placed onto predefined locations on the device substrate by controlling the position and rotation of the probe station chuck. The nanowires are released from the manipulator to the device substrate by the attractive electrostatic force from the substrate. In this case, the electrostatic force F_{Sub} from the flat surface of the device substrate is larger than F_{Tip}. After the nanowires are aligned with respect to the metal fiducials (method I) or trenches (method II), they are covered by 80 nm of sputtered SiO_2 at room temperature. The SiO_2 further helps the nanowires maintain their position for both methods. In step 3, compatible photolithographic steps which are aligned to the initial alignment features were used to define metal contacts to nanowires. The SiO_2 in the contact area was etched by using 2% HF before metal deposition. The contacting metal is deposited by thermal evaporation of a 20-nm Al film followed by a 60-nm Au film and defined by using a lift-off process. The two schematics at the bottom of Fig. 3 (left and right sides) show cross sections of the metal/nanowire structures fabricated by using methods I and II, respectively.

III. TLM and Kelvin Test Structures and SiNW FET

In order to characterize the intrinsic conduction properties of semiconductor nanowires, it is necessary to separately determine the contact resistance. Primarily, the four-terminal method has been used to investigate contact resistance and conductance in nanowires [16]–[18]. Better methods are needed to improve the characterization of these electrical properties. The TLM test structure has been widely used as a precise technique for extracting contact and sheet resistance [19]. As shown in Fig. 4(a), a nanowire-based TLM test structure was fabricated by using method II followed by annealing with N_2 at 420 °C for 60 s to improve the Al/Si contact. For the TLM test structure [in Fig. 4(a)], the total resistance (R_T) of any two contacts is

$$R_T = 2R_C + \rho_l L \tag{1}$$

where R_C is the contact resistance, ρ_l is the resistance per unit length of the SiNW (165 nm in diameter), and L the contact spacing. The plot of total resistance as a function of contact spacing L is shown in Fig. 4(b) for a range of current levels.

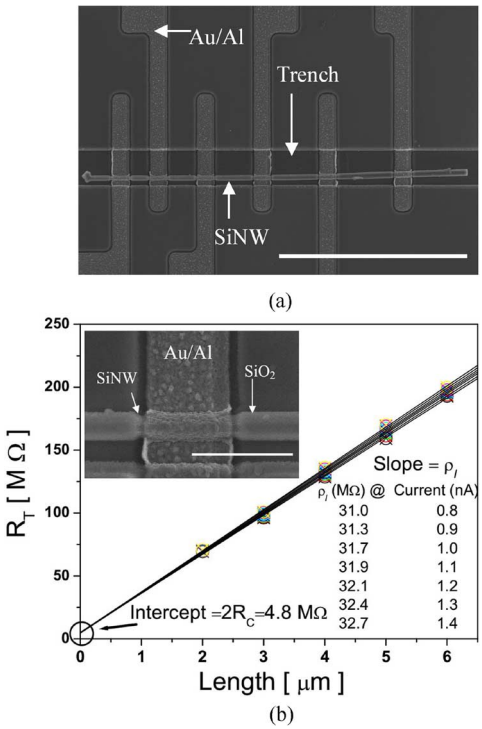


Fig. 4. (a) SEM image of a transfer length method test structure for characterization of metal/SiNW contact resistance. (Scale bar: 20 μm). This particular structure was fabricated by using method II. (b) Plot of total resistance (R_T) as a function of contact spacing, length: 2 to 6 μm. Total resistance of the seven curves was obtained under currents of 0.8 to 1.4 nA. Intercept is $2R_C$, where R_C is the contact resistance (R_C is 2.5 $\mathrm{M}\Omega$ on average). Slopes of each curve are resistance of SiNW (150 nm in diameter) per micrometer under different currents: 0.8 to 1.4 nA. Inset of (b) shows larger image of metal/SiNW contact (Scale bar: 2 μm).

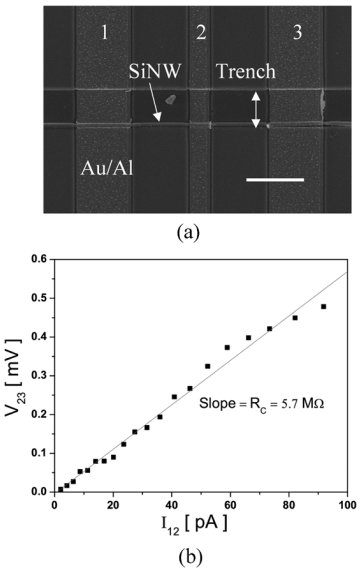


Fig. 5. (a) SEM image of Kelvin test structure for characterization of metal/SiNW contact resistance (Scale bar: 5 μm). This structure, fabricated by using method II, has three electrodes 1, 2 and 3. (b) Plot of voltage across metal/SiNW contact (V_{23}) as a function of current through electrode 1 and 2 (I_{12}). Slope is contact resistance ($\approx 5.7\ \mathrm{M}\Omega$) of SiNW (78 nm in diameter).

From a linear least square fit (LLSF), for this SiNW, the intercept $2R_C$ ranges from 4.5 to 5.1 $\mathrm{M}\Omega$, and the slope of each curve is ρ_l for currents of 0.8 to 1.4 nA [listed in Fig. 4(b)].

The Kelvin test structure is another semiconductor characterization technique widely used to measure contact resistance [19]. As shown in Fig. 5(a), a nanowire-based Kelvin test structure was fabricated by using method II and annealed with N_2 at 420 °C for 60 s to form good Al/Si contacts. With current flowing from contact 1 to contact 2, the contact resistance is

$$R_C = \frac{V_{23}}{I_{12}} \tag{2}$$

where V_{23} is the voltage drop measured between contact 2 and contact 3. The plot of V_{23} as a function of I_{12} is shown in Fig. 5(b). The contact resistance $(\approx 5.7\ \mathrm{M}\Omega)$ is the slope of the plot by using a LLSF.

The specific contact resistivity (ρ_C) is defined as $\rho_C = R_C A$, where A is the contact area (estimated from $\pi \mathrm{D} d$ by assuming a cylindrical feature for SiNW with D as the diameter of the SiNW and d as the contact width, 2 μm for both test structures in Figs. 4(a) and 5(a). The specific contact resistivity of Al and SiNW is found to be $\approx 2.3 \times 10^{-2}\Omega \cdot \mathrm{cm}^2$ and $\approx 2.8 \times 10^{-2}\Omega \cdot \mathrm{cm}^2$ from the TLM and Kelvin structures, respectively. We attribute the relatively high specific contact resistivity to the undoped SiNW; however, further studies are in progress to understand the effect of SiNW doping and annealing condition on the contact resistance.

As shown in the inset of Fig. 6(a), a simple back-gated SiNW FET was fabricated by using method II. The I-V characteristics are shown in Fig. 6(a) $(I_d - V_g)$ and Fig. 6(b) $(I_d - V_d)$. The thick bottom-gate oxide (approximately 200 nm) was obtained by dry etching back a thermally grown 600-nm oxide. The $I_d - V_g$ characteristic indicates the threshold voltage (V_T) at approximately -0.4 V. These results further demonstrate the capabilities of the SNMS.

IV. SiNW Nanoelectromechanical Switch

The SNMS is also capable of fabricating SiNW nanoelectromechanical devices such as the switch shown in Fig. 7. It has been reported that the nanoelectromechanical switches formed from carbon nanotubes (based upon EBL) showed interesting switching behaviors [20], [21]. We report here the fabrication of a nanoelectromechanical switch with single SiNW based on method I. Schematics of the fabrication of this single SiNW nanoelectromechanical switch are shown in Fig. 7. The nanowire was first placed on a predefined location with one end suspended above a metal pad by SNMS (left schematic). The suspended gap is obtained by dry-etching 400 nm of the 600-nm thermal SiO_2 followed by 20-nm Au deposition and lift-off. Then, a second-level metal (20 nm/60 nm of Au/Al) was patterned on both sides of the SiNW (right schematic). The metal deposited on the suspended end of the SiNW creates better electrical contact when the switch is closed to turn it on (i.e., the SiNW touches the bottom metal pad).

An SEM image of an SiNW nanoelectromechanical switch is shown in Fig. 8(a). The typical, reversible switching current–voltage characteristics of the SiNW switch are shown in Fig. 8(b) with an inset of the switch ON/OFF diagram. The switch remains off (i.e., open) until the voltage is high enough (turned-on voltage, $V_{\mathrm{On}} = 5$ V) to bend the nanowire to touch the bottom metal pad. The ON/OFF current ratio is over 10 000. The OFF state is re-established as the voltage decreases to

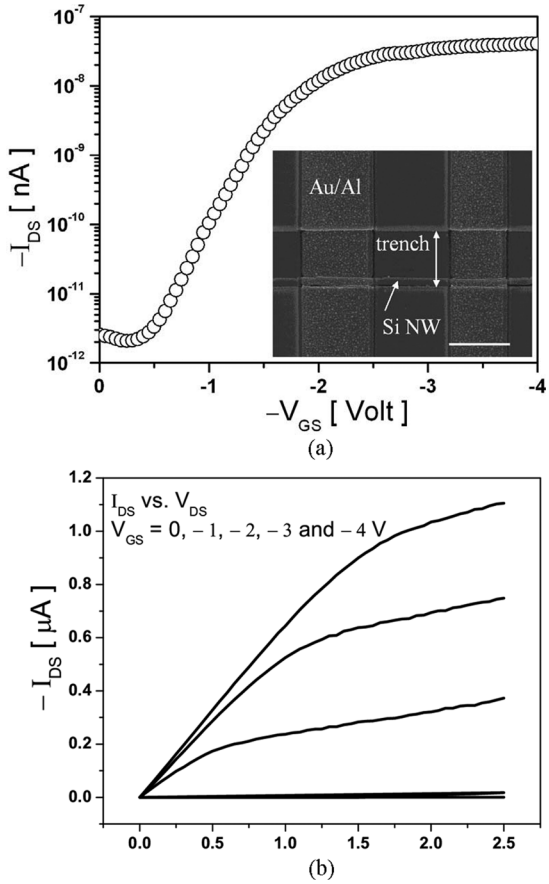


Fig. 6. (a) $I_{DS}-V_{GS}$ with $V_{DS}=-100$ mv and $(b) I_{DS}-V_{DS}$ of a simple bottom-gated SiNW (145 nm in diameter) FET. Inset of (a) is SEM image (Scale bar: 3 μm).

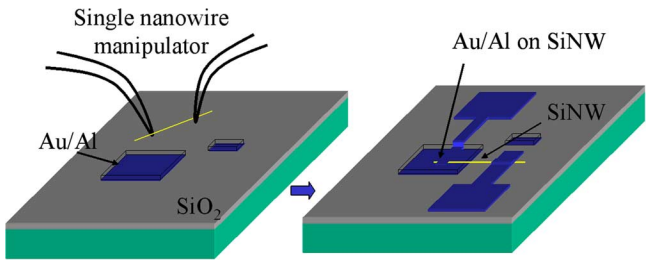


Fig. 7. Schematics of fabrication of nanoelectromechanical switch with SiNW suspended above a metal pad by using method I.

$V_{\mathrm{Off}}(V_{\mathrm{Off}} < V_{\mathrm{On}})$. Similar effects were also reported in nanotube nanoelectromechanical switches [20], [21]. We believe the hysteresis in the I-V curve is due to the electrostatic force between the SiNW and the metal pad.

V. Conclusion

In this paper, we have developed a single nanowire manipulation system and compatible photolithographic processes to align and integrate nanowires. In addition, we have developed and characterized nanowire-based TLM and Kelvin test structures for measuring the resistance of contacts to nanowires. We have also fabricated a simple SiNW FET and a SiNW nanoelectromechanical switch with a large ON/OFF ratio. The fabrication

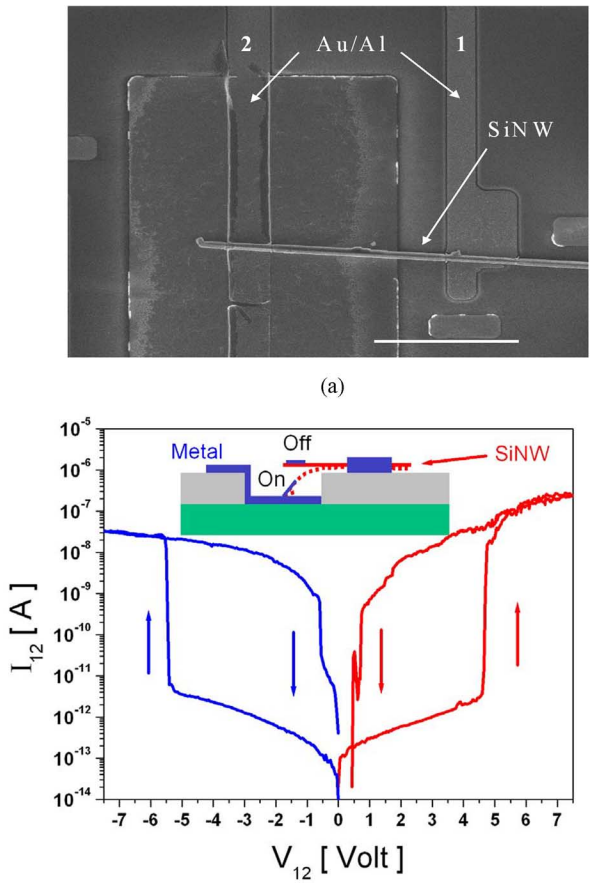


Fig. 8. (a) SEM image of SiNW NEMS (Scale bar: 10 μm). Suspended gap is 400 nm. SiNW is about 150 nm in diameter. (b) Plot of switching current (I_{12}) as a function of switching voltage (V_{12}). Inset of (b) shows schematic of NEMS switch ON/OFF as the SiNW is bent by electrostatic force.

of various test structures and devices by using one regular photolithographic step indicates the SNMS approach is an attractive strategy to integrate nanowires for research device applications.

Acknowledgment

Contribution of the National Institute of Standards and Technology is not subject to U.S. copyright. Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

The authors would like to thank H. Xiong and K.-S. Chang for careful reading of the manuscript.

References

[1] L. L. Chang, Y. K. Choi, J. Kedzierski, N. Lindert, P. Q. Xuan, J. Bokor, C. M. Hu, and T. J. King, "Moore's law lives on—Ultra-thin body SOI and FinFET CMOS transistors look to continue moore's law for many years to come," *IEEE Circuits Devices*, vol. 19, no. 1, pp. 35–42, 2003.

[2] T. Hiramoto, H. Majima, and M. Saitoh, "Quantum effects and single-electron charging effects in nano-scale silicon MOSFETs at room temperature," *Mater. Sci. Eng. B-Solid State Materials for Advanced Technol.*, vol. 101, pp. 24–27, 2003.

[3] T. Hertel, R. Martel, and P. Avouris, "Manipulation of individual carbon nanotubes and their interaction with surfaces," *J. Phys. Chemistry B*, vol. 102, pp. 910–915, 1998.
[4] Y. Huang, X. Duan, Q. Wei, and C. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science*, vol. 291, pp. 630–633, 2001.
[5] C. H. Oon and J. T. L. Thong, "*In situ* nanowire growth for electrical interconnects," *Nanotechnol.*, vol. 15, pp. 687–691, 2004.
[6] J. T. L. Thong, C. H. Oon, M. Yeadon, and W. D. Zhang, "Field-emission induced growth of nanowires," *Appl. Phys. Lett.*, vol. 81, pp. 4823–4825, 2002.
[7] Y. G. Zhang, A. L. Chang, J. Cao, Q. Wang, W. Kim, Y. M. Li, N. Morris, E. Yenilmez, J. Kong, and H. J. Dai, "Electric-field-directed growth of aligned single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, pp. 3155–3157, 2001.
[8] A. Ural, Y. M. Li, and H. J. Dai, "Electric-field-aligned growth of single-walled carbon nanotubes on surfaces," *Appl. Phys. Lett.*, vol. 81, pp. 3464–3466, 2002.
[9] P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, "Electric-field assisted assembly and alignment of metallic nanowires," *Appl. Phys. Lett.*, vol. 77, pp. 1399–1401, 2000.
[10] J. J. Boote and S. D. Evans, "Dielectrophoretic manipulation and electrical characterization of gold nanowires," *Nanotechnol.*, vol. 16, pp. 1500–1505, 2005.
[11] L. A. Nagahara, I. Amlani, J. Lewenstein, and R. K. Tsui, "Directed placement of suspended carbon nanotubes for nanometer-scale assembly," *Appl. Phys. Lett.*, vol. 80, pp. 3826–3828, 2002.
[12] R. Agarwal, K. Ladavac, Y. Roichman, G. H. Yu, C. M. Lieber, and D. G. Grier, "Manipulation and assembly of nanowires with holographic optical traps," *Optics Expr.*, vol. 13, pp. 8906–8912, 2005.
[13] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," *Appl. Phys. Lett.*, vol. 4, pp. 89–90, 1964.
[14] E. I. Givargizov, "Fundamental aspects of Vls growth," *J. Crystal Growth*, vol. 31, pp. 20–30, 1975.
[15] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, "Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction," *J. Vacuum Sci. Technol. B*, vol. 15, pp. 554–557, 1997.
[16] J. F. Lin, J. P. Bird, Z. He, P. A. Bennett, and D. J. Smith, "Signatures of quantum transport in self-assembled epitaxial nickel silicide nanowires," *Appl. Phys. Lett.*, vol. 85, pp. 281–283, 2004.
[17] S. E. Mohney, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. M. Redwing, and T. S. Mayer, "Measuring the specific contact resistance of contacts to semiconductor nanowires," *Solid-State Electron.*, vol. 49, pp. 227–232, 2005.
[18] E. Stern, G. Cheng, M. P. Young, and M. A. Reed, "Specific contact resistivity of nanowire devices," *Appl. Phys. Lett.*, vol. 88, pp. 053106–053106, 2006.
[19] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: Wiley, 1998.
[20] S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube," *Appl. Phys. Lett.*, vol. 86, pp. 083105–083105, 2005.
[21] J. E. Jang, S. N. Cha, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Nanoelectromechanical switches with vertically aligned carbon nanotubes," *Appl. Phys. Lett.*, vol. 87, pp. 163114–163114, 2005.

Qiliang Li (S'01 –M'04) received the B.S. degree in physics from Wuhan University, Wuhan, China, in 1996, the M.S. degree in physics from Nanjing University, Nanjing, China, in 1999, and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 2004. His doctoral research was in the area of molecular electronics and hybrid silicon/molecular field effect transistors and memories.

Since 2004, he has been with the Semiconductor Electronics Division of National Institute of Standards and Technology (NIST), Gaithersburg, MD, as a Research Scientist, where he has been involved with the simulation, fabrication and characterization of advanced CMOS and solid state nanoelectronics materials and devices. He has also worked on silicon solar cell, ferroelectric and magnetoresistance materials and devices. He is an author of over 35 technical papers and one U.S. patent.

Sang-Mo Koo (M'05) received the B.S. degree in electrical engineering from Korea University, Seoul, in 1997, and the Ph.D. degree in electronics from the Royal Institute of Technology (KTH), Stockholm, Sweden, in 2003.

In 1999, he was a Visiting Researcher at Francis Bitter Magnet Lab, Massachusetts Institute of Technology (MIT), Cambridge, where he research magnetic memory junctions. In 2000, he joined the Device Technology Lab of KTH, where he has been engaged in the development of field-effect transistors in wide bandgap semiconductors. In 2003, he joined the Semiconductor Electronics Division of National Institute of Standards and Technology (NIST), Gaithersburg, MD. His research at NIST was focused on the silicon-based nanoelectronic devices. In 2006, he joined the faculty of Kwangwoon University, Seoul, Korea, where he is currently an Assistant Professor of electronic materials engineering. His current research interests include advanced semiconductor materials and transistors, and nanowire-/nanotube-based devices. He has authored or coauthored over 30 papers, a book chapter, and five invited conference presentations.

Curt A. Richter (SM'02) was born in Roanoke, VA, in 1965. He received the B.S. degree from The College of William and Mary, Williamsburg, VA, and the M.S., M.Phil., and Ph.D. degrees in applied physics from Yale University, New Haven, CT.

After matriculation from Yale, he joined NIST. During much of Richter's tenure at NIST he has been studying the physical properties of gate dielectric materials for Si CMOS technology, with an emphasis on interface roughness and accurate measurements of ultrathin-film thickness. In addition to his current technical research on molecular electronics, he is a recognized leader in the field of electrical and optical characterization of gate dielectric materials. He is an author of more than 65 technical articles and Editor of one book. He is currently Project Leader of the Nanoelectronic Device Metrology Project which is currently developing measurement science infrastructure for post-CMOS technologies (such as molecular electronics and confined-Si electronics) that show promise to extend traditional scaling laws for increased computational performance beyond the limits of conventional CMOS.

Dr. Richter serves on the Steering Committee for the ISDRS, is a TAB Member for the SRC, is part of the ITRS ERM Working Group, and is an NNI advisor.

Monica D. Edelstein (M'04) received the BEE degree from Johns Hopkins University, Baltimore, MD, in May 2004.

She has been a member of the technical staff at the National Institute of Standards and Technology (NIST), Gaithersburg, MD, since 1988, where she has been involved with a variety of research on advanced CMOS and nanoelectronics, including electron beam lithographic fabrication, electrical and physical characterization, organic electronics, and dielectric reliability metrology.

John E. Bonevich received the B.S.E. degree in metallurgical engineering from University of Michigan, Ann Arbor, in 1986, and a Ph.D. degree in materials science and engineering from Northwestern University, Evanston, IL, in 1991.

He had research fellowships at Hitachi Advanced Research Laboratory and the NCEM at Lawrence Berkeley Laboratory prior to joining the MSEL at NIST in 1995. He is the Director of the MSEL Microscopy Facility. His research interests include structure, property relationships in microelectronic interconnects, magnetic multilayer thin films, ferroelectric and optical materials, and nanostructured materials.

Joseph J. Kopanski (M'87-SM'01) received the B.S. degree in applied physics and the M.S. degree in electrical engineering and applied physics from Case Western Reserve University, Cleveland, OH, in 1982 and 1985, respectively. His thesis involved the development of semiconductor processing technology for silicon carbide MOSFET.

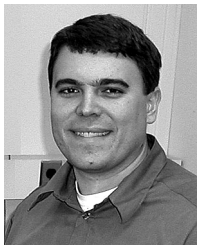
He joined the National Institute of Standards and Technology (then the National Bureau of Standards) in Gaithersburg, MD, in 1985, where he is currently a member of the technical staff. His research interests are currently focused on using scanning probe techniques, such as scanning capacitance microscopy, tunneling atomic force microscopy, and scanning Kelvin force microscopy for electrical transport characterization of nanostructures. He is Director of the Summer Undergraduate Research Fellowship (SURF) program in the Electronics and Electrical Engineering Laboratory of NIST. He is the first author of over 40 publications.

Dr. Kopanski received U.S. Department of Commerce's bronze metals for superior federal service in 2000 and 2002. He is a member of ECS.

John S. Suehle (SM '95) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1980, 1982, and 1988, respectively.

Since 1982, he has been in the Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), Gaithersburg, MD, where he is Leader of the CMOS and Novel Devices Group. His research activities include failure and wear-out mechanisms in semiconductor devices, radiation effects in microelectronic devices, micro-electro-mechanical-systems (MEMS), and metrology issues relating to future electronic devices. He has published over 150 technical papers or conference proceedings and holds five U.S. patents.

Dr. Suehle has served as Guest Editor of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY and holds positions on the editorial review board of the IEEE TRANSACTIONS ON ELECTRON DEVICES and on management committees of the IEEE International Reliability Physics Symposium and the IEEE International Integrated Reliability Workshop. He serves as the Chairman of the Oxide Integrity Working Group of the EIA/JEDEC JC 14.2 Standards Committee and is a member of Eta Kappa Nu.



Eric M. Vogel (S'93–M'96–SM'06) received the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, NC, in 1998.

He is currently Associate Professor of Electrical Engineering at the University of Texas, Dallas (UTD). Prior to joining UTD in August of 2006, he was Leader of the CMOS and Novel Devices Group at the National Institute of Standards and Technology. He has performed a broad range of research in MOS devices, nanodevices, and gate dielectrics including electrical characterization, physical characterization, and reliability physics. He has published over 50 journal publications and proceedings, has written two book chapters, and has given over 25 invited talks and tutorials.

Dr. Vogel is a member of the International Technology Roadmap for Semiconductors (ITRS) Emerging Research Materials working group, was Founding Director of the NIST AML Nanofab, was General Chair of the 2005 Semiconductor Interface Specialists Conference, and has been involved in numerous conferences.