

Status of High-Voltage, High-Frequency Silicon-Carbide Power Devices [†]

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Abstract: *The emergence of High-Voltage, High-Frequency (HV-HF) Silicon-Carbide (SiC) power devices is expected to revolutionize commercial and military power distribution and conversion systems. The DARPA Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is spearheading the development of HV-HF SiC power semiconductor technology. In this paper, detailed characteristics of the devices being produced by the HPE program are presented and the circuit performance enabled by these devices is discussed.*

Keywords: High-voltage; Power semiconductor; Silicon-carbide; Solid State Power Substation; Wide band-gap.

Introduction

Recent breakthroughs in Silicon Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10-kV, 20-kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize commercial and military power distribution and conversion by extending the use switch-mode power conversion to high voltage applications.

Currently, there are significant efforts underway to accelerate the development and application insertion of the new HV-HF SiC devices. The goal of the ongoing Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is to develop 10-kV, 100-A, 20-kHz class power semiconductor devices enabling future electric ships, more electric aircraft, and all electric combat vehicles [1]. DARPA is particularly interested in developing the power electronics device technology deemed necessary to enable a 2.7 MVA Solid State Power Substations (SSPS) for future Navy warships.

The purpose of this paper is to describe the recent progress and current status of the devices being developed in Phase 2 of the DARPA HPE program. In reference [2], performance metrics and measurement equipment needed to evaluate HV-HF device and package performance was introduced. Currently, these device and package performance metrics developed at National Institute of

Standards and Technology (NIST) along with the wafer level performance metrics developed at the Naval Research Laboratory (NRL) are being used to assess progress toward meeting the HPE Phase 2 goal of developing reliable 10-kV, 100-A, 20-kHz class SiC half-bridge power modules. The results presented in this paper are for devices developed early in HPE Phase 2.

10-kV SiC PiN Diode

Substantial progress has been made thus far in HPE Phase 2 by demonstrating PiN diodes with excellent breakdown voltage and leakage current characteristics, improved on-state voltage, and improved forward bias degradation performance. Progress has also been made in increasing the speed of the PiN diode, although further improvement is required to enable 20 kHz hard switching at 200 °C.

Figure 1 shows the reverse leakage current and breakdown characteristics for a 0.2-cm² PiN diode produced in HPE Phase 2. These characteristics are measured with a pulse width of 0.1 s using the NIST variable-pulse-width 25-kV curve-tracer with a voltage isolated temperature controlled test fixture. The characteristics of Figure 1 demonstrate a sharp breakdown voltage above 12 kV (1 mA/cm²) with extremely low leakage current below 10 kV (less than 10 nA) for all temperatures from 25 °C to 200 °C. The positive temperature coefficient of breakdown voltage suggests uniform avalanche multiplication across the chip. The individual voltage and current pulse waveforms (not shown) are also repeatable and do not have the sporadic oscillations and momentary faults seen in previous devices.

Figure 2 shows the forward conduction characteristics of a HPE Phase 2 PiN diode for temperatures from 25 °C to 200 °C indicating the 300 W/cm² power dissipation level. This indicates that the device can operate continuously at 20 A (100 A/cm²) with a package capable of dissipating 300 W/cm². The device has a small negative temperature coefficient of -1.4 mV/C at 20 A. This should provide reasonable ability to parallel multiple chips.

Figure 3 shows the temperature dependence of an HPE Phase 2 PiN diode reverse recovery switching waveform. Although the reverse recovery time is much faster than high voltage Silicon PiN diodes, further improvement is needed to enable 20 kHz hard switching at 200 °C. (A reverse recovery time of 50 to 100 ns is necessary to prevent excessive switching loss in the complementary MOSFET switch.) Figure 4 shows a comparison of the

[†] Contribution of NIST; not subject to copyright. The devices discussed in this paper were produced by Cree Inc. under a DARPA HPE Phase 2 contract funded by Sharon Beerman-Curtin (DARPA) and monitored by Harry Dietrich (ONR).

reverse recovery waveforms at 200 °C for two different PiN diode designs. The reverse recovery time is determined with a dI/dt that results in a peak reverse recovery current approximately equal to the forward current. The reverse recovery time has been improved from 500 ns for device (a) to 300 ns for device (b).

A major concern with SiC PiN diodes in the past has been forward bias degradation. This has been shown to be due to stacking fault growth nucleated at defects originating in the starting wafer and from process induced defects. Recently progress has been made in eliminating these nucleation sites resulting in devices that do not degrade after many hours of operation [3,4]. Figure 5 shows the change in forward voltage of two HPE Phase 2 PiN diodes after being stressed for hundreds of hours at 20 A. Device (c) degraded by 0.4 V while device (d) only degraded slightly.

Figure 6 shows the current uniformity images (obtained using high speed transient thermal imaging) of device (c) in Figure 5 before and after 0.4 V of forward bias degradation. The pattern on the device before degradation is due to shadows from the wirebonds. Although the increased on-state voltage does not represent a significant increase in on-state loss, it does reduce the current conduction area and thus degrades the thermal performance [4]. This is a dramatic improvement, however, from the forward voltage increase and conduction area reduction seen in previous devices [2,4].

10-kV SiC MOSFET

Substantial progress has been made thus far in HPE Phase 2 in demonstrating 10-kV SiC MOSFET characteristics that are generally suitable for 20 kHz hard switching applications such as the SSPS. Major accomplishments beyond previous MOSFETs [6] include lower internal gate resistance leading to faster switching, higher transconductance leading to better on-state voltage and lower gate voltage requirements, and higher threshold voltages resulting in the channel being fully off at $V_g=0$ V for temperatures up to 175 °C.

Figure 7 shows the voltage blocking characteristics of an HPE Phase 2 MOSFET for different temperatures and gate voltages indicating that the device is fully off for gate voltages less than 0 V and temperatures less than 175 °C (i.e., the leakage current is the same for all curves with $V_g \leq 0$). At each temperature the gate voltage is increased until the channel current added to the leakage current. For example, at 25 °C, the channel is fully off for $V_g = +1$ V but results in additional current through the MOSFET channel for $V_g = +2$ V. Similarly, at 175 °C the channel current is fully off for $V_g = 0$ V but results in an increased current for $V_g = 1$ V. It is important for the channel to be fully off while blocking high voltage to avoid FBSOA failures that may result from the decrease in threshold voltage with increasing temperature. The HPE Phase 2 MOSFETs do not exhibit the sporadic oscillations and

momentary faults often observed in the leakage current pulses of HPE Phase 1 devices.

Figure 8 shows the forward output characteristics at (a) 25 °C and (b) 200 °C for an HPE Phase 2 MOSFET with gate voltages from 0 through 20 V in steps of 2 V. These figures indicate that the MOSFET is fully on at 8 A for gate voltages from 16 to 20 V. Figure 9 shows the $V_g = 20$ V curve (on-state characteristic) for temperatures from 25 °C to 200 °C in steps of 25 °C indicating the 300 W/cm² power dissipation level. This indicates that the device can operate at 4 A (30 A/cm²) for the entire temperature range with less than 300 W/cm² heat removal requirement for the package.

Figure 10 shows clamped inductive load turn-off waveforms for different turn-off currents, a clamp voltage of 5-kV, and a gate resistance of 4 Ω. This figure indicates that the devices can be switched off safely for a clamped inductive load with over 128 A/cm² and a 5-kV clamp voltage. The switching speed is 30 ns for the 16-A case and 80 ns for the 4-A case. This is significantly faster than HPE Phase 1 devices.

Conclusion

Although HPE Phase 2 is in the early stages, significant progress has been demonstrated in improved breakdown voltage and leakage current characteristics, lower on-state voltage, and higher switching speeds. Substantial improvements have also been made in overcoming device reliability concerns such as PiN diode forward bias voltage degradation and MOSFET gate leakage.

Acknowledgment

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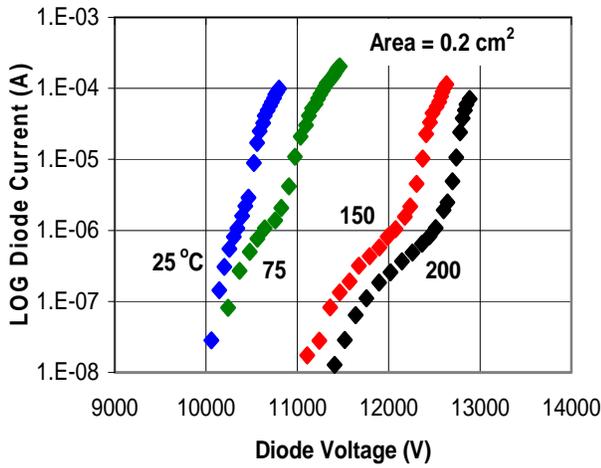


Figure 1. Log of reverse leakage current versus voltage for a SiC PiN diode at different temperatures.

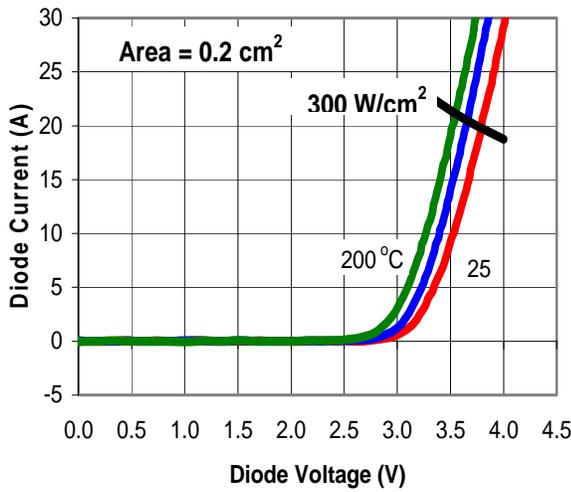


Figure 2. Forward conduction characteristics of a 10-kV SiC PiN diode at 25 °C, 100 °C and 200 °C.

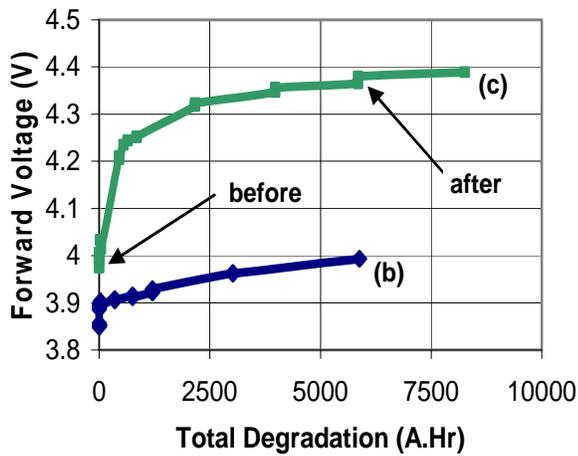


Figure 5. Forward voltage degradation versus forward conduction time at 20 A for two devices.

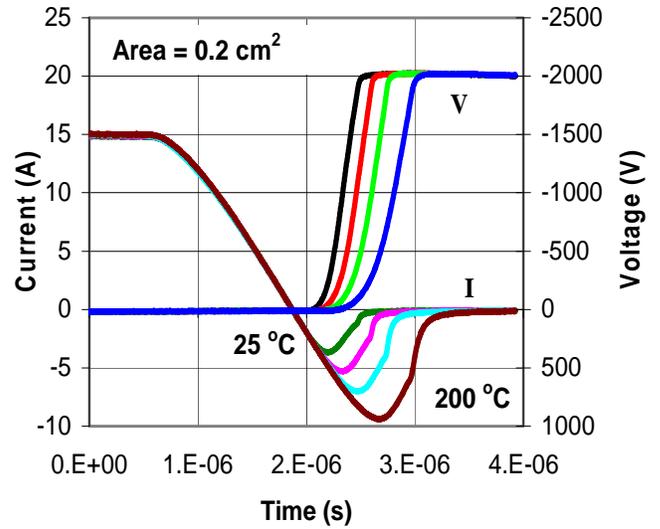


Figure 3. Reverse recovery characteristics for a 10-kV SiC PiN diode at 25, 75, 125, and 200 °C.

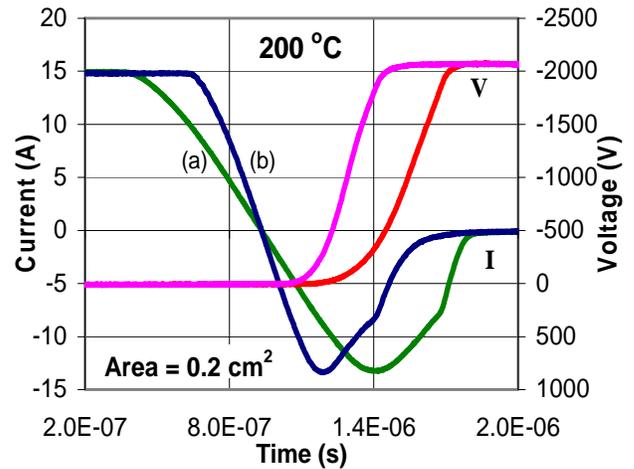


Figure 4. Reverse recovery time for two different 10-kV SiC PiN diodes at 200 °C.

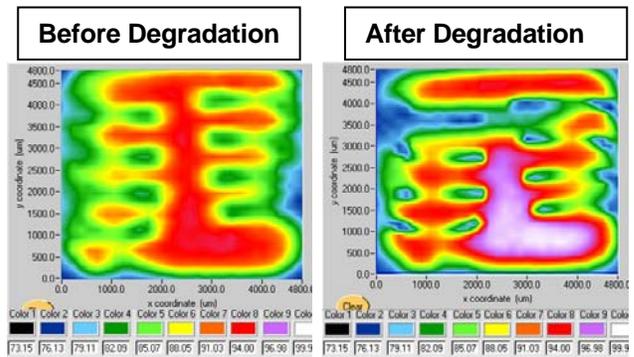


Figure 6. Current uniformity obtained from high speed thermal images before and after degradation as indicated in Figure 5 for device (c).

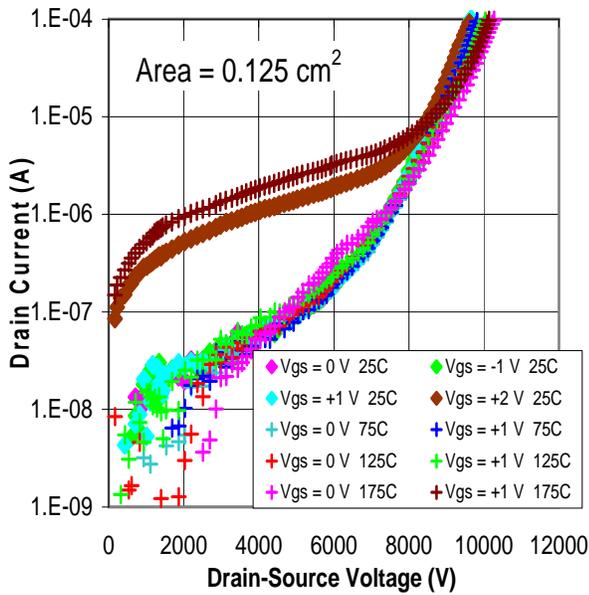


Figure 7. Forward blocking characteristics of a 10-kV SiC MOSFET at different gate voltages and temperatures.

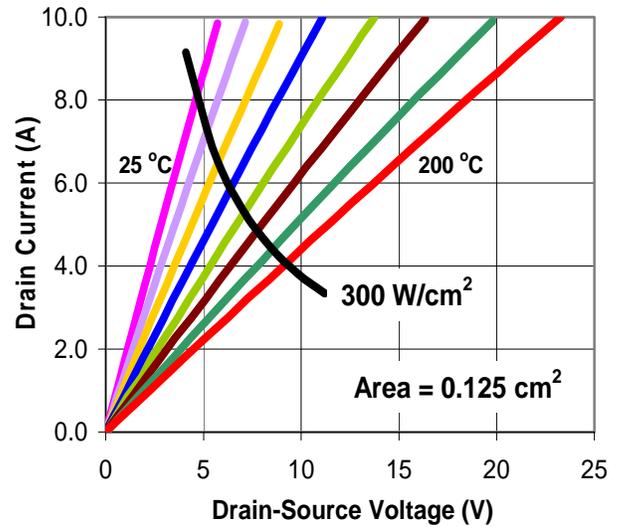
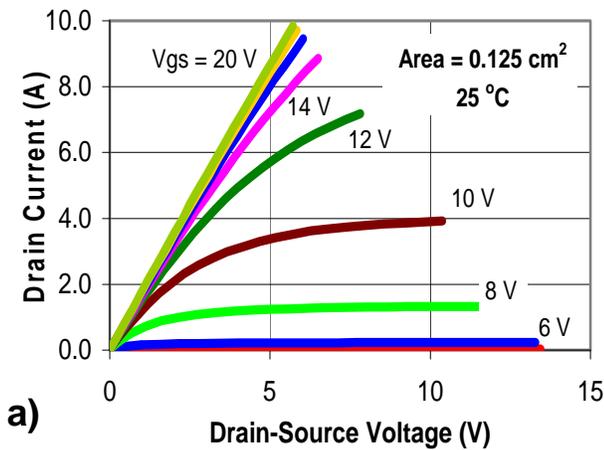
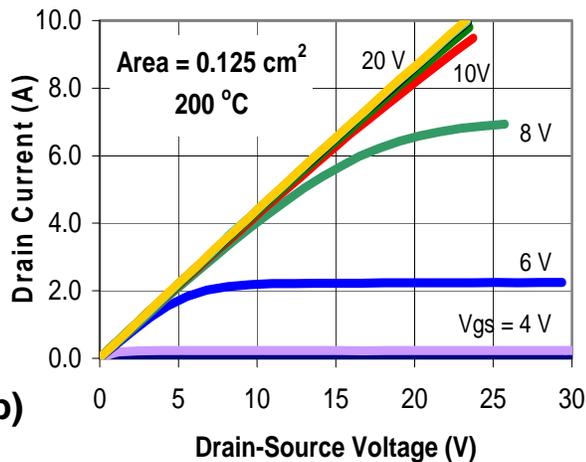


Figure 9. On-state characteristics for $V_g=20$ V at temperatures from 25 °C to 200 °C in steps of 25 °C indicating the 300 W/cm² power dissipation level.



a)



b)

Figure 8. Forward conduction characteristics of a 10-kV SiC MOSFET at (a) 25 °C and (b) 200 °C with gate voltages from 0 V to 20 V in of 2 V steps.

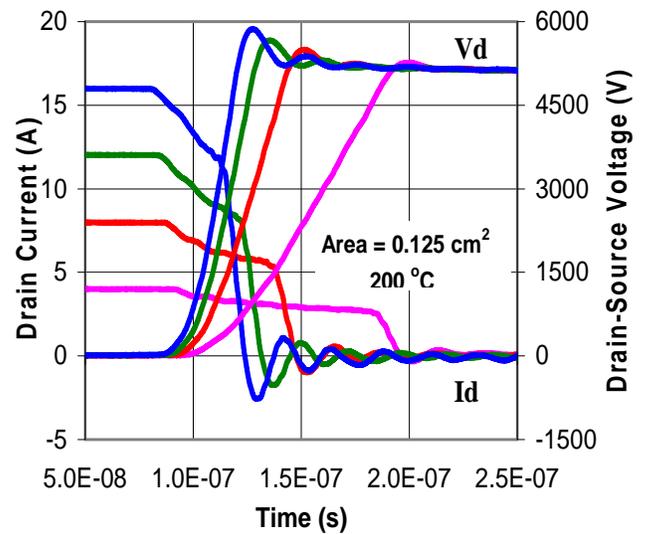


Figure 10. Inductive load turn-off switching current and voltage waveforms for inductor currents of 4, 8, 12 and 16 A at 25 °C.