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Interface characterization of molecular-monolayer/SiO_2 based molecular junctions

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Abstract

We present a correlation of the results of dc-current–voltage (*IV*) and ac-capacitance–voltage (*CV*) measurements with vibrational spectroscopy of Au/monolayer/SiO_2/Si structures to establish an improved understanding of the interactions at the buried metal/monolayer and dielectric/silicon interfaces. A novel backside-incidence Fourier-transform infrared-spectroscopy technique was used to characterize the interaction of the top-metallization with the organic monolayers. Both the spectroscopic and electrical results indicate that Au has a minimal interaction with alkane monolayers deposited on SiO_2 via silane chemistry. An intriguing negative-differential-resistance and hysteresis is observed in the *IV* measurements of Au/alkane/SiO_2/Si devices. It is unlikely that this behavior is intrinsic to the simple alkane monolayers in these structures. We attribute the observed *IV* features to charge trapping and detrapping at both the alkane/SiO_2 and the Si/SiO_2 interfaces.
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Keywords: Molecular electronics; Negative-differential-resistance; Self-assembled monolayer; Current–voltage; Capacitance–voltage; FTIR

1. Introduction

Novel electrical functionalities such as negative-differential-resistance (NDR) [1,2] and two-state switching [3–8] (or hysteresis) are highly sought after for emerging technologies such as molecular electronics [9–18]. In the search for devices that exhibit such novel effects, it is critical to ensure that the observed behavior is arising from an intrinsic property of the molecules (or other novel material under test) and not from artifacts of the test platform. The electronic functionality experimentally observed in molecular electronic devices is typically directly attributed to the behavior of the molecules in the structures; however, in some cases molecule independent effects such as switching have been observed in molecular electronic test structures [7,8]. In certain molecular structures, these effects are attributable to the interfaces in the devices [7]. Therefore, in order to observe and study intrinsic molecular effects, the role the molecular electronic test structure plays in the measurement must be determined. In particular, the properties and behavior of the interfaces within the test structure must be understood.

The properties of molecular monolayers on thin SiO_2 are of great interest for future hybrid Si-molecular device technologies [6,19–24]. In addition, the interface between organic materials and SiO_2 is critical for determining the device properties of organic electronic devices [25–31]. We have used electrical and optical characterization techniques to probe the top-metal/molecule interface and the molecule/SiO_2 interface in an effort to better understand the properties of these interfaces.

It is remarkably difficult to characterize the buried metal/monolayer/substrate interface *in situ*. Metal films

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become opaque to experimental probes (both optical and charge particle) at thicknesses on the order of 10 nm. Therefore, in order to analyze metal/monolayer systems, semi-transparent metal layers or destructive analysis is typically used. We utilized a novel, but straightforward, optical measurement, p-polarized backside reflection absorption infrared spectroscopy (pb-RAIRS) [32] to characterize alkane monolayers under bulk metal overlayers. pb-RAIRS is applicable to any metal/molecule/substrate system where the substrate is IR transparent, and is therefore ideal for the characterization of molecular monolayers on SiO_2 or directly attached to Si. The pb-RAIRS results are directly correlated with electrical characterization of capacitor structures on identically fabricated films. The agreement of the results from these very different characterization approaches increases our confidence in both the experimental results and our interpretations. We find that Au metal overlayers minimally perturb alkane monolayers formed on SiO_2 via silane reactions enabling the properties of the molecular monolayer to be electrically investigated in devices made from these systems. We characterized simple Au/alkane/SiO_2/Si capacitor structures by using dc-current–voltage (*IV*), ac-capacitance–voltage (*CV*), and ac-conductance–voltage (*GV*) both to relate these results with the pb-RAIRS results and to thoroughly characterize the electrical behavior of these molecular devices.

NDR and an accompanying hysteresis was observed in the *IV* measurements of Au/alkane/SiO_2/Si devices. It is unlikely that these intriguing effects are intrinsic to a simple alkane monolayer—which is expected to behave as a dielectric layer. The picture most consistent with the hysteresis observed in these Au/alkane/SiO_2/Si molecular junctions appears to be a model based upon charge trapping and detrapping at both the alkane/SiO_2 and the SiO_2/Si interfaces.

2. Experimental

Simple capacitor structures (Fig. 1) were fabricated for use in this investigation of the properties of interfaces in molecular monolayer based junctions. Three types of capacitors were formed, metal on alkane monolayers attached to SiO_2 on Si substrates (Fig. 1(a)), metal on alkane monolayers directly attached to Si(1 1 1) substrates (Fig. 1(c)), and no-molecule oxide controls (Fig. 1(b)). Alkane monolayers from the reaction of octadecanetrichlorosilane (OTS) were formed on thin thermal oxides (Thr). The substrates were either double side polished Si(1 1 1) wafers or single side polished Si(1 0 0) wafers. Both of the substrate orientations were lightly doped n-type (8 Ω cm to 12 Ω cm). The wafers first underwent an RCA clean. The resultant chemical oxide was stripped by buffered oxide etch prior to growth of the dry thermal oxide (800 °C with a 30 min densification anneal in N_2 at 1000 °C). In some cases, a short (~20 s) oxygen pulse was given at the start of the 1000 °C anneal to grow approximately two monolayers of SiO_2 in order to reform the Si/SiO_2 interface at this higher temperature.

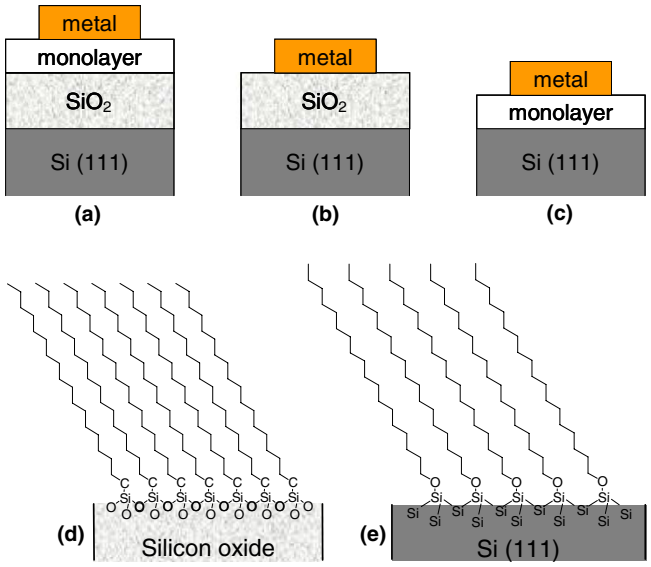

Fig. 1. (a)–(c) Schematic diagrams of the simple molecular-monolayer/SiO_2 junction capacitor devices used in this study. (d) Schematic of the alkane monolayer on thin SiO_2 formed from OTS, and (e) an alkoxy monolayer on Si(1 1 1) formed from octadecyl alcohol.

OTS was deposited by immersion of the substrates in a 2 mmol/L solution in hexadecane for 18 h. Immediately prior to immersion, the thermal oxide samples were cleaned by using a 5 min ultraviolet ozone (UVO) treatment on each side. The OTS processing was done in a class 10,000 clean room at a relative humidity of 45%. Upon removal from solution, the samples were cleaned to remove any OTS overlayers by ultrasonic treatment in chloroform, isopropyl alcohol, and 18 MΩ cm water. The samples were then annealed at 150 °C for 10 min. Thickness of the films was determined by spectroscopic ellipsometry (1.2–6.5 eV). The oxide thickness was determined from freshly UVO cleaned reference films by using a 3 phase model (air, SiO_2, Si) and the SiO_2 index of refraction reported by Brixner [33]. The OTS film thickness was determined from a 4 phase model (air, OTS, SiO_2, Si), fixing the oxide thickness at the value experimentally determined from the reference film, and assuming an index of 1.5 for the OTS layer. The alkane film thickness on the thermal oxide was typically 2.3 ± 0.1 nm, and sessile water contact angles ranged from 106° to 109°.

Alkoxy monolayers directly attached to Si were formed by the UV promotion of the reaction of dilute solutions (≈10 mmol/L) of octadecyl alcohol (OA) in CH_2Cl_2 with the H-terminated Si(1 1 1) surface (H–Si) as described previously [34]. The resultant films are dense and covalently bonded to the Si(1 1 1) substrate. Direct attachment was indicated by the elimination of the Si–H vibrational features. The films were moderately robust to oxidative attack, as no Si–O–Si features were observed during brief (24 h) exposure to air. The ellipsometric thickness of the

films was 2.2 ± 0.1 nm [35], with typical water contact angles of $102 \pm 1°$. The ellipsometric thickness indicates a slightly lower density for the directly attached films, compared to silanization, which has been attributed to packing constraints imposed by the Si lattice [34].

A backside-incidence Fourier-transform infrared-spectroscopy (FTIR) technique, pb-RAIRS [32], was used to investigate the interaction of the top-metallization with these alkane monolayers. In this technique (which is described in detail in Ref. [32]) the FTIR spectra of a molecular monolayer (or other thin films) is taken by using IR radiation incident on the backside of an IR-transparent substrate and the use of a thick metal layer on top of the monolayer that acts as an IR mirror (see the schematic in Fig. 2). Interactions between the metal overlayer and organic molecules can be investigated at this buried interface by careful comparison of transmission FTIR spectra of un-metallized monolayers mode with spectra obtained via pb-RAIRS of the metallized monolayers.

Two hundred nanometer metal films were deposited by direct thermal evaporation from a source ≈60 cm from the samples which are in good thermal contact with a large copper block to avoid excess heating during deposition. The deposition rate was (0.05–0.1) nm/s for the first ≈10 nm and then (0.5–0.8) nm/s for the remaining deposition. The evaporator base pressure prior to evaporation was $\approx 1.3 \times 10^{-4}$ Pa (10^{-6} Torr) and did not exceed $\approx 1.3 \times 10^{-3}$ Pa (10^{-5} Torr) during evaporation. Blanket metal films were deposited on nominally 15 mm × 25 mm samples for FTIR characterization. To investigate metals, such as Ti, which are poor IR reflectors, a stack of 9 nm Ti followed by 200 nm of Au was used to form the IR mirror necessary for the pb-RAIRS measurements.

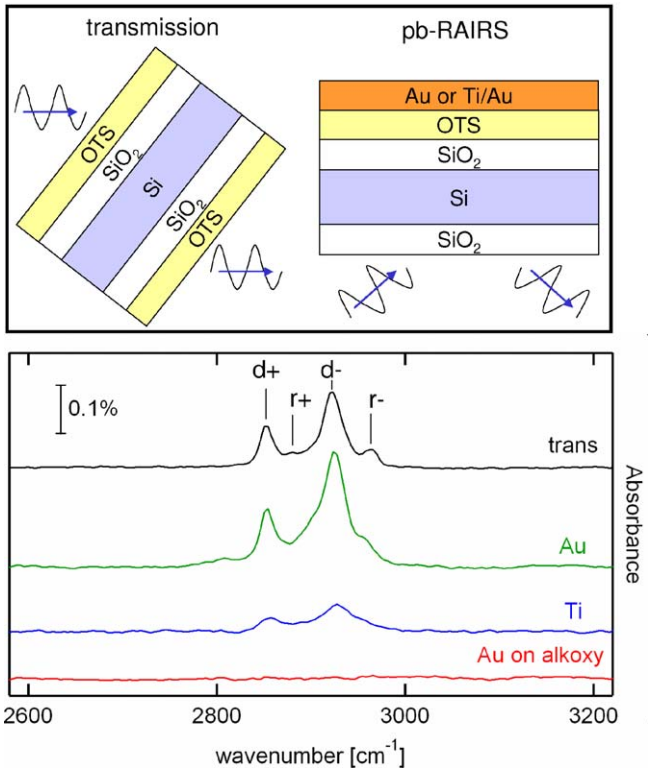

Fig. 2. Results of "backside" FTIR measurements. Green: Au on alkane/SiO_2. Blue: Ti on alkane/SiO_2. Red: Au on alkoxy/Si(1 1 1). Black line: transmission results before metal deposition. Peaks are labeled as described in the text. Schematic: experimental configurations for: (left) p-polarized Brewster's angle transmission and (right) the transparent sample with a deposited metal (Au or Ti/Au) IR-mirror configured for pb-RAIRS. The film thicknesses are not drawn to scale.

Reference samples were created by deposition of the metals directly on the thermal oxide films and on H–Si. The alkane films and metal depositions were performed via batch processing, providing a high degree of reproducibility. All IR spectra were recorded with a commercial Fourier transform (FT) instrument with a MCT detector at 8 cm^{-1} resolution. Five hundred and twelve scans were co-added for a total data acquisition time of ≈6.5 min. p-Polarized Brewster angle (≈73.7°) transmission spectra were acquired with a custom-built sample holder. p-Polarized, near-Brewster angle, backside reflection spectra were acquired with a commercial 80° reflection accessory. The actual reflection angle was determined to be ≈76.5°. For both measurements, wire grid polarizers (on either ZnSe or BaF_2 substrates) were used to define the polarization. Fig. 2 presents schematic diagrams for both the transmission and pb-RAIRS experimental configurations.

Arrays of 150 μm diameter Au dots were deposited via a shadow mask to create metal gate electrodes and form the capacitor structures for electrical characterization. The relatively large device area, the lack of a backside metal contact, and a dense spacing of the top-metal dots make these simple structures ideal for direct comparison with the pb-RAIRS measurements; however, these same features make these less than optimal electrical test structures. dc-current–voltage (IV), capacitance–voltage (CV), and ac-conductance–voltage (GV) measurements were carried out to electrically characterize these capacitor structures. Bias is applied to the top metal gate electrode and referenced with respect to the substrate (which remains at instrument ground). All electrical measurements were performed with a commercial low-electronic noise probe station.

3. Results

3.1. pb-RAIRS characterization

Fig. 2 shows a typical p-polarized Brewster angle transmission spectrum (black line) of a double side functionalized alkane (OTS) reference film on a thin (≈3.6 nm) thermal oxide (OTS/Thr). This spectrum is referenced to a freshly prepared H–Si sample and agrees with previous reports [36,37]. The methylene symmetric stretch (d+ near 2850 cm^{-1}) and asymmetric stretch (d-near 2920 cm^{-1}) are the dominant vibrational features in the C–H stretch region. The frequencies of these stretches indicate the degree of order of the alkane backbone [38,39], and the observed C–H frequencies for OTS/Thr (d+ ⇒ 2852 cm^{-1},

r+ ⇒ 2879 cm^{-1}, d− ⇒ 2921 cm^{-1}, and r− ⇒ 2964 cm^{-1}) are consistent with a nearly all-*trans*, crystalline film. The pb-RAIRS of the metallized films are also shown in Fig. 2. These spectra are referenced to the appropriate metal deposited on an H–Si sample. It should be noted that it is essential that the entrance faces (or backside) of the sample and reference be spectroscopically equivalent. For the Au and Ti:Au samples reported here, the entrance faces were prepared after metal deposition by a 5 min UVO clean, 18 MΩ cm water rinse, 3 min UVO clean, 18 MΩ cm water rinse, HF strip, and 30 min UVO oxide growth.

The results (Fig. 2) indicate that Au has a minimal interaction with alkane monolayers on SiO_2. The d− frequency shifts slightly to higher wavenumbers upon metal deposition, indicative of slight disordering of the chains due to weak interactions with the metal. Ti, on the other hand, causes significant changes in the vibrational spectra. The intensities of all bands are severely reduced indicative of the partial consumption of the alkane monolayer, and the d− frequency appears at 2926 cm^{-1}, characteristic of a disordered liquid. The severe attenuation and disruption of the film is consistent with earlier studies of Ti on alkanes [40,41] and suggests a chemical interaction between the Ti and the hydrocarbon, probably due to Ti carbide formation [41] partially consuming the monolayer and disordering the film. Top metals (such as Au) appear to completely displace alkoxy monolayers directly assembled on Si(1 1 1) since there is no evidence for organic material remaining under the deposited metals. These pb-RAIRS results indicate that reactive top metals, such as Ti are likely to aggressively degrade underlying organic monolayers, while alkoxy monolayers directly attached to Si are completely displaced by top-metallization. Thus, systems consisting of Au top-metal structures on OTS/Thr are the most likely of those in this study from which to form devices in which the current path includes the organic monolayer of interest enabling its electrical characterization.

3.2. IV and CV characterization

Based on the pb-RAIRS results, simple Au on OTS/Thr capacitor structures were electrically characterized. Fig. 3 shows shows typical dc *IV* results for a Au/OTS/Thr device and a no-molecule Au/Thr control device. Devices containing OTS have significantly lower current for a given gate metal bias indicating that the monolayer of OTS remains intact under the Au metal blocking the current. The *CV* data shown in Fig. 4 also indicates that the OTS monolayer remains and is acting as a good dielectric layer. The accumulation capacitance (i.e., the capacitance for positive biases) is lower in the Au/OTS/Thr devices with respect to the no-molecule Au/Thr control devices. The combined dielectric stack of the alkane monolayer on SiO_2 is a thicker total dielectric giving rise to the observed lower accumulation capacitance. Thus, both the dc-*IV* and *CV* indicate that the OTS is present and behaving as a dielectric

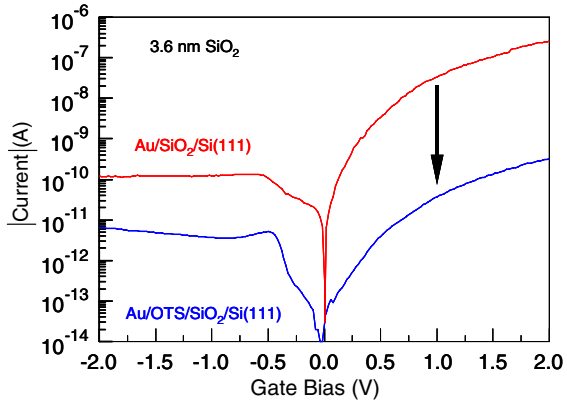

Fig. 3. Current–voltage curves for Au/OTS/SiO_2 and Au/SiO_2 (3.6 nm) devices.

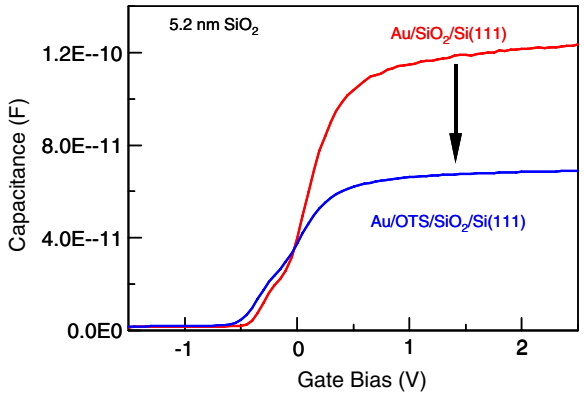

Fig. 4. Capacitance–voltage curves (1 kHz) for Au/OTS/SiO_2 and Au/SiO_2 (5.2 nm) devices.

film in agreement with the pb-RAIRS data. The dielectric thickness [42] of the alkane films can be extracted from the *CV* measurements by presuming two capacitors in series, $1/C_{total} = 1/C_{SiO_2} + 1/C_{alkane}$ where C_{total} is the experimentally measured accumulation capacitance of the OTS/Thr device, the values for C_{SiO_2} are experimentally determined from the thermal oxide control samples, and C_{alkane} is the capacitance of the alkane monolayer. The dielectric thickness of the alkane layer is found by presuming a parallel plate capacitance model ($C_{alkane} = \kappa\varepsilon_0 A/d$ where ε_0 is the permittivity of free space, A the area of the device, d the dielectric thickness) and the dielectric constant, $\kappa = 2.5$ (at 1 kHz) for the alkane monolayer. When this analysis is done, it is typically found that the derived thickness of OTS monolayers under Au is ≈1.5 nm (or ≈0.7 nm less than the original ellipsometric thickness). While slightly thinner, this thickness is in relatively good agreement with the ellipsometric thickness again indicating that the Au overlayer is not significantly damaging the alkane monolayer. This is in contrast to Ti overlayers which partially consume the organic material leading to electrically-derived thicknesses that are typically only 0.7 nm (≈1.5 nm less than the values measured ellipsometrically prior to metal deposition [7,32]).

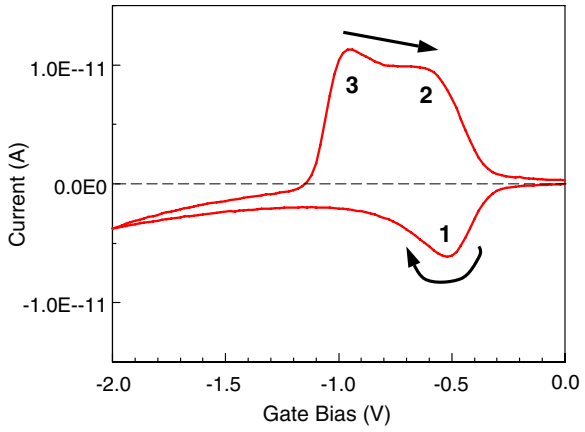

Fig. 5. Current–voltage curves for Au/OTS/SiO_2 (≈3.6 nm)/Si(1 1 1) devices acquired from 0 V to −2 V back to 0 V at a bias sweep rate of 50 mV/s. Peaks are labeled 1–3 for ease of identification. Typical "two-peak" behavior on the return −2 V to 0 V bias sweep.

There is a dramatic hysteresis observed at approximately −0.5 V in the *IV* curves obtained for OTS/Thr samples as illustrated in Fig. 5. This feature appears as a negative-differential-resistance (NDR) peak (with a room temperature peak to valley ratio that can be greater than 6) on the initial negative direction sweep from 0 V to negative biases (typically −2 V or −2.5 V). On the return sweep (from negative bias to 0 V) devices typically show two positive current peaks (Fig. 5), although it should be noted that in a very small subset of devices only a single peak is observed on the return sweep. These hysteresis peaks in these solid state devices are qualitatively very similar in appearance to electrochemical cyclic voltammetry curves [43], and it is tempting to refer to them in electrochemical terms. The single peak pair consisting of peaks 1 and 2 looks very much like the cyclic voltammogram of a reversible redox reaction; however, the voltage difference between the position of the forward and reverse peaks is larger (≈120 mV) and of the opposite sign of the ≈59 mV peak spacing expected for an ideal, reversible, single-electron transfer redox reaction at room temperature. Peak 3 on the other hand, which does not have an accompanying negative direction peak, is similar in appearance to a peak arising from a slow, irreversible effect. This hysteresis has been observed for many different fabrication runs and for devices with alkane layers on oxide films ranging from (3.5 to 5.2) nm thick grown on both Si(1 1 1) and Si(1 0 0) substrates. It should be noted that the experimental observability of this hysteresis is strongly dependent upon the total current in these devices. In devices where the current density is too high (due to a very thin oxide layer such as a native oxide) or when the current density is very low (as in devices with a thick SiO_2 layer) the hysteresis is not observed.

The *IV* hysteresis peaks have a strong sweep rate dependence as illustrated in Fig. 6. The peak amplitude increases with sweep rate dependence for all three peaks. While the position of the peak pair at lower absolute biases (peaks 1 and 2) is invariant for different sweep rates, the position

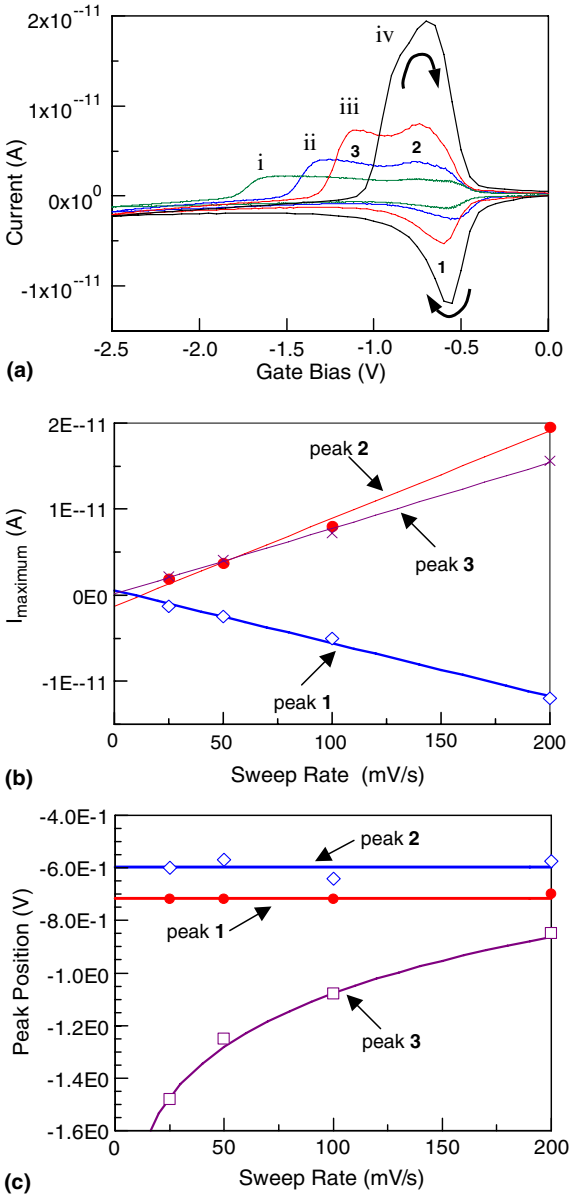

Fig. 6. Gate bias sweep rate dependence of the *IV* hysteresis peaks for a typical Au/OTS/SiO_2 (≈5.2 nm)/Si(1 1 1) device. (a) *IV* curves for bias sweep rates of (25, 50, 100, and 200) mV/s for traces i–iv, respectively. Peaks are labeled 1–3 for ease of identification. (b) The peak current and linear fits for each of the peaks (1—blue, 2—red, and 3—purple) as a function of sweep rate. (c) The bias voltage position for the current maximum for each of the peaks; lines are guides for the eye.

of peak 3 strongly depends on the sweep rate, shifting to more negative biases at slower sweep rates.

In order to further elucidate the behavior of these alkane/SiO_2-based molecular junctions, the frequency dependence of the capacitance and ac-conductance was measured. Typical results are shown in Fig. 7. Recall that in order to be compatible with the pb-RAIRS measurements, these devices are made on lightly doped-Si substrates, and there is no backside processing to improve electrical contact to the substrates. Therefore, there is a relatively large resistance in series with the molecular junction.

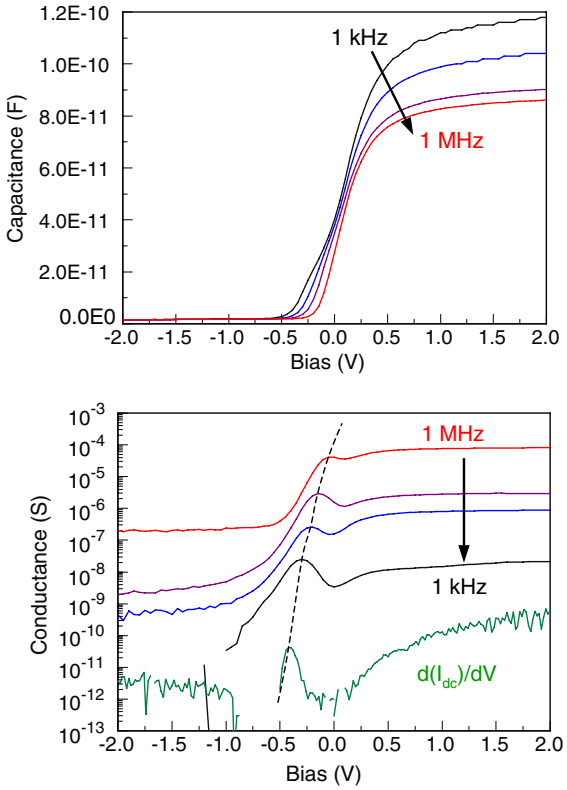

Fig. 7. Capacitance–voltage (top) and conductance–voltage (bottom) data at frequencies 1 kHz (black), 10 kHz (blue), 100 kHz (purple), and 1 MHz (red) for a Au/OTS/SiO_2 (5.2 nm) device. Dashed line is a guide to the eye.

This series resistance is the cause for the observed lowering of the accumulation capacitance with increasing frequency, as well as the increasing "steps" in the ac-conductance with increasing frequency. The large conductance peak and the slight "shoulder" on the *CV* curves qualitatively indicates that there are a large number of interface traps at the Si/SiO_2 interface in these samples [44]. While the presence of the large series resistance makes a detailed quantitative interface trap analysis of the conductance (G) as a function of frequency (ω) unfeasible [45], G/ω curves indicate that the density of interface traps in these samples is in the range of $(1–5)\times10^{11}$ cm^{-2}. It should be noted that this trap density is approximately three orders of magnitude lower than the density of the molecules [46], $\cong5\times10^{14}$ cm^{-2}, in these devices. The dc-conductance obtained by taking the local derivative of the dc-*IV* curve is also shown in Fig. 7. The position of the dc-conductance peak (only peak 1 is shown in this unidirectional data) is suggestive that the dc- and ac-conductance peaks are correlated.

4. Discussion

It is most likely that charge trapping in defect states at the Si/SiO_2 and the SiO_2/alkane interfaces in the dielectric stack of these devices is the underlaying cause for the observed hysteresis. Charging of the trap states at a given energy during the initial negative-going bias sweep gives rise to the NDR peak (peak 1). This charge remains trapped in the defect states until it is released on the return positive-going bias sweep in peaks 2 and 3. The large density of interface traps (D_{it}) as indicated by the analysis of the ac-conductance as a function of frequency and the correlation (shown in Fig. 7) of the voltage position of the dc-*GV* peak (peak 1) with the position of the ac-*GV* peak indicate that Si/SiO_2 interface traps are playing a role in the observed hysteresis. However, it is unlikely that charging of Si/SiO_2 interface traps is the mechanism giving rise to all three of the observed peaks.

The sweep rate dependence of the three peaks (shown in Fig. 6) provides further insights into the underlying mechanics. The maximum current of all three peaks depends linearly on the voltage sweep rate (Fig. 6(b)). This linear dependence implies a capacitive relationship between the gate and the source of the *IV* peaks [47]. The slope of the maximum current as a function of sweep rate is the associated capacitance which is found to be $\approx6.2\times10^{-11}$ F, $\approx1.0\times10^{-10}$ F, and $\approx7.6\times10^{-11}$ F for peaks 1–3, respectively. As Fig. 6(c) shows, the positions of peaks 1 and 2 do not change with voltage sweep rate, and there is a fixed separation of ≈120 meV between them. Peak 3, however, has a very strong sweep rate dependence indicating that this peak is arising from a different mechanism with much slower dynamics than the one associated with peaks 1 and 2. The slow dynamics of peak 3 are evidence that it is not due to conventional Si/SiO_2 interface traps which are known to be in rapid electrical communication with the Si substrate [48]. Charge traps that are spatially separated from the Si/SiO_2 interface yet close enough to exchange charge with the underlying Si (often known as border traps) respond more slowly [48,49]. Charge trapping defects at the SiO_2/alkane interface should be classified among these border traps for the thin oxide layers in this study. Thus, the slow dynamics of peak 3 as indicated by the strong sweep rate dependence support a model for trapped charges at the remote SiO_2/alkane interface as the fundamental mechanism for this peak. Furthermore, fast dynamics of the peaks 1 and 2 pair combined with the large number of Si/SiO_2 interface traps as determined via *GV* analysis are evidence that Si/SiO_2 interface traps are the most likely basis for this pair of peaks.

This hypothesis of trapped charges at the two SiO_2 interfaces is empirically supported by further experimental data. Multiple fabrication runs were performed to make series of molecular junctions with oxide thicknesses from 3.5 to 5.2 nm. Typically, the oxides were grown at 800 °C in oxygen (with a 1000 °C N_2 densification anneal) on Si(1 1 1) substrates. The lower temperature was used to allow better thickness control for these relatively thin films. In an effort to determine if the *IV* hysteresis is specific to the oxides grown on Si(1 1 1) under these conditions, devices were fabricated from oxides grown on Si(1 0 0) and from oxides where a short O_2 growth at 1000 °C followed the 800 °C growth (in order to reform the Si/SiO_2 interface by growing ≈2 monolayers of SiO_2 at this elevated temperature). For

each oxide growth condition and substrate orientation, no-molecule control capacitors were made as well as OTS/Thr molecular junction devices. For all successful device fabrication runs [50], hysteresis was observed in the OTS/Thr molecular junction devices for each of these growth conditions and substrates. No trend was found with respect to substrate orientation or growth temperature. The large, dramatic *IV* hysteresis (such as Figs. 5, 6(a) and 8(a)) is observed only in devices containing alkane monolayers. As shown in Fig. 8(b), a small hysteresis is sometimes observed in control samples. Such *IV* hysteresis is only observed for a small subset of the control sample fabrication runs, and it is small in amplitude as Fig. 8(b) illustrates. The position of the hysteresis peaks in the control samples coincides with the position of peaks 1 and 2 in the OTS/Thr samples supporting the argument that this peak-pair is due to Si/SiO_2 interface traps. The fact that peak 3 is clearly observed only in OTS/Thr samples supports a trap mechanism at the remote interface alkane/SiO_2 interface.

While we have taken great care to optimize our device fabrication approach, we suspect that the extensive wet chemistry and UVO treatments associated with the OTS monolayer deposition process can damage the starting SiO_2 which may be the reason that the peaks 1 and 2 pair are more strongly observed in OTS/Thr samples. In previous work [32] we found that a widely used air–plasma approach to preparing SiO_2 for OTS deposition, while leading to excellent alkane monolayers, was extremely detrimental to the SiO_2 and lead to unusable electrical devices.

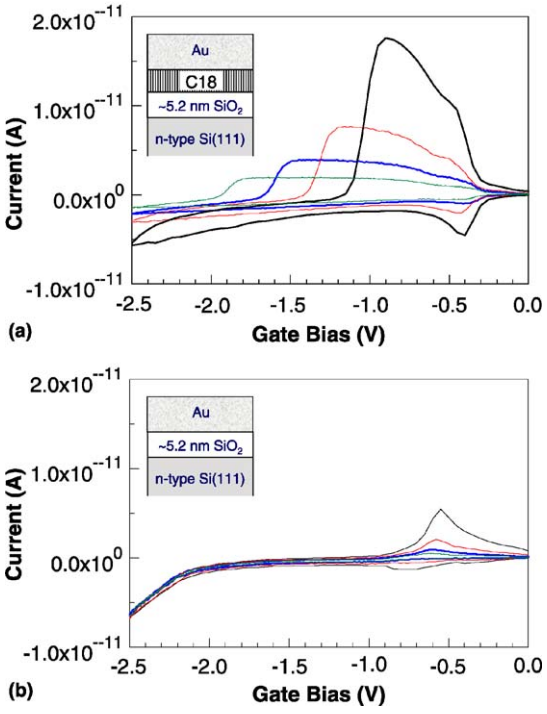

Fig. 8. Hysteretic current–voltage behavior for a typical device containing an Au/OTS/SiO_2 (≈5.2 nm)/Si(1 1 1) molecular junction (a) and for a simultaneously fabricated no-molecule "control" device: Au/SiO_2 (≈5.2 nm)/Si(1 1 1) (b). *IV* curves acquired for bias sweep rates of (25, 50, 100, and 200) mV/s for green, blue, red, and black curves, respectively. Inserts schematically show device structures.

5. Conclusions

In summary, we have correlated the results of pb-RAIRS with electrical device measurements (such as *IV* and *CV*) to spectroscopically and electrically characterize devices containing a molecular-monolayer/SiO_2 junction. Both the optical and electrical measurements indicate that alkanes attached to SiO_2 via silane chemistry are relatively "robust" to Au deposition. On the other hand, a reactive metal, Ti, severely degrades the alkane monolayer, additionally, it appears that metals displace alkoxy monolayers directly attached to Si(1 1 1). An intriguing NDR peak and *IV* hysteresis is observed in *IV* measurements of devices based upon Au/alkane/SiO_2 junctions. It is unlikely that this effect is intrinsic to the molecule itself, but it is arising from the properties of the interfaces in the sample. It is most likely that one set of peaks (the peaks 1 and 2 pair) is arising due to charge trapping defects at the Si/SiO_2 interface. It is also likely that charge trapping and detrapping at the SiO_2/alkane interface is the underlying source of the third, bias sweep rate dependent, peak (peak 3) observed in the *IV* measurements. These data illustrate the critical importance of understanding and controlling the nature of interfaces in molecular electronic devices.

Towards the goal of observing and characterizing electrical device behavior based upon intrinsic molecular effects, the role of test structures and their interfaces must be understood and eventually effectively controlled. Furthermore, these data illustrate the need for researchers to grow and use silicon complementary metal–oxide–semiconductor (CMOS) quality oxides and not allow them to degrade during molecular assembly and further processing. The dielectrics and other materials used when fabricating molecular devices must be made at the highest level of control to avoid impurities and defects which are likely to lead to spurious device behavior. As is well known in the CMOS manufacturing community, defects can easily degrade and even dominate the performance of MOS devices. It is likely that molecular and organic devices need to be made with at least the same levels of purity and control that are used in the successful fabrication of silicon CMOS devices in order to create devices in which to characterize intrinsic molecular effects.

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