10 V programmable Josephson voltage standard circuits using NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stacks

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Using NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stack technology we have demonstrated a programmable Josephson voltage standard chip that operates up to 10.16 V output voltage cooled with a two-stage Gifford–McMahon cryocooler. The circuit uses double-junction stacks, where two junctions are fabricated in each stack, in order to integrate 327 680 junctions into a 15.3 mm $\times$ 15.3 mm chip. A 1-to-32 microwave distribution circuit is also integrated on the chip. The chip is divided into 22 cells, which perform as an 11-bit digital-to-analog converter. The 21 working cells include 307 200 junctions biased with 16 GHz microwaves at 10.2 K that generated flat voltage steps with current margins greater than 1 mA, which indicates good uniformity of the stacked junctions. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2167789]

A programmable Josephson voltage standard (PJVS) using superconductor/normal-metal/superconductor (SNS) Josephson junction arrays is promising for the next-generation Josephson voltage standard because of its programmable output voltage, short voltage-settling time (less than 1 ms), and large operating margins (greater than 1 mA). To date, a number of researchers have proposed or demonstrated the use of damped SNS junctions for a PJVS system.[1–4] Benz *et al.*[5] first demonstrated a programmable 1 V Josephson voltage standard using Nb/PdAu/Nb junctions with an I_cR_n product of about 30 μV, corresponding to a characteristic frequency of 15 GHz. Schulze *et al.*[6] reported the fabrication of junction arrays for a 10 V PJVS with a 200 μA step width, which included 69 120 Nb/AlO$_x$/Al/AlO$_x$/Nb junctions. Chong *et al.*[7] demonstrated 3.87 V maximum output voltage with practical operating current margins greater than 1 mA using triple-stacked junctions with $MoSi_2$ barriers.

The National Institute of Advanced Industrial Science and Technology (AIST) and the National Institute of Standards and Technology (NIST) have cooperated in the development of NbN-based digital-to-analog converters (DACs) for PJVS systems.[8] The main advantage of NbN-based DACs is that they can operate at 10 K, which is accesible with practical cryocoolers.

Previously, we reported operation of an eight-bit DAC using a compact refrigeration system.[9] We have previously reported the fabrication of an 11-bit DAC for 10 V PJVSs that had two major problems.[10] One problem was very low fabrication yield, and another was poor microwave characteristics. The width of the constant-voltage step was less than 0.5 mA, and it required a large microwave power greater than 1 W. In this letter, we describe a fully operational 10 V programmable Josephson voltage standard with 1 mA current margins operating at 10.2 K on a cryocooler.

The fabrication process for the PJVS chip was simplified compared with the previous design.[8] Previously, we planarized both the base and counter electrode layers in order to avoid significant reduction of the wiring critical current I_{max}. The wiring critical current was typically about 15 mA. It has been reported that junction heating in the array also reduces the wiring critical current for the array, and that a wide base electrode would improve the wiring critical current.[11] Therefore, we increased the width of the base electrode from 6 μm to 17 μm, which improved I_{max} to greater than 20 mA. Thus, by using wide base electrodes we were able to skip the first planarization without reduction of I_{max}.

Another significant factor that reduced our yield was poor insulation performance of our SiO_2 films, which caused short circuits between metal layers. The major cause of the pin holes in the SiO_2 films was found to be contamination of the surface of the base electrode due to high humidity in our clean room. We observed that our fabrication yield depended on the season, namely that the fabrication yield dropped during the rainy season (the beginning of the summer in Japan). After replacing the air conditioner in the clean room, we can now reliably maintain relative humidity at 50%.

Finally, the fabrication yield was improved by use of an interdigitated capacitor instead of a parallel-plate capacitor that was susceptible to oxide pin holes. From electromagnetic field simulations, we found that the low-pass filter using the interdigitated capacitor had some resonant peaks in the frequency dependence of the reflection coefficient S_{11}.[12] We compared the frequency dependence of the current margin for fabricated simpler 1 V PJVS chips using the two types of capacitors. The frequency dependence for the parallel-plate capacitor was a little flatter than that for the interdigitated capacitor over the frequency range from 10 to 20 GHz. However, this result cannot be a serious disadvantage for the interdigitated capacitor because the microwave frequency will not be changed over a wide range when the PJVS chips are used for dc-voltage applications.

Figure 1 shows the equivalent circuit of the 11-bit DAC design for the 10 V PJVS, and Fig. 2 shows a photograph of the fabricated chip. Each array contains 5120 NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stacks inter-

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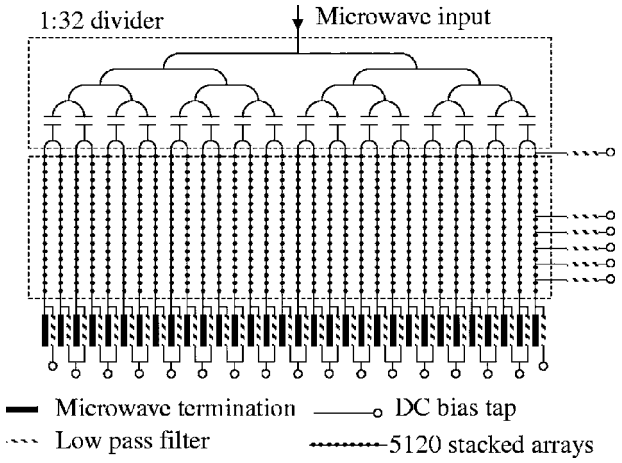

FIG. 1. Equivalent circuit of an 11-bit DAC for a programmable Josephson voltage standard.

connected with NbN wiring. For DAC operation, the total series-connected array containing 163 840 stacks was divided into 22 cells with 23 bias taps. The number of stacks in each of the 22 cells was: 160, 160, 320, 640, 1280, 2560, 5120, and 15 cells with 10 240 stacks. The 23 bias taps are connected to the array through 16 GHz quarter-wavelength transformers for microwave blocking. The size of the junctions is 3.4 μm $\times$ 3.4 μm and the critical current density was about 7×10^8 A/m^2. The DAC chip is designed to use one tap to launch the microwave power and the microwave power was equally split to 32 arrays through a coplanar network circuit and dc blocking capacitors. A 16 GHz quarter-wavelength coplanar waveguide (CPW) with a specific impedance of 36 Ω was connected to two 50 Ω CPWs, which functioned as a two-way splitter. Five consecutive stages of this two-way splitter were connected in series in order to divide the microwave power to 32 arrays. The center linewidth and the space between the center and outer conductors for both the 36 and 50 Ω CPWs were optimized using the

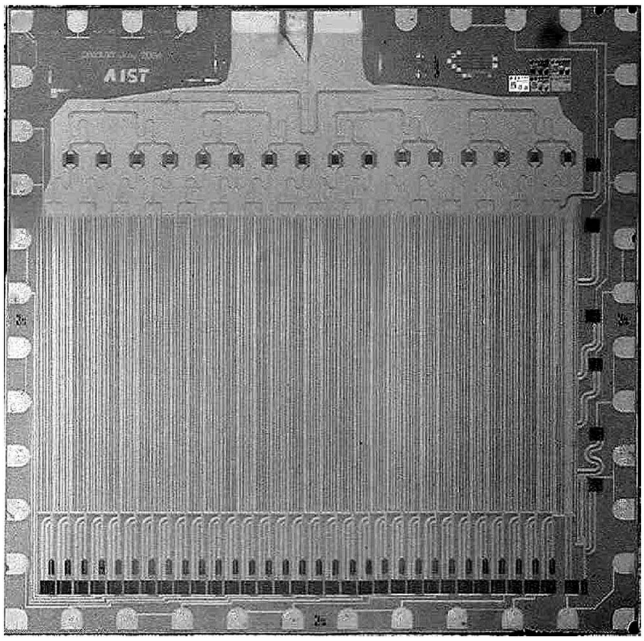

FIG. 2. Photograph of a NbN-based 11-bit DAC chip for a programmable Josephson voltage standard. 163 840 NbN/TiN$_x$/NbN/TiN$_x$/NbN double-junction stacks are integrated on a 15.3 mm $\times$ 15.3 mm chip.

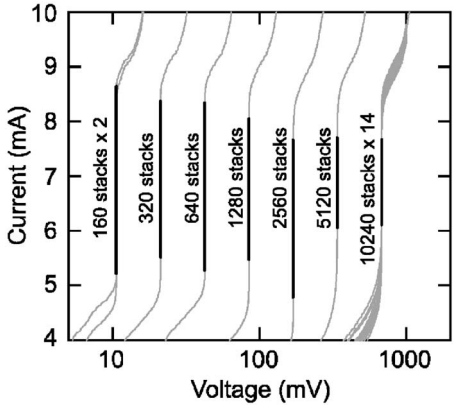

FIG. 3. $I-V$ characteristics for 21 array cells from the 11 bit 10 V PJVS circuit using TiN$_x$ double-junction stack arrays. All $I-V$s were measured with the same power of 400 mW at 16 GHz. The chip was cooled by a refrigerator to 10.2 K. The multiple overlapping $I-V$s with the largest voltage step correspond to the 14 array cells, each having 20 480 junctions. The remaining cell (cell No. 13) was not dc biased because it did not generate a flat step.

electromagnetic field simulation taking into account the kinetic inductance of the NbN film.[12] This optimization of the specific impedance significantly reduced the microwave power required to achieve steps with 1 mA current range from 1 W to 400 mW.[10]

Figure 3 shows current-voltage (I-V) characteristics for all working cells with 16 GHz microwaves at 10.2 K, showing the 11-bit DAC function. Table I summarizes the minimum current, maximum current, and current margins for the first step, which correspond to the black lines in Fig. 3. The multiple I-Vs with the largest voltage step correspond to the 14 working array cells with 20 480 junctions each. The 13th cell was not used because it did not produce a flat step. The chip was cooled to 10.2 K with a two-stage Gifford–McMahon cryocooler, which had a refrigeration capacity of 1.4 W at 10 K. The applied microwave power was about 400 mW, measured at the output of the microwave source. The 21 cells, which included 307 200 junctions, generated a flat step of about 10.16 V. Fortunately, the 13th cell that did not generate a flat step remained superconducting when no dc-bias current was supplied. Therefore, this defect of the cell did not prevent DAC functionality apart from a slightly smaller maximum output voltage. The 327 680 junctions

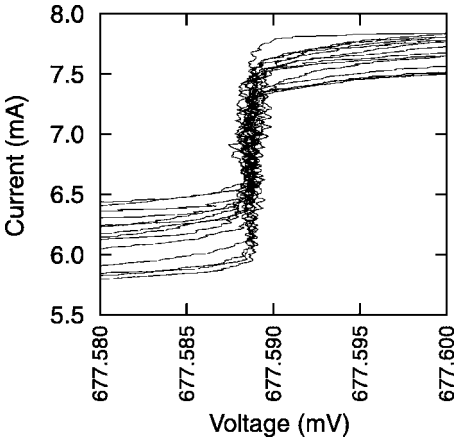

FIG. 4. Overlaid $I-V$ curves for the largest 14 cells, showing overlapping $n=1$ steps that are flat within the measurement noise.

TABLE I. Array cell characteristics. There are two junctions in each stack.

Cell number	Number of stacks	The first step (mA)		
		Min	Max	Width
1	640	5.25	8.22	2.97
2	160	5.29	8.53	3.24
3	160	5.21	7.98	2.77
4	320	5.60	8.26	2.66
5	1280	5.59	7.90	2.31
6	2560	4.87	7.57	2.70
7	5120	6.10	7.70	1.60
8	10 240	6.18	7.62	1.44
9	10 240	6.11	7.63	1.52
10	10 240	6.46	7.53	1.07
11	10 240	6.41	7.63	1.22
12	10 240	6.22	7.76	1.54
13	10 240	···	···	0.00
14	10 240	5.89	7.62	1.73
15	10 240	6.48	7.76	1.28
16	10 240	6.38	7.78	1.40
17	10 240	6.29	7.67	1.38
18	10 240	6.29	7.62	1.33
19	10 240	6.22	7.37	1.15
20	10 240	5.87	7.52	1.65
21	10 240	5.90	7.37	1.47
22	10 240	5.97	7.46	1.49

were expected to generate an output voltage of 10.81 V when biased with 16 GHz microwaves, while the fully functional 21 cells of 307 200 junctions generated an output voltage of 10.16 V.

Figure 4 shows the magnification of the steps for the largest 14 cells. The nonfunctioning cell number 13 is not displayed. The current width was determined with a 10 μV voltage threshold on the nanovoltmeter's 1 V scale. Because the dc-bias current sources were not designed for precision measurement, the current source contained both 50 Hz noise related to the cryocooler compressor and high-frequency noise from a computer bus. These noise sources are likely the cause of the 2 μV wide noise on the steps. To confirm the flatness of these steps, the bias current circuits should be isolated electrically from the compressor and the computer; this measurement will be completed and discussed elsewhere in more detail.

All cells except the 13th cell have practical current margins greater than 1 mA, which indicates sufficient uniformity for the double-junction stacks. The cause of the defect in cell 13 might be a patterning defect that produced a junction of different area, resulting in a voltage step with a very different current range from the other junctions. At present, it is difficult to produce a perfect chip because of limited fabrication yield. Fortunately, even without one array we can still produce accurate programmable voltage over the full range from −10.16 V to +10.16 V.

In summary, we have successfully demonstrated an 11-bit digital-to-analog converter circuit for a programmable Josephson voltage standard with a 10.16 V maximum output voltage, having practical operating current margins greater than 1 mA. Furthermore, this performance was demonstrated under liquid-helium-free conditions by use of a cryocooler operating at 10.2 K. The 327 680 Josephson junctions with TiN_x barriers and a 1-to-32 microwave distribution circuit were integrated on a 15.3 mm × 15.3 mm chip, and sufficient uniformity and fabrication yield were obtained. If fabrication yield can be improved, this programmable Josephson voltage standard circuit might be a practical replacement for conventional Josephson voltage standards.

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