

Reverse short channel effects in high- k gated nMOSFETs

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Abstract

Anomalous threshold voltage roll-up behavior, commonly referred as reverse short channel effect (RSCE), has been observed in high- k (HfO₂ on SiON buffer, Al₂O₃ on SiON buffer) gated submicron nMOSFETs, while the SiO₂ or SiON control samples show normal short channel effect (SCE) behavior. The possible causes such as inhomogeneous channel doping profile and gate oxide thickness variation near S/D ends have been ruled out. The results indicate that interface trap density that depends on channel length is the main cause of the RSCE observed here. In addition, oxide charge also plays a role.

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1. Introduction

The reverse short channel effect (RSCE) refers to an increased threshold voltage (V_{th}) with decreasing channel length (L_{ch}) in MOSFETs. It has commonly been attributed to laterally inhomogeneous channel doping profile, generated by enhanced diffusion at the source/drain (S/D) ends that in turn can be mediated by a variety of possible mechanisms [1–3]. However, here we present strong evidence that the RSCE observed in HfO₂-gated nMOSFETs is not due to dopant redistribution; instead, it can be consistently explained by effects of interface traps and oxide charge [4,5].

2. Device details and experiments

nMOSFETs were fabricated by using a conventional CMOS process flow with a poly-Si gate [6]. The HfO₂

gate dielectric was fabricated by atomic layer deposition of HfO₂ on an ultra-thin layer (<1 nm) of pre-grown silicon oxynitride (SiON). In addition, control samples with SiON gate dielectrics were fabricated for comparison. A standard method was used to measure the MOSFET I - V characteristics, from which we determined V_{th} , the midgap voltage (V_{mg}) [7], and the subthreshold slope, which is related to interface trap density.

3. Results and discussion

A strong RSCE was found in nMOSFETs (i.e. V_{th} increases with moderately short channel decreasing) with HfO₂ gate dielectric (thickness 30 and 60 Å), whereas the SiON control samples exhibit a normal short channel effect (SCE), as shown in Fig. 1. One should note that the devices are not aggressively short channel MOSFETs; in particular, halo implant was skipped for process simplicity. For devices with a channel length less than 0.4 μm, the roll-off of V_{th} as normal SCE was observed. These data are not shown, because it is not our main focus here.

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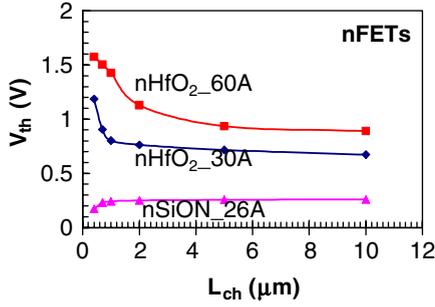


Fig. 1. Threshold voltage (V_{th}) as a function of channel length (L_{ch}) for nMOSFETs, showing RSCE for samples gated with 30 Å HfO₂ and 60 Å HfO₂ (both deposited on ultra-thin SiON buffer layer), but a normal SCE for control samples with SiON as gate dielectric.

As mentioned in the introduction, the RSCE in SiO₂ gated MOSFETs is commonly attributed to certain processing steps which enhance dopant diffusion and hence increase channel dopant concentration near the source/drain (S/D) junctions [1,2]. The inhomogeneous dopant concentration is thought to underlay the increase in V_{th} seen for shorter channel devices [3]. In order to test this hypothesis in our devices, we looked for evidence of inhomogeneous dopant concentration in the channel by measuring the dependence of threshold voltage on substrate bias; representative results for nMOSFETs with 60 Å HfO₂ are shown in Fig. 2. To a good approximation, the linear lines of V_{th} versus square root of substrate bias for three different L_{ch} are parallel; therefore we found no indication that a significant dependence of the channel dopant concentration on L_{ch} exists (see Eqs. (31) and (32) in [8]) simplified version is shown as Eq. (1):

$$V_T \propto \sqrt{N_A(V_{bs} + C)}, \quad (1)$$

The good linear regression fits of C_{ox} (C_{inv}) versus L_{ch} for SiON and 30 Å HfO₂ shown in Fig. 3 indicate that there is a uniform oxide thickness for FETs of all

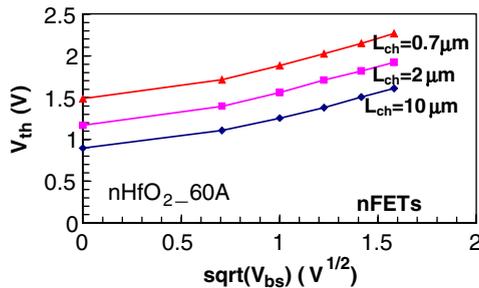


Fig. 2. V_{th} as a function of the square root of substrate bias (V_{bs}) for nMOSFETs (60 Å HfO₂) with three different L_{ch} . The parallel lines indicate that there is no significant dependence of the effective channel doping concentration on channel length.

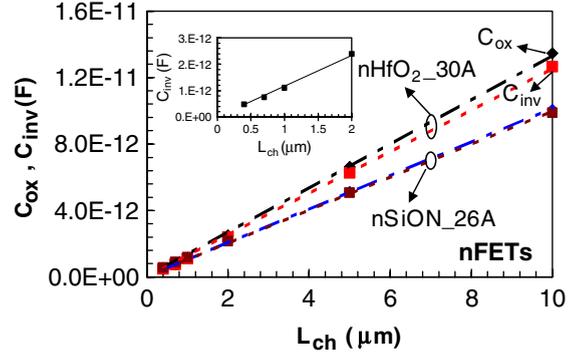


Fig. 3. C_{ox} (C_{inv}) is a linear function of L_{ch} for nMOSFETs with SiON and 30 Å HfO₂. The inset plots C_{inv} vs. L_{ch} ($\leq 2 \mu\text{m}$) for 30 Å HfO₂ case.

tested L_{ch} , hence there is no significant evidence that the oxide thicknesses near the S/D region is greater than in the channel region. Thickness inhomogeneity may then be ruled out as a possible cause of RSCE. The normal SCE seen in the SiON control samples is also consistent with this conclusion.

To determine the cause of the RSCE in our samples, we measured the subthreshold characteristics: for the HfO₂ nMOSFET. The subthreshold swing (SS) and V_{th} were found to depend on L_{ch} in a similar fashion (Fig. 4).

Since the SS is proportional to the interface trap density [8] in the weak inversion region as shown in Eq. (2),

$$SS = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{min} + qD_{it}}{C_{ox}} \right), \quad (2)$$

this result strongly suggests that interface traps play an important role in causing the RSCE. More specifically, the shorter the channel, the higher the interface-trap density, which in turn causes a higher V_{th} . Note that the SS measurement, being a quasi-DC measurement,

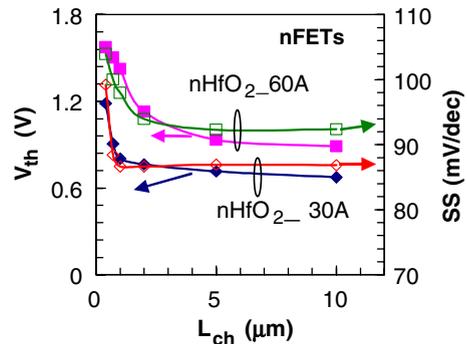


Fig. 4. V_{th} and SS as a function of L_{ch} of nMOSFETs (30 and 60 Å HfO₂, respectively). Both, V_{th} and SS, show similar dependence on L_{ch} .

includes effects of not only fast interface traps but also of border traps (slow states) and even bulk traps.

To investigate the possible role of oxide charge, we estimated V_{mg} , from the subthreshold characteristic according to the procedure described in [7], where it was shown that the shift in V_{mg} is proportional to the oxide charge density N_{ox} , whereas the shift in V_{th} is a combination of N_{it} and N_{ox} induced effects, as shown in Eqs. (3) and (4):

$$N_{it} \approx \frac{[(V_{th} - V_{mg}) - (V_{th} - V_{mg})_{ideal}]C_{ox}}{qA}, \quad (3)$$

$$N_{ox} \approx \frac{(V_{mg} - V_{mg(ideal)})C_{ox}}{qA}. \quad (4)$$

The shifts in V_{mg} and V_{th} were found to be dependent on L_{ch} in a similar fashion (Fig. 5). This suggests that oxide charge (negative charge) does contribute to the RSEC. However the shift magnitude is significantly smaller for V_{mg} than for V_{th} , hence the contribution of oxide charges to the RSCE is likely to be smaller than that of interface traps.

We hypothesize that process-induced damage near the channel edges which locally increases N_{it} and N_{ox} could be a cause for the channel length dependence. For shorter channel devices, the damaged section constitutes a larger portion of the total channel, and therefore increases V_{th} . The subsequent annealing process was capable of healing this process-induced damage in the SiON control samples, whereas it was far less effective in the high- k gated MOSFETs. Such a difference is likely, since SiON and high- k materials are intrinsically different. Therefore the control SiON samples do not exhibit the RSCE, instead showing normal SCE. A qualitatively similar RSCE has been observed for Al_2O_3 -gated nMOSFETs as well (Fig. 6). The physical thickness of Al_2O_3 layer is approximately 50 Å, underly-

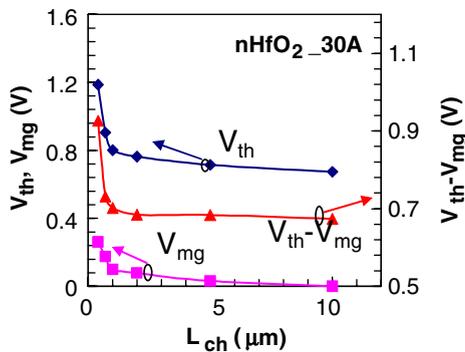


Fig. 5. V_{th} , V_{mg} , and their difference ($V_{th}-V_{mg}$, right hand ordinate) as a function of L_{ch} of nMOSFETs (30 Å HfO_2), suggesting that both interface traps and oxide charge may contribute to the RSCE.

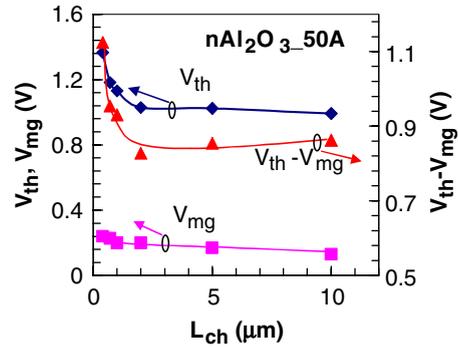


Fig. 6. Pilot data obtained in 50 Å Al_2O_3 gated nFETs. Again, interface traps are the major cause of the RSCE whereas oxide charge play minor role here.

ing SiON buffer layer is less than 1 nm. A similar explanation may be given for these samples, the interface traps are the major cause whereas oxide charges seem to play role here as well, but not significantly.

4. Summary

The RSCE has been observed in high- k gated samples (HfO_2 on SiON buffer, Al_2O_3 on SiON buffer), while control samples (SiO_2 or SiON) show normal SCE. An inhomogeneous channel doping profile generated by dopant enhancement near the S/D extension region has been ruled out as a possible cause; instead, strong evidence indicates that channel length dependent interface traps may be the major cause of the RSCE in high- k gated MOSFETs.

Acknowledgements

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