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Enhanced Channel Modulation in Dual-Gated Silicon Nanowire Transistors

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ABSTRACT

Dual-gated silicon nanowire (SiNW) field-effect transistors (FETs) have been fabricated by using electron-beam lithography. SiNW devices (W $\approx$ 60 nm) exhibit an on/off current ratio greater than 10^6, which is more than 3 orders of magnitude higher than that of control devices prepared simultaneously having a large channel width ($\sim$5 μm). In addition, by changing the local energy-band profile of the SiNW channel, the top gate is found to suppress ambipolar conduction effectively, which is one of the factors limiting the use of nanotube or nanowire FETs for complimentary logic applications. Two-dimensional numerical simulations show that the gate-induced electrostatic control is improved as the channel width of the FETs decreases. Therefore, enhanced channel modulations can be achieved in these dual-gated SiNW devices.

Because of their one-dimensional structure, high surface-to-volume ratio, and small size, silicon nanowires (SiNWs)[1,2] and carbon nanotubes (CNTs)[3,4] have attracted much attention recently for their potential use in high-density electronics[5,6] as well as in high-performance sensors.[7,8] For these applications, the most fundamental and important structures made of SiNWs or CNTs are field-effect transistors (FETs) with direct metal contacts forming the source and drain.[1−8] Because there is no intentional doping process involved for the source/drain metal contacts, NWFETs and CNTFETs typically exhibit ambipolar characteristics. Both hole and electron conduction occurs depending on the gate bias.[9] However, the ambipolar behavior is undesirable for complementary metal-oxide-semiconductor (CMOS) logic applications. An experimental study of single asymmetric back-gated CNTFET structures[10] and a theoretical study on double top-gated CNTFET structures[11] have been reported, which describe efforts to suppress the ambipolar behavior in CNTFETs. Si-based Schottky barrier FETs with large channel widths ($\sim$10 μm)[12] and SiNW-based single electron transistors with doped sources and drains[13,14] have been studied extensively. However, there has been little experimental work to date on the properties of nanoscale channel Schottky barrier SiNWFETs, and an increased gate coupling for these devices has yet to be reported. In this work, we report dual-gated SiNWFETs, where a back gate accumulates or inverts the entire channel and a top gate locally controls the energy-band profile of the channel. Our results show that the top gate can control the ambipolar conduction in SiNWFETs effectively with an improved on/off current ratio.

Figure 1a shows a schematic diagram of the fabricated dual-gated SiNWFET structure. The starting materials were (100)-oriented silicon-on-insulator (SOI) wafers, which have a 50-nm Si layer on top of a 100-nm thermally grown buried oxide (BOX) layer. Both the Si layer and the substrate are *p*-type with boron doping of $\sim 2 \times 10^{15}$ cm^{-3}. Prior to the contact metal deposition, the wafer was cleaned by using the standard RCA procedure followed by HF/H_2O (1:10). The source and drain metal electrodes were formed by evaporating first Ti and then Au onto the hydrogen-terminated silicon layer. The source/drain electrodes were defined further by a photolithography and etch process. The SiNW channel was then patterned between the source and drain metals by electron beam lithography (EBL). Thus, the source and drain electrodes act as alignment marks for EBL as well as a self-aligned mask.[15] Reactive ion etching (RIE) defines the SiNW channel together with the source and drain areas. Note that there is no additional doping step for the source/drain region and no subsequent thermal annealing was applied. A 2-nm-thick native oxide layer was formed on the SiNW surface. The thickness of the top native oxide layer, SOI, and BOX layers have been determined by using spectroscopic ellipsometric mapping characterization over a control wafer processed simultaneously with an area of 10 $\times$ 10 cm^2. The top Au gate was defined by EBL and a lift-off process based upon a bilayer of polymethyl methacrylate (PMMA) layer and copolymer-PMMA (co-PMMA). The SiNWFETs reported in this letter have channel widths of 60 nm, top gate lengths of 2 μm, and channel lengths of 28 μm. Control FETs with larger channel widths of 5 μm were fabricated simultaneously as reference devices. Scanning electron microscopy (SEM) images of the SiNW channel

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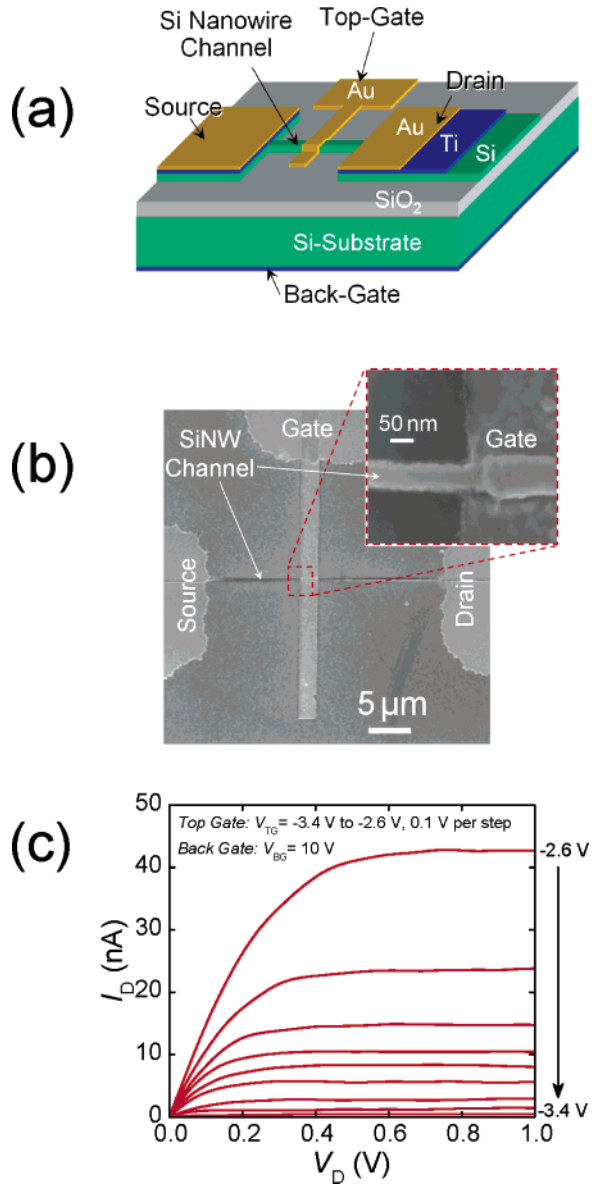

Figure 1. (a) Schematic device structure of a dual-gated SiNWFET. (b) Scanning electron micrography (SEM) image of the fabricated SiNWFET. The inset shows the channel and top-gate region. (c) Drain output ($I_D - V_D$) characteristics of a SiNWFET. The top-gate voltage (V_{TG}) was varied from −3.4 to −2.6 V with 0.1 V per step. The back-gate voltage (V_{BG}) was set as 10 V to turn the channel on with electrons inverted.

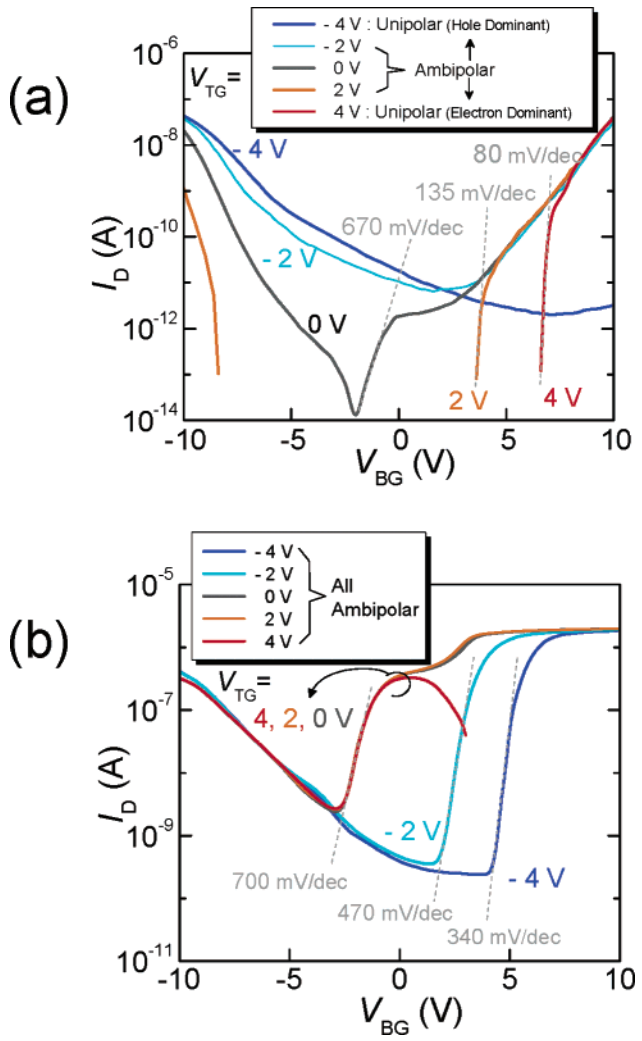

Figure 2. I_D-V_{BG} characteristics of the (a) SiNWFET and (b) Control FET for $V_D = 0.5$ V.

and the gate region of a typical SiNWFEET are shown in Figure 1b. The devices are all dual-gated structures having both a top metal gate and a backside substrate gate. The back gate can be biased to form a conducting channel of either accumulated holes or inversion electrons. The back gate also controls the shape of the Schottky barriers between the source/drain and the channel. The top gate, however, is biased independently and changes the local potential of the channel under it.

The drain current versus drain voltage (I_D-V_D) output characteristics of a representative NWFET are shown in Figure 1c for top-gate voltages (V_{TG}) varying from −3.4 to −2.6 V with 0.1 V per step. The back-gate voltage (V_{BG}) was set at 10 V to turn the channel on with inversion electrons. The measured I_D-V_D characteristics show well-saturated behavior with top-gate induced transconductances ($g_m = dI_D/dV_{TG}$) up to 0.3 μS. This corresponds to a transconductance of 5 mS/mm and, assuming negligible contact resistance ($R_C \cong 0$),[16] can be converted to 1400 mS/mm for a decreased channel length of 80 nm and a channel width of 60 nm.[17]

Figure 2 shows back-gate transfer characteristics (I_D-V_{BG}) under different top-gate conditions for the SiNWFETs and control FETs. V_{BG} was varied from −10 V to +10 V for a drain voltage of $V_D = 0.5$ V. When the top gate voltage is zero ($V_{TG} = 0$), the FETs behave as typical back-gate devices exhibiting ambipolar characteristics with both *p*- and *n*-type behavior. When positive or negative bias is applied to the top gate, as shown in Figure 2a, the hole or electron current component of the SiNW channel can be selectively controlled. Suppressing one of the two conduction components in the ambipolar characteristics is necessary in order to realize improved on-state characteristics. In contrast to the NWFET, the control FET shows ambipolar conduction for the rage of V_{TG} from −8 to 4 V irrespective of the given top-gate

bias. In this case, as shown in Figure 2b, the top-gate control between −4 to 4 V is not sufficient to deplete the channel region electrostatically to tune it to unipolar conduction. The control FET exhibits only threshold voltage (V_{th}) shifts for the electron conduction, whereas the current level and V_{th} remain unchanged for hole conduction.

For the case of SiNWFETs, in addition to the separate charge injection control, the energy-band profile offset induced by the top gate results in improved subthreshold properties. As shown in Figure 2a, the subthreshold slope S $\approx$ dV_{BG}/d(log I_D) for the electron conduction improves significantly from 670 mV/dec[18] to 80 mV/dec for changing V_{TG} from 0 to 4 V. For the case of control FETs, as shown in Figure 2b, the improvement in subthreshold slope of electron conduction for increased top-gate bias is significantly smaller (from 700 to 340 mV/dec) than that of NWFET (from 670 to 80 mV/dec). In a conventional MOSFET, the subthreshold current is dominated by diffusion through the source/drain-to-the channel $p-n$ junction. This results in a limitation of the minimum subthreshold slope ($S = kT/q$ ln 10 $\approx$ 60 mV/dec) at 300 K. Recent theoretical[19] and experimental[20] work explored the possibility of subthreshold swing values less than 60 mV/dec in Schottky barrier source/drain transistor structures. However, these results still require further confirmation. Experimentally, it is also found here that the on/off current ratio I_{ON}/I_{OFF} for the control FET ($\sim 10^3$) is about 3 orders of magnitude lower than that for SiNWFETs ($>10^6$). The lower I_{OFF} values for NWFETs would lead to improved power dissipation.

To understand the channel transport properties of FETs, the corresponding band diagrams along the nanowire channel from source to drain, for different V_{TG} and V_{BG} conditions, are shown as solid lines in Figure 3. The following discussion first considers the case of zero top-gate bias. The switching behavior of the devices is determined by the Schottky barrier at the source/drain contacts as shown as the dotted band-gap profiles in Figure 3. For low back-gate bias voltages ($V_{BG} \approx 0$) corresponding to the "off state" the drain current I_D is very small and is due primarily to the thermionic emission of carriers across the barriers. The thermionic current level is related to the Schottky barrier height as $I \approx \exp(-q\Phi_B/kT)$, where q is the electronic charge, k is the Boltzmann constant, and T is the absolute temperature in Kelvin. At high back-gate voltages, tunneling of electrons or holes may occur as the width of the barrier decreases, turning the device to the on state. For a positive back gate bias ($V_{BG} > 0$), an inversion electron channel can be formed, and the width of the barrier decreases for increased positive drain voltages (V_D). Thus, the channel is turned on because of electrons injected from the drain (see the dotted band-gap profiles in Figure 3c and d). Similarly, an accumulation channel is formed for a negative back-gate bias ($V_{BG} < 0$). For negative back-gate bias, the tunneling hole barrier becomes more transparent as the drain voltage becomes more negative. As shown as the dotted potential schematics in Figure 3a and b, the hole conduction from the drain dominates in this case.

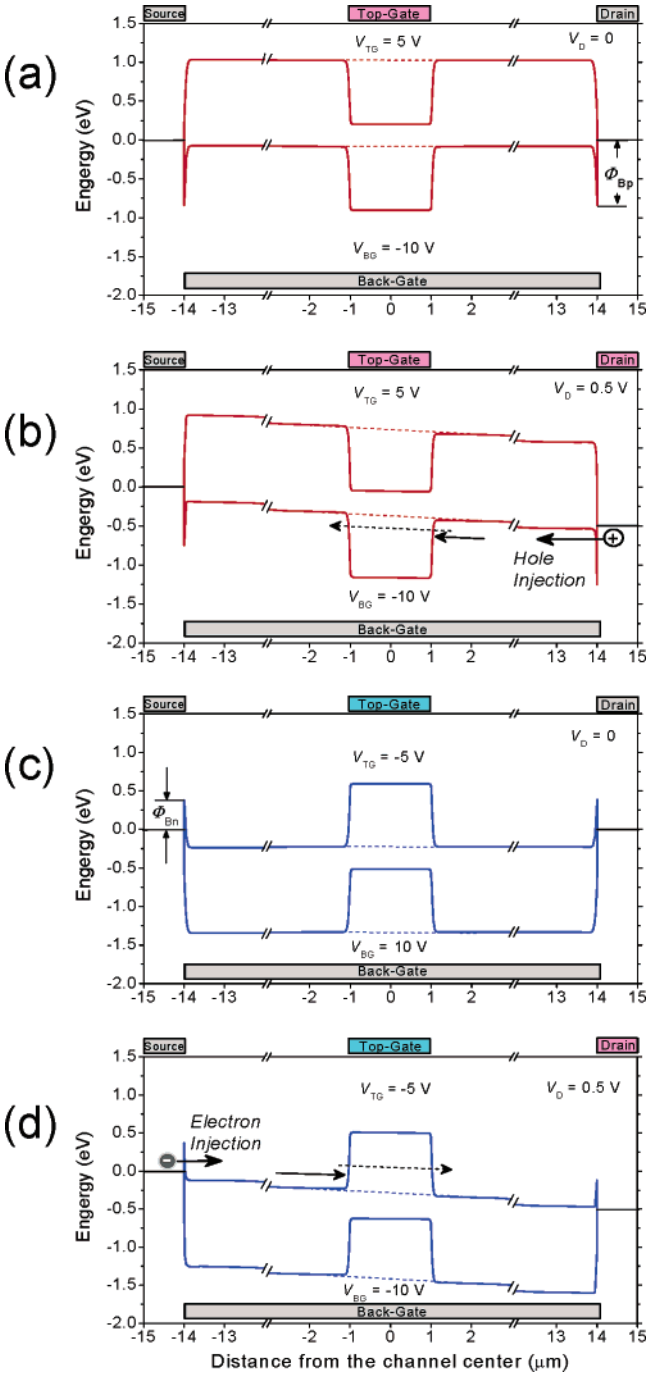

Figure 3. Energy-band profile from source to drain of a dual-gated SiNWFET for different bias conditions: the dotted profiles represent zero-biased top-gate V_{TG} condition, whereas solid lines correspond to positive V_{TG} for a and b, and negative V_{TG} for c and d, respectively. (a) Negative back-gate bias $V_{BG} = -10$ V without drain bias $V_D = 0$, (b) positive drain bias $V_D = 0.5$ V, (c) positive back gate bias $V_{BG} = 10$ V without drain bias $V_D = 0$, and (d) positive drain bias $V_D = 0.5$ V.

By applying a positive bias to the top gate ($V_{TG} > 0$) for an accumulated channel with a negatively biased back gate ($V_{BG} < 0$), as shown in the solid band gap profile in Figure 3a and b, the energy-band profile in the top-gated channel region is lowered so that the channel is depleted. The band diagram shown in Figure 3 suggests that the back gate has negligible influence on the top-gated channel region.[21] The

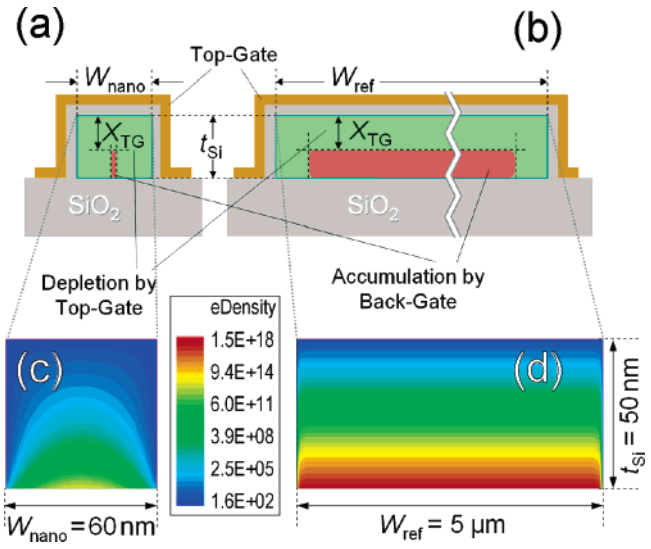

Figure 4. Schematic diagram of the channel cross-section area where the top gate is covered for (a) a SiNWFET and (b) a Control FET. The 1D depletion width (X_{TG}) shows a possible full depletion by lateral narrowing in SiNWFET. Simulated electron distributions of the 2D channel cross-section area biased into inversion when $V_{BG} - V_{TG} = 7.5$ V for (c) a SiNWFET and (d) a control FET. Note that the expansion of the depletion in the simulation is more remarkable because of the 2D coupling effect, and the 1D calculations underestimate the depletion in a SiNWET.

barrier profile of the middle of the channel bends down, and the injected holes at the drain side are blocked by the top-gate induced barrier, which results in the suppression of the hole currents. Thus, mainly electron transport is allowed, and the hole current (I_D for $V_{BG} < 0$) decreases for increasing V_{TG} from -4 V to $+4$ V as shown in Figure 2a. The same discussion holds for biasing the top gate voltage negatively ($V_{TG} < 0$) to suppress the electron conduction, when the back gate is positively biased ($V_{BG} < 0$) to invert the channel. For a negatively biased V_{TG}, the top-gated channel region is depleted, and the band-gap profile of the top-gated region is bent up with respect to the rest of the channel with inverted electrons, which forms a barrier for electrons (see Figure 3c). Therefore, the hole transport dominates the channel conduction, and the electron current (I_D for $V_{BG} > 0$) diminishes. It is not the Schottky barrier thickness at the source or drain that restricts the hole transport but the band bending in the middle of the channel induced by the top gate. Note that as shown is Figure 2, far better top-gate control is observed for SiNWFETs than for control FETs.

To better understand the effect of the channel size on the control of transport properties of the dual-gated FETs using the top gate, we have performed two-dimensional simulations. The effect of the top gate can be understood by investigating the depletion depth. In a thin layer of Si channel, the full depletion of the channel occurs when the gate-induced depletion width (in this case X_{TG} in Figure 4a and b) reaches the thickness of the Si layer ($X_{TG} \geq t_{Si}$). However, for a narrow channel device, the condition for full depletion involves not only the channel thickness (t_{Si}) but also the channel width (W_{nano}). This is because the channel can be fully depleted laterally when the depletion from each side wall merges ($2X_{TG} \geq W_{nano}$).

We have used a 2D numerical simulator, ISE-TCAD,[22] to simulate the channel structure and examine this effect further. Figure 4c and d shows the simulated electron distributions in the channel biased into inversion by using the back gate and depletion with the top gate. Note that the potential difference between the top gate and the back gate ($V_{BG} - V_{TG}$) is 7.5 V without assuming any interface states or fixed oxide charges. As shown in Figure 4a and b, the simple estimation of the 1D depletion width (X_{TG}) from three sides of the SiNW underestimates the channel depletion effect, but still shows an easier channel shut-off by the depletion in NWFETs than in control FETs. The 2D numerical simulations (Figure 4c) show an expansion of the depletion over the 2D channel cross-section. This suggests that the so-called 2D coupling effect[23] should be considered because the lateral depletion regions of the side wall cooperate to reduce the effective doping of the channel in such a way that the resulting gate depletion region from the top can be extended further. However, the full depletion does not occur before X_{TG} reaches the vertical dimension (equal to the channel thickness, t_{Si}) for larger channel widths as shown for the case of control FET in Figure 4d. Therefore, an electron channel with a free electron density as high as $1.5 \times 10^{18}/\text{cm}^3$ exists in the control FET, whereas the highest electron density for the NWFET is only $\sim 10^{14}/\text{cm}^3$ under the same gate bias conditions.

In conclusion, we have demonstrated experimentally that the change in the local electrostatic depletion in SiNWFETs enhances their device properties significantly. Unipolar action can be controlled in dual-gated SiNWFETs, allowing the devices to be either *n*-type or *p*-type by the polarity of the applied biases on the top gate. This manipulation is crucial for using SiNWs in CMOS-type logic applications. In addition, the SiNWFET ($W \approx 60$ nm) exhibited more than 3 orders of magnitude improvement in on/off current ratio when compared to control devices prepared simultaneously ($W_{ref} \approx 5$ μm). The conduction mechanism in a dual-gated SiNWFETs is attributed to the top-gate-bias-induced changes in the local energy-band profile. By using 2D numerical simulations, we have confirmed that the electrostatic control over current flow is enhanced in a SiNW compared to larger channel width devices. The results demonstrate that the proposed dual-gate SiNWFET structure can manipulate and improve the device characteristics effectively.

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(16) This may suggest a g_m value approximately 2−5 times higher than those of state-of-the-art planar silicon FETs and FinFETs with channel lengths of 50−100 nm. Our simple conversion neglects the contribution of increased contact resistance (R_C), which would lead to a g_m value less than 1400 mS/mm. However, note that the source/drain contact of our FET is a Schottky barrier only when the device is "off", and it shows Ohmic or tunneling contact properties when the device is "on". It has been reported that by using silicide source/drains and nanoscale channel lengths, Schottky barrier FETs may eliminate the parasitic resistance and thus may deliver more on current than the conventional MOSFET.
(17) It is worth noting that our devices are fully compatible with the silicon CMOS technology and that the parameter values extracted from the device can be optimized further by decreasing the channel length as a simple modification. For example, by using a selective scaling for the given channel length (L) and channel width (W), the transconductances are scaled with a factor of W/L, while keeping the thickness (t_{Si}) constant. Therefore, a g_m value of 0.3 μS for $L = 28$ μm corresponds to a g_m value of 1400 mS/mm for $L = 100$ nm. Also at the same time, by using a scaling factor for 1/3 for the buried oxide thickness, the back-bias voltage of 10 can be adjusted to be ∼3.3 V as typical operating voltages.
(18) We followed the extraction of S after ref 20, where S is extracted between the current level of 10^{-12} and 10^{-15} A. Note that CNTFETs and NWFETs often exhibit a nonlinear subthreshold slope, as in poly-Si thin-film transistors. This is ascribed to a competing mechanism between tunneling and thermionic emission, which is different from the conventional MOSFET. Above all, our results clearly show qualitative improvement of the top-gate control for a SiNWFET compared to conrol FETs.
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(21) Assuming that the entire voltage drop for the gate bias is across the oxide layer, the electric field across the top oxide layer (E_{TOX}) is 50 times higher than that across the buried oxide (E_{BOX}) for the same top- and back-gate bias conditions ($V = V_{TG} = V_{BG}$) because the electric field can be simply estimated as $E_{TOX} = V/t_{TOX}$ for top-gate oxide thickness $t_{TOX} \approx 2$ nm and buried-gate oxide t_{BOX} (∼100 nm) as measured by a spectroscopic ellipsometer. Note that this estimation ignores the voltage drops associated with the interface states and the charge screening at electrode interfaces. However, inclusion of these effects would increase the ratio of E_{TOX}/E_{BOX}, which indicates even improved control by the top gate, because the additional voltage drop across the back substrate gate should be higher than that across the top gate.
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