
SEMICONDUCTOR MICROELECTRONICS AND NANOELECTRONICS PROGRAMS

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References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 2003; and to the 2004 update.

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2003 edition*. International SEMATECH: Austin, TX, 2003.

This document is available on-line at URL: <http://public.itrs.net> or in printed copy by contacting International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, ITRS department 860-008, phone: (512) 356-3500.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

CONTENTS

Welcome and Introduction	v
Office of Microelectronics Programs Organization	vii
Lithography Metrology Program	1
Metrology Supporting Deep Ultraviolet Lithography	3
Metrology Supporting Extreme Ultraviolet Lithography	9
Polymer Photoresist Fundamentals for Next-Generation Lithography	15
Critical Dimension and Overlay Metrology Program	21
Wafer-Level and Mask Critical Dimension Metrology	22
Scanning Electron-Based Dimensional Metrology	23
Scanning Probe Microscope-Based Dimensional Metrology	29
Small Angle X-Ray Scattering-Based Dimensional Metrology	35
Electrical-Based Dimensional Metrology and Critical Dimension Reference Material Development	39
Optical-Based Photomask Dimensional Metrology	45
Model-Based Linewidth Metrology	49
Atom-Based Dimensional Metrology	53
Wafer-Level and Overlay Metrology	57
Front-End Processing Metrology Program	63
Wafer and Chuck Flatness Metrology	65
Modeling, Measurements, and Standards for Wafer Surface Inspection	69
Front-End Materials Characterization	73
Chemical Metrology of Materials	83
Interconnect and Packaging Metrology Program	87
Atomic Layer Deposition – Process, Models, and Metrology	89
Superconformal Deposition Copper and Advanced Interconnect Materials	93
Nanoporous Thin-Film Metrology for Low- κ Dielectric Materials	97
Interconnect Materials and Reliability Metrology	101
Basic Materials Properties	103
Interconnect Test Structures	111
Wire Bonding to Copper/Low- κ Semiconductor Devices	115
Solders and Solderability Measurements for Microelectronics	117
Process Metrology Program	121
Gas Property Data and Flow Standards for Improved Gas Delivery Systems	123
Low Concentration of Humidity Standards	127
Temperature Measurements and Standards for Rapid Semiconductor Processing	133
Plasma Process Metrology	137

Analysis Tools and Techniques Program	143
Thin-Film X-Ray Metrology For Microelectronics.....	145
Electron Microscope Tomography of Electronic Materials.....	151
High-Resolution Microcalorimeter X-ray Spectrometer for Chemical Analysis	153
Device Design and Characterization Program	159
Device Characterization and Reliability	161
Nanoelectronic Device Metrology.....	165
Power Semiconductor Device Metrology	169
Organic Electronics Metrology.....	173
NIST Advanced Measurement Laboratory Nanofab	177
System Design and Test Metrology Program	179
Metrology for System-on-a-Chip (SoC).....	181
BioElectronics Metrology.....	185
At-Speed Test of Digital Integrated Circuits.....	189
Thermal Measurements and Packaging Reliability	193
Manufacturing Support Program	199
Factory Time Synchronization Standards Development for e-Manufacturing.....	201
Engineering Chain Management in the Semiconductor Industry.....	203
NIST/SEMATECH e-Handbook of Statistical Methods.....	205
Abbreviations and Acronyms	206
Technical Contacts	210

WELCOME AND INTRODUCTION

WELCOME

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

HISTORICAL PERSPECTIVE

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of sixty with a \$6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

INDUSTRIAL METROLOGY NEEDS

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a \$12.0 million budget in fiscal year 2004, and a \$12.2 million budget in fiscal year 2005.

FOSTERING NIST's RELATIONSHIPS WITH THE INDUSTRY

NIST's relationships with the SIA, SEMATECH and its subsidiary, International SEMATECH Manufacturing Initiative (ISMI), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP and NIST Laboratories represents NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. NIST staff are also active in the semiconductor standards development work of the American Society for Testing and Materials (ASTM), the International National Electronics Manufacturers Initiative (iNEMI), the Electronic Industries Association (EIA), the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

LEARN MORE ABOUT SEMICONDUCTOR METROLOGY AT NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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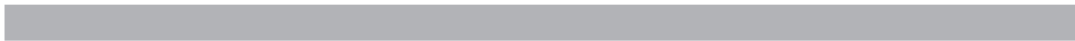
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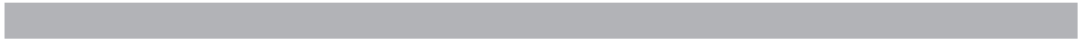


From left to right: Stephen Knight, Michele Buckley, and Joaquin Martinez de Pinillos.



LITHOGRAPHY METROLOGY PROGRAM

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are in leading edge manufacturing facilities. The first 193 nm immersion lithography tools will be shipped later this year. Development of exposure tools operating at 157 nm are “on hold” while high index fluids and lens materials for 193 nm tools are under intense exploration to develop high numerical aperture systems. If successful, the 157 nm tool generation may be bypassed. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials, and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.



METROLOGY SUPPORTING DEEP ULTRAVIOLET LITHOGRAPHY

GOALS

Develop solutions to key optical metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

CUSTOMER NEEDS

Increasing information technology requirements have created a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate optical measurements at DUV laser wavelengths.

A new lithography technology, immersion lithography, depends on incorporating a high-index fluid between the optical system and the wafer and possibly also incorporating a high-index material as the last lens element. Design and development of 193 nm and 157 nm immersion lithographies require accurate measurements of the index properties of the potential 193 nm and 157 nm fluids and materials.

To support these efforts, the National Institute of Standards and Technology (NIST), with SEMATECH support, has developed a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential solutions for lithographic systems are discussed in the 2003 International Technology Roadmap for Semiconductors and its 2004 Update. On page 1 of the Update Lithography section, "...193 nm wavelength exposure systems, including 193 nm immersion systems... [may become] dominant solutions for the next two nodes... Furthermore, immersion lithography appears as potential solution at the 32 nm

and 22 nm nodes." The need for metrology in lithography is discussed on page 32 of the 2003 Metrology section on Integrated Metrology and Advanced Process Control, "Metrology plays a key role in productivity gains made through advanced process control (APC), particularly as the trend toward integrated metrology—from offline to inline to in situ techniques—enables a richer, more powerful spectrum of process control strategies."

TECHNICAL STRATEGY

■ High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5 ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has begun constructing a new state-of-the-art minimum-deviation system and separately developed another system based on a VUV FT spectrometer and a synchrotron radiation as a continuum source (see Fig. 1). Both of these systems will enable measurements to an accuracy of 1 ppm, and will be used to characterize high-index lens materials and immersion fluids for 193 nm and 157 nm lithography systems.

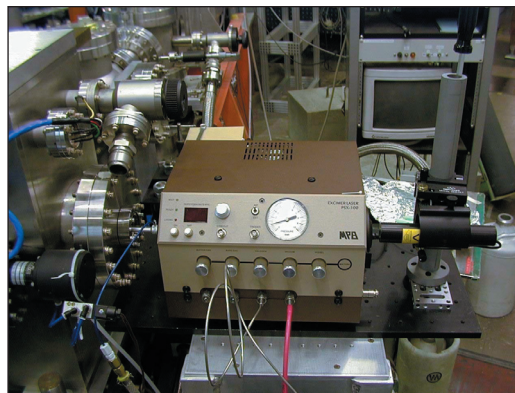


Figure 1. Facility for detector VUV radiation damage study using synchrotron radiation from SURF and a 157 nm excimer laser.

Technical Contacts:

J. H. Burnett
M. Dowell

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild, Massachusetts Institute of Technology's Lincoln Laboratory

DELIVERABLES: Index measurement capability with 1 ppm uncertainty. 3Q 2005

■ Taking full advantage of the potential resolution gain with immersion lithography may require using high-index materials as the last lens element, though as yet no such material has been demonstrated at 193 nm. To address this need we have begun, with the support of SEMATECH, a survey of candidate materials. We have identified several classes of oxide-based materials which have very high indices (near 2.0) at this wavelength and which can in principle be highly transparent at 193 nm. We have begun a program of complete optical characterization measurements of these materials to identify the most promising candidates and to assess their potential for development for lithography optics.

DELIVERABLES: Fully characterize the 193 nm optical properties of leading candidate high-index materials. 4Q 2005

■ An absolute light source in the DUV range based on synchrotron radiation using NIST's Synchrotron Ultraviolet Radiation Facility (SURF III) has been established using a dedicated beamline at SURF III. The flux of the DUV radiation at this beamline can be known to very high accuracy through the well established equations governing the behavior of the synchrotron radiation. The beamline is designed for customer calibration of a variety of DUV instruments to assist the development of the DUV lithography such as monochromators, discharge lamps, and irradiance meters. The spectral range covers all of the current important wavelengths for semiconductor industry such at 248 nm, 193 nm, 157 nm and even down to 13 nm. The uncertainty of such calibration is better than 1% in the case of deuterium lamp calibration.

DELIVERABLES: Provide customer DUV calibration for discharge lamps, monochromators, and irradiance meters using SURF III source-based beamline with highest accuracy. 4Q 2005

Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF (248 nm) and ArF (193 nm), and more recently F_2 (157 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs

of the optical lithography community, we have developed primary standards and associated measurement systems at 193 nm and 248 nm, and 157 nm. Figure 2 shows the excimer laser calibration facility.

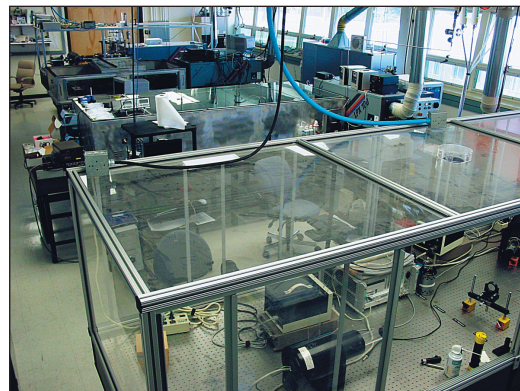


Figure 2. Laboratory for excimer laser energy and power meter calibrations, with measurement systems for 248 nm, 193 nm, and 157 nm. The excimer lasers are along the top right and the enclosures for nitrogen gas purging are in the foreground.

DELIVERABLES: Proved high-quality calibration services, and supporting measurements for excimer laser power and energy meters to the Semiconductor Industry at 248 nm, 193 nm, and 157 nm. Ongoing.

ACCOMPLISHMENTS

■ We have used our Hilger-Chance refractometer system to assist the industry in the search for appropriate high-index fluids (with n greater than water, 1.4366 at 193 nm) for possible use in immersion photolithography. In addition to providing measurement services to several companies which are developing new fluids for 157 nm and 193 nm lithography, we have performed our own survey of fluids at 193 nm. The results are shown in Fig. 3. As this figure shows, there are a number of fluids which are transparent at 193 nm and have n larger than water, up to 1.62 for glycerol. However, the thermo-optic coefficient, dn/dT , is larger as well, which may make their use in a commercial stepper system difficult because of thermal stability issues.

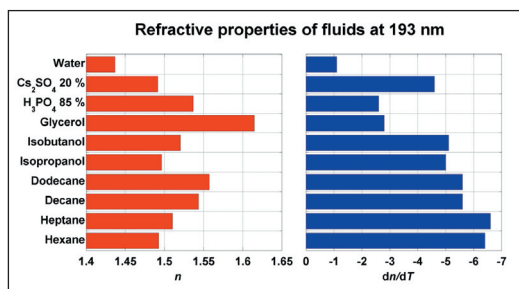


Figure 3. Measured index of refraction n and thermo coefficient dn/dT of a number of potential immersion fluids for 193 nm lithography.

■ We have performed additional measurements of the effect of dissolved air on the refractive index of water at several wavelengths in the visible and UV and compared the results with predictions based on the equation of state of water and the known partial molar volumes and polarizabilities of the soluble components of air. The data and model calculations are in reasonable agreement, and demonstrate that the magnitude of the effect gets larger at shorter wavelength, up to -6.7×10^{-6} at 193 nm. While industry uses degassed water for immersion lithography, our results will enable any potential optical distortions due to air exposure to be modeled at the system level.

■ We have identified four major classes of oxide-based materials that have potential to be used as high-index lens materials for enabling further feature-size reduction with immersion lithography. The four classes are: 1) Group II oxides, *e.g.*, MgO, 2) crystalline spinel (MgAl_2O_4) and its variants, 3) a ceramic form of spinel, and 4) aluminum garnets, *e.g.*, YAG. We have made preliminary characterization measurements of the key 193 nm optical properties (see Fig. 4), including the intrinsic birefringence, of members of each of these classes needed to assess their suitability. As

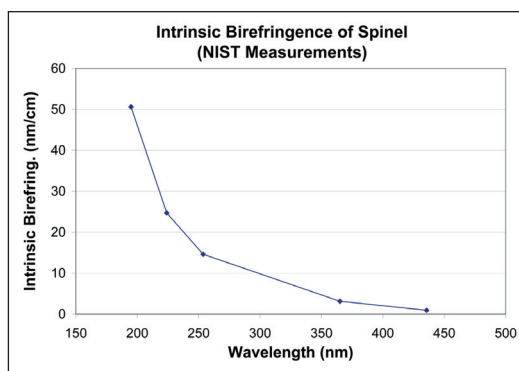


Figure 4. Measured intrinsic birefringence of crystalline spinel vs. wavelength.

a result of these measurements, several potentially feasible candidates have been established.

■ We have constructed a radiometric facility tailored for the DUV range using a beamline at NIST's SURF III with the radiation measurement scale derived from a high-accuracy cryogenic radiometer. The beamline is designed for very general-purpose high-accuracy measurements. We have used this facility to measure DUV general material properties such as transmission and reflectance. Examples of such measurements include DUV mirrors, windows, filters, and also the transmission and absorption of liquids that could be used for immersion lithography. On the detector side, we have calibrated and characterized a variety of DUV detectors such as solid state photodetectors, solar-blind detectors, photoconductive detectors, and pyroelectric detectors. We also performed irradiance calibrations for DUV irradiance meters.

■ We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation (see Fig. 5) and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1 %. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F_2 excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes. For example, we have determined that for silicon photodiodes under irradiation with a 157-nm excimer laser, an important mechanism for the degradation is the formation of trap states at the interface of the silicon-silicon dioxide induced by the damaging radiation. These trap states act as recombination centers and reduce the yield of electric current generated by incident radiation. A model was developed to simulate the change in response for photodiode irradiated by 157 nm radiation.

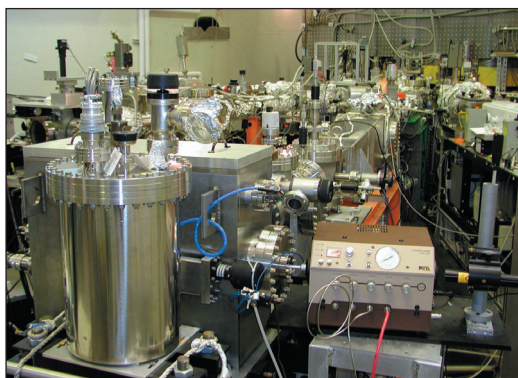


Figure 5. Measurement system for detector damage study by a 157 nm pulsed excimer laser.

■ During the last 15 years we have developed a suite of laser calorimeter standards for 248 nm, 193 nm, and 157 nm excimer laser energy and power measurements traceable to SI units. The 248 nm and 193 nm calorimeters use a specially designed absorbing cavity with a volume absorbing glass to reduce potential damage to the cavity by the high peak power in the UV laser pulses. The 157 nm calorimeter is a fundamentally new type of laser calorimeter standard that uses a thin-walled SiC absorbing cavity, which is designed to completely absorb and spread the incoming laser energy through multiple reflections. All of these calorimeters are calibrated using an imbedded electrical heater that allows for traceability to SI units through electrical standards of resistance and voltage. Calibrations for industry customers are accomplished for each wavelength with appropriate measurement systems that involve purging of oxygen to eliminate atmospheric absorption of the laser radiation.

■ As a further extension of our excimer laser services we have developed the capability to directly measure UV irradiance or “Dose” at 248 nm and 193 nm, which involves homogenizing the beam profile and measuring the energy transmitted through a calibrated aperture. This capability can improve accuracy for customers who need to measure the energy absorbed at a surface such as at the wafer plane.

■ We have also developed the capability to characterize the nonlinear response of 193 nm and 248 nm excimer laser detectors based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. Using this system, one can easily determine problems such as those due to the

incident pulse energy, range discontinuities associated with detector gain, and detector background noise (see Fig. 6).

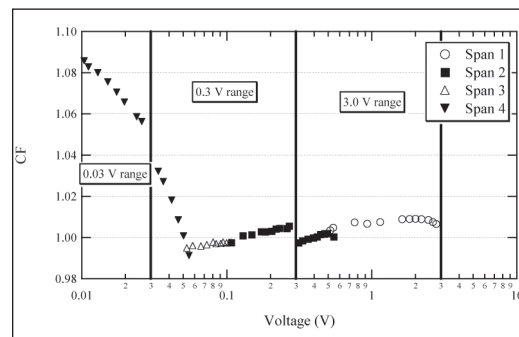


Figure 6. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

■ We completed the first internal comparison of the NIST UV excimer laser calorimeters. This work includes measurements taken over the course of a two-year period in which the performance of the NIST 157, 193, and 248 nm excimer laser calorimeters was monitored at the design wavelengths as well as at the other excimer laser wavelengths. The results show good agreement among the transfer standards and excellent stability over time. From these data, we determined that the responsivity of the NIST UV laser calorimeters all agree within their stated uncertainties. In all but one case, the calorimeters' responsivities agree to better than 0.3 %. The comparison between the DUV (193 nm) and UV (248 nm) calorimeters at 248 nm uncovered a 1 percent difference between the calorimeters' responsivities. This difference is due to partial transmission of the 248 nm radiation through the absorbing glass of the DUV calorimeter which, reduces the calorimeter's absorbance and alters its response.

COLLABORATIONS

Air Products and Chemicals, Inc., Bridgette Budhlall, immersion photolithography fluid development.

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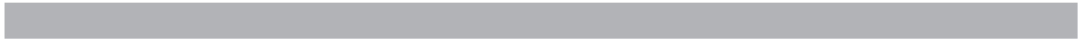
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METROLOGY SUPPORTING EXTREME ULTRAVIOLET LITHOGRAPHY

GOALS

Provide leading-edge metrology for the development and characterization of optical components and detectors used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

CUSTOMER NEEDS

An intense international effort is presently underway to develop EUVL for the patterning of wafers beginning in about 2009. A milestone in the U.S. effort was the building of an alpha-tool called the ETS (Engineering Test Stand) that is housed at the Sandia National Laboratory. While the ETS has demonstrated the feasibility of EUVL for 70 nm design rules and beyond, much work needs to be done to improve the throughput, mask fabrication, and lifetime of the optics.

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the mid 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) precise EUV reflectivity maps; 2) EUV dosimetry; 3) EUV damage characterization; and 4) nanometer level optical figure measurement.

TECHNICAL STRATEGY

1. PRECISE EUV REFLECTIVITY MAPS

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. The beamline can provide a monochromatic beam of EUV or soft X-ray radiation in the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants through angle dependent reflectance measure-

ments. A diagram of the NIST/DARPA EUV Reflectometry Facility is shown in Fig. 1.

Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics larger than 200 mm in diameter. A recent international intercomparison among NIST and several other labs demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.01 nm. Plans are under-way to reduce wave-length uncertainty by an order of magnitude.

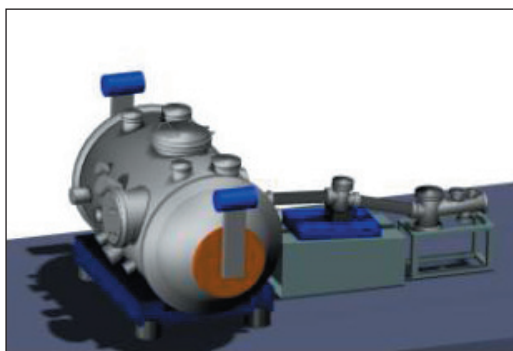


Figure 1. Diagram of NIST/DARPA EUV Reflectometry Facility, including the sample chamber and monochromator.

DELIVERABLES: Full reflectivity map of EUV mirrors up to 40 cm in diameter and 45 kg mass on an as needed basis for the EUVL community. Reflectivity and transmittance measurements of metrology components for EUVL community.

2. EUV DOSIMETRY

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. Until recently all NIST-characterized EUV photodetectors were calibrated on the SURF storage ring, which is essentially a cw source. Recently we have designed and built a pulsed EUV source similar to the source used in the ETS to calibrate EUV detectors for characterizing sources as well as wafer-plane dosimeters to be used in EUVL.

Two major concerns arise when using solid state photodiodes for detection of short pulse length radiation. First, while the average power may be quite modest, the peak power can be quite high. For example, a 10 Hz laser with an average power of 10 mW has a peak power of 100 kW for a 10 ns pulse. Photodiode saturation may

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seriously affect the linearity of EUVL dosimeters, even at fairly low average power levels. We have measured the limit of the linear operating range for an EUV sensitive Si photodiode using 532 nm radiation as a proxy for 13.4 nm; the absorption characteristics in Si are nearly identical. We have found that the photodiode responsivity is an inherently non-linear function of pulse energy, but the responsivity can be fit by a calibration function having two constant parameters. Use of the non-linear calibration function allows the photodiode to be used with reasonable uncertainty even when the responsivity has decreased due to saturation effects by as much as a factor of two. Defining the limit of linear operation as the pulse energy at which there is a loss of responsivity of 2 %, the total charge collected from a Si photodiode is a linear function of pulse energy at peak powers of 1 W (for an unbiased device) to 5 W (for a reverse bias of 10 V). The peak voltage developed is a linear function of pulse energy from 60 mW (unbiased) to 250 mW (10 V reverse bias). Currently, we are extending these results to determine the effect of the longer pulse lengths typical of EUVL plasma discharge sources, to understand the dependence on pulse energy density, and to explore a range of higher reverse bias conditions. A second concern is the equivalence of the responsivity under pulsed conditions and under the cw conditions of calibration facilities. We have compared the measured responsivity of a Si photodiode under pulsed conditions to the results of a low-power cw calibration. The low-power limit of the non-linear pulsed responsivity function is identical to the low-power cw responsivity with a relative standard uncertainty of 1 %. Thus, the results of a cw calibration may be transferred to a pulsed application if the pulse energy dependence is properly accounted for. Finally, we are investigating the saturation behavior using cw EUV radiation. The combination of these three conditions should lead to a good understanding of pulsed-EUV behavior.

We have developed a model of the physical processes that are responsible for the observed non-linear response function of the photodiodes. The loss of total collected charge is modeled as a result of recombination processes in the device during the electronic readout process. In this model, the decrease in the peak voltage developed arises from an increase in the junction capacitance due to the presence of the photogenerated electron-hole pairs, which act as a polarizable dielectric medium. The model correctly pre-

dicts the behavior of both calibration parameters as a function of reverse bias. To date, we have obtained results in the reverse bias range from 0 V to 10 V, and we will shortly be extending our observations to 150 V.

We have recently reduced the uncertainty of our cw radiometric scale in the neighborhood of 13 nm wavelength from the previous relative standard uncertainty of 4 % to 1 %. We accomplished this by operating an absolute cryogenic radiometer (ACR) on a high-throughput beamline at the SURF III synchrotron radiation facility and calibrating working standard photodiodes by direct comparison to the radiometer. The improved cw scale is transferred to the EUVL calibration facility described above to provide a U.S. national radiometric scale for detector-based pulse energy measurements at 13.5 nm wavelength with a relative standard uncertainty of a few percent.

Our group recently conducted the first ever responsivity measurements of an assembled Flying Circus metrology tool for EUVL on a pulsed EUV laser-produced plasma source, shown in Fig. 2.

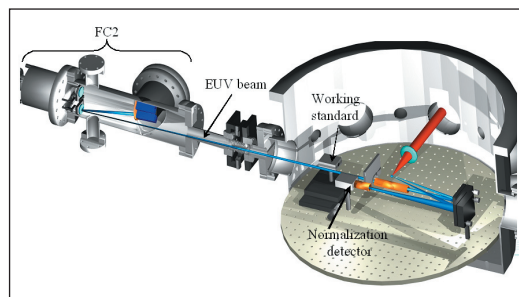


Figure 2. Flying Circus attached to laser-produced plasma source for calibration.

The Flying Circus (FC2) was developed by FOM (Foundation for Fundamental Research on Matter in the Netherlands). It is a filtered radiometer composed of Mo/Si Multilayer mirror, a thin film filter, and an EUV sensitive photodetector. The measurements were compared to the expected performance of the FC2 based on the NIST calibration of the FC2's individual components. The comparison found that there was a saturation effect in the NIST working standard detector, this was also predicted by the work noted above with visible light tests. The information and a model generated from those experiments was used to compensate for saturation effects in the working standard. With the saturation compensation, the resulting FC2 responsivity measurements were within 2 % to 3 % of that predicted by individual

component measurements. These measurements confirmed that EUV radiometry tools can incorporate calibrations based on individual component calibrations, thus eliminating the need for difficult assembled instrument calibrations. The experiments also allowed us to determine limits of linear performance for a commonly used EUV detector. Finally, our measurement and subsequent saturation modeling further substantiates the use of visible light as a proxy for EUV in detector saturation experiments.

In order to further our understanding of the saturation effects in silicon photodiodes we will continue to study the performance of these detectors under various pulse conditions. We will vary the spot size on these detectors to determine the effect of illumination area on saturation performance. In addition, we shall do a survey of several devices to determine the sample-to-sample dependence of saturation performance and develop tests that consumer's can use to determine the saturation onset levels of individual devices in house. Finally, we intend to expand our EUV measurement capabilities to include Synchrotron light-based measurements of EUV spectrograph and CCD responsivity to further aid the EUV lithography community.

DELIVERABLES: (1) EUV CCD responsivity Measurement Q3 2005 (2) EUV spectrograph measurement Q4 2005 (3) pulsed detector saturation evaluation Q3 2005

3. EUV DAMAGE CHARACTERIZATION

One of the potential showstoppers for commercialization of extreme ultraviolet lithography (EUVL) is the degradation of the multilayer-mirror stepper optics. The mirrors lose reflectivity because adsorbed contaminant gases such as hydrocarbons and water are cracked by the energetic (13.5 nm) photons. This leads to growth of an amorphous carbon layer on the optics surfaces or to oxidation of the optics themselves. The former effect is largely reversible; however, the latter is not. Unfortunately, these ambient contaminants cannot be eliminated by baking because the alignment of the mirror stack must be maintained to submicron tolerances. Various capping layers are currently being developed to extend the lifetime of the multilayer mirrors towards the required goal for commercialization of only a few per-cent reflectivity loss over 30 000 h of use.

To study the effectiveness of new capping layers and to better understand the underlying processes responsible for mirror degradation, NIST has commissioned a new beamline at the Synchrotron Ultraviolet Radiation Facility (SURF III) that can expose capped-multilayer samples to $\approx 6 \text{ mW/mm}^2$ of 13.5 nm radiation in an environment of controlled water or hydrocarbon partial pressures up to $6.7 \times 10^{-4} \text{ Pa}$. To date the most successful capping layer available to the community has been $\sim 2 \text{ nm}$ of ruthenium. Our exposure facility has demonstrated that multilayers with this capping layer suffer approximately one-tenth the reflectivity loss of bare Si-capped multilayers when exposed for $\approx 100 \text{ h}$ under rather aggressive conditions of $1 \times 10^{-4} \text{ Pa}$ of water vapor.

Clearly testing multiple capping layers for the required 30 000 h optic-lifetime is not feasible. So we are developing a program for accelerated lifetime testing which will expose multilayers to various intensities under various atmospheric conditions. The ultimate goal of this program is to develop a model of mirror damage that will enable the extrapolation of the years-long-lifetime under normal operating conditions from a few hundred hours of exposure under appropriately chosen accelerated exposure conditions. This effort requires an understanding of the underlying damage mechanisms that will be developed by an iterative series of controlled exposures and analysis. In addition to measuring the reflectivity loss of exposed multilayers, the damage will be characterized using a range of surface analysis techniques. Although this effort is just beginning, we have already discovered that small levels of hydrocarbons ($1 \times 10^{-7} \text{ Pa}$) can completely determine the rate of mirror damage, even in the presence of much larger partial pressures of water vapor ($7 \times 10^{-4} \text{ Pa}$). Thus the vacuum environment must be carefully controlled and well characterized for any accelerated testing procedure to produce meaningful results.

To respond to the growing need for optic-lifetime characterization we have continued to expand our capabilities. The original lifetime testing facility was developed with support from Sematech and Sandia National Labs. With intramural support from the Advanced Technologies Program this beamline will soon be expanded to deliver two orders of magnitude greater intensity. A second beamline is also being constructed with industry support to meet the testing throughput demands

of the larger EUVL community. In addition to expanding our facilities, we have also established very fruitful collaborations with experts in surface dynamics both within and outside the NIST community.

DELIVERABLES: (1) Carry out experiments on samples provided by EUVL community. (2) Work towards development of accelerated damage model by performing additional exposures and analyses; (3) Expand existing beamline to increase maximum exposure intensity a hundred fold; (4) Construct new lifetime testing beamline.

4. SUB-NM OPTICAL FIGURE MEASUREMENT

The commissioning of the “eXtremely accurate CALIBration InterferometerR” (XCALIBIR) at NIST is now complete and the instrument is fully functional (Fig. 3). The XCALIBIR interferometer is a multi-configuration precision phase-measuring interferometer for optical figure measurements of flat, spherical and aspheric optics that can achieve the very low measurement uncertainties that are required for the measurement of EUVL optics.

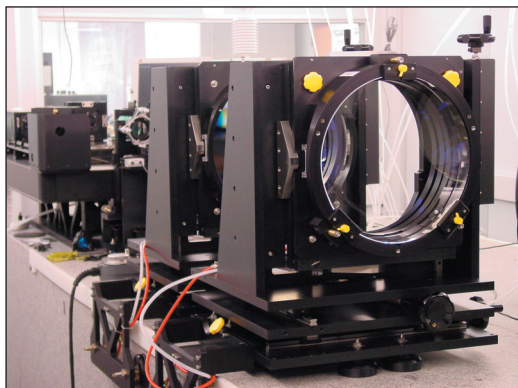


Figure 3. A view of the XCALIBIR interferometer.

The interferometer may be operated in either Twyman-Green or Fizeau configurations. A beam expander in the test arm of the interferometer provides a collimated test beam with 300 mm diameter. Transmission spheres are used to realize a spherical Fizeau interferometer for the testing of spherical and aspheric surfaces. The part under test is mounted on a remotely controlled 5+1-axis mount that can be moved on air bearings along a precision slideway in the direction of the optical axis of the interferometer. A system of three laser-interferometers tracks the movement of the test mount in the direction of the optical axis. A single-mode external cavity

diode laser (ECDL) is used as the light source in XCALIBIR. The laser frequency can be modulated to vary the effective temporal coherence over a wide range. Optical fibers with different core diameters are used to couple the light into the interferometer. The spatial coherence of the light source can thus be varied by changing the fiber core diameter.

The 300 mm diameter reference flats for the flat Fizeau configuration of the interferometer were calibrated with a 3-flat, 6-position self-calibration test. Figure 4 shows the topography of one of the reference flats. A large number of 3-flat measurements were made to estimate the measurement uncertainty. For each of the flats A, B, and C the *rms* of the difference between the averaged flat solutions and the individual measurements was plotted in a histogram (Fig. 5). A (statistical) measurement *rms* uncertainty of approximately 0.2 nm is evident.

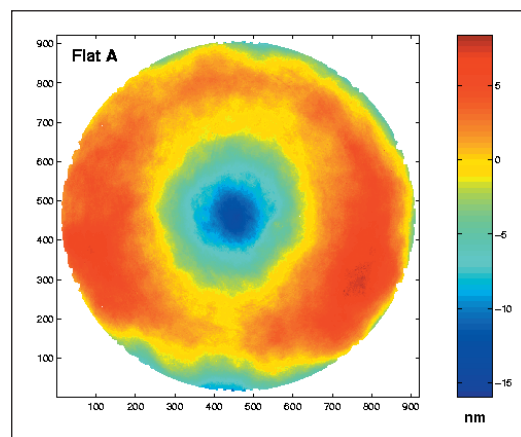


Figure 4. Topography of a 300 mm diameter XCALIBIR reference flat.

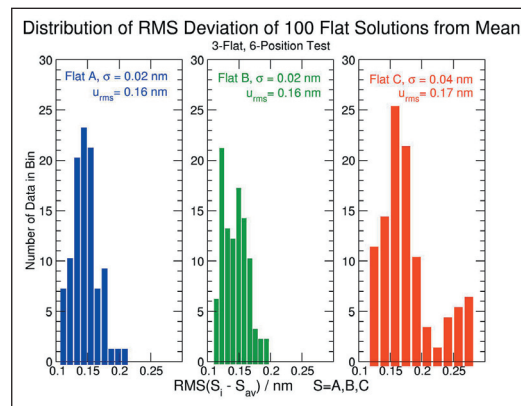


Figure 5. Distribution of rms deviations from best estimates surface (mean) for three flats A, B, and C.

When measurements of aspheric optics without null-optics are made, it is frequently the case that only a part, or subaperture, of a surface can be measured at once. For the figure measurement of the entire aspheric surface a number of overlapping subaperture measurements must then be combined, or “stitched” together. We have implemented flexible and robust algorithms for the stitching of subaperture measurements. To demonstrate the power of the stitching algorithm a precision silicon sphere was set up on a rotary table in XCALIBIR and the surface figure error was measured with an F/1.3 transmission sphere. 36 surface error measurements were made at 10° intervals. As shown in Fig. 6, the individual, overlapping, surface error measurements were then stitched together to form a map of the form error of the silicon sphere.

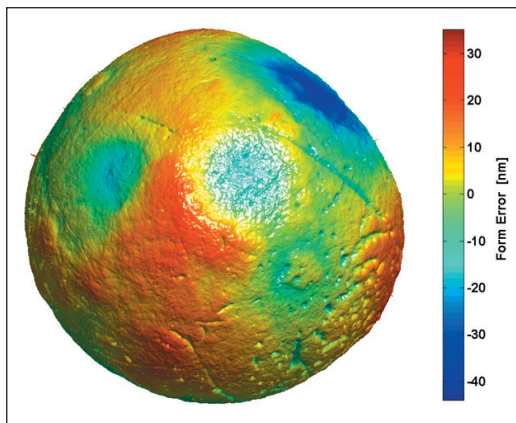


Figure 6. Topography of a precision silicon sphere, stitched from 132 measurements. The figure error is approximately 60 nm PV.

DELIVERABLES: Establish capability for measuring aspheric optics without null optics. 4Q 2003

ACCOMPLISHMENTS

■ IR² has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and thus allows us to make a measurement of the wafer’s thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty.

■ The thickness variation (TTV) of a low-dopant double side polished silicon wafer has been characterized.

■ The flatness of 200 mm and 300 mm diameter wafers in the chucked condition was explored using the XCALIBIR interferometer.

COLLABORATIONS

VNL at Sandia National Laboratory, Leonard Klebanoff, Environmental team.

VNL at Lawrence Livermore National Laboratory, Saša Bajt, EUV Multilayer Development and Coating Team.

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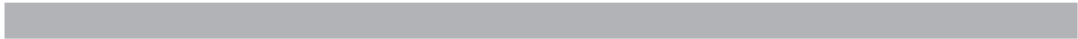
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POLYMER PHOTORESIST FUNDAMENTALS FOR NEXT-GENERATION LITHOGRAPHY

GOALS

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The understanding developed in this program will provide a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 50 nm structures. The unique measurement methods we apply include X-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), near-edge X-ray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), nuclear magnetic resonance (NMR), atomic force microscopy (AFM), fluorescence correlation spectroscopy (FCS) and combinatorial methods. Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the physical properties of and polymer chain conformation within sub 50 nm structures; (2) the spatial segregation and distribution of photoresist components; (3) the transport and kinetics of photoresist components, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermophysical properties of interfaces as applicable to immersion lithography. These data are needed to meet the future lithographic requirements of sub 50 nm imaging layers and critical dimensions.

CUSTOMER NEEDS

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified (CA) photoresists, complex and highly tuned formulations

of a polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility in an aqueous base developer solution. These reaction, diffusion, and development processes must be understood and controlled at the nanometer length scale to fabricate effectively integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 50 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 50 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm, 157 nm, or EUV) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, viscosity, or transport properties. Furthermore, the required resolution for a sub 50 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2004 International Technology Roadmaps for Semiconductors on page 3, Lithography Section, "Photoresists need to be developed that provide good pattern fidelity, good linewidth control (including roughness), and low defects. As feature sizes get smaller, defects and

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"[This work] opens a window of opportunity to construct structure-property relationships between chemical transport mechanisms and ultimate resist resolution. It may also lead to insights into the ultimate, intrinsic resolution limits and critical dimension control of polymer-based imaging materials."

*E. Reichmanis and
O. Nalamasu, Bell Labs, Lucent
Technologies, Science, 297,
349 (2002).*

polymers will have comparable dimensions with implications for the filtering of resists.”

TECHNICAL STRATEGY

In this project, we use model photoresist materials to validate the new measurement methods. Model photoresist materials (248 nm, 193 nm, 157 nm, and EUV) have been used initially to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the reaction kinetics of the deprotection reaction, and the physics of the development process. We also are adapting the application of combinatorial methods as a tool to determine rapidly important lithographic parameters and to identify material factors impacting feature resolution. These results provide a strong basis for understanding the material property changes that may affect the development of lithography for sub-50 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance.

DELIVERABLES: Develop model thin films to measure the transport and kinetics of photoresist components and the deprotection reaction as a function of PAG size and resist copolymer chemistry. 2Q 2005

DELIVERABLES: Conclude protection degree effect on the dissolution and swelling behavior and the relationship to surface roughness for 193 nm photoresist polymers. 3Q 2005

DELIVERABLES: Utilize reaction-front bilayer geometry to identify and quantify the effects of developer solution parameters (base concentration, ionic strength) on the final resolution of lithographic materials. 3Q 2005

DELIVERABLES: Quantify surface segregation, surface deprotection chemistry, distribution of photoresist components (resist, photoacid, base additive) in 193 nm resists, using NEXAFS. 4Q 2005

DELIVERABLES: Develop immersion metrology methods using NR and QCM to quantify developer profiles within ultrathin photoresist films. 2Q 2005

ACCOMPLISHMENTS

■ The molecular origin of dimensional changes within ultrathin films when exposed to developer

solutions was measured using neutron reflectivity. A model 157 nm photoresist material provided needed in the fundamentals of material sources to line-edge roughness. Quartz crystal microbalance measurements complement these measurements with the added ability to measure the kinetics of swelling, however, the profile and chemical specificity are exclusively obtained with NR.

These new measurement methods, applicable to immersion lithography, demonstrate that swelling and aqueous base penetration must be considered to improve dissolution models involving solid-liquid interfaces. The aqueous base profile, shown in Fig. 1, illustrates the penetration of the small base molecule throughout the thin film as a function of developer strength. The swelling, due to polyelectrolyte effects, was predicted in FY03. The influence of moisture and interfacial energy are also probed using NR, XR, and quartz crystal microbalance techniques allowing a complete equilibrium and kinetics measurement methods.

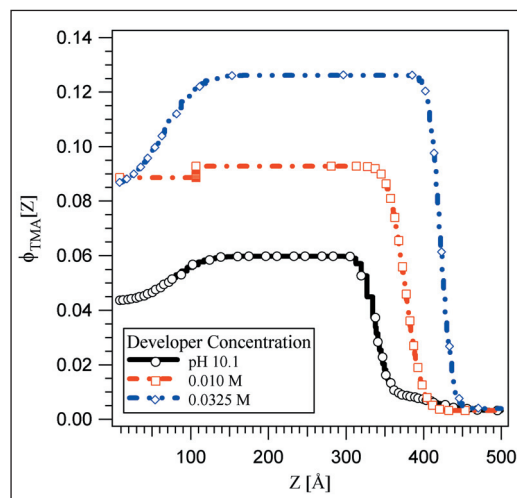


Figure 1. Developer Fundamentals for LER. Direct measure of the base concentration dependence of swelling and deuterated tetramethyl ammonium ion profile throughout the thickness, of a model 157 nm photoresist using liquid immersion neutron reflectivity.

■ After photogeneration, acid molecules catalyze multiple reactions within the photoresist matrix. A central issue in photoresist design is quantifying both the number of reactions each acid can catalyze and the size and shape of the deprotected volume created upon reaction. The size and shape of the volume have been identified in recent computer simulations as a primary source line edge roughness (LER) formation.

Using SANS and specially deuterated polymers, we successfully measured characteristics of the deprotection volume due to acid diffusion paths in a model photoresist. The general technique is readily extendible to photoresists with the appropriate deuterium labeling, independent of the PAG species. The deprotection volume from dispersed acid molecules features a diffuse interface, a result inconsistent with a well-defined two-phase structure. The data in Fig. 2 are consistent with models for random walk statistics. We determined that the deprotection volume has a radius of approximately 8.5 nm after 120 s of post exposure bake at 90 °C. Infrared spectroscopy was used to determine the level of deprotection at 32 % with a 0.7 % mass fraction of PFOS. The result is consistent with a large diffusion path, and hence a large number of catalyzed reactions per acid molecule.

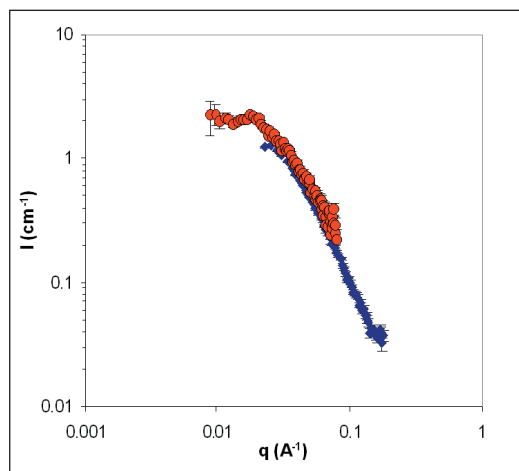


Figure 2. SANS data from the deprotection of dispersed PAGs after exposure and bake. The data are consistent with a random walk deprotection reaction path.

■ The deprotection reaction front profile was measured with nanometer resolution by combining neutron reflectivity and FTIR on a bilayer structure prepared with model 193 nm photoresists. The upper layer of the structure is loaded with the photoacid generator. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group partially leaves the film, quantified by FTIR, upon reaction. The contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of

the reaction and the development process itself. These data are the first available with this spatial resolution and are critically needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that the reaction front width is dependent upon resist chemistry and PAG size. These experimental data provides a rational design of next-generation photoresist component from the resist chemistry to the reaction-diffusion process.

■ NEXAFS measurements were used to measure the surface concentration of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment in Fig. 3. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge x-ray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer chemistry and PAG size. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport

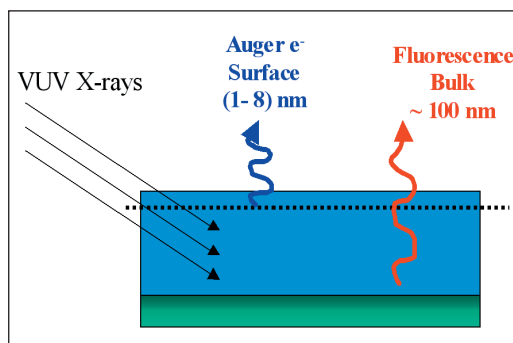


Figure 3. Schematic diagram of the NEXAFS measurement geometry. Spectra are obtained from the film surface and bulk simultaneously.

and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stability against model airborne contaminants and influence on *in situ* processing.

■ The development step selectively removes UV exposed photoresist material and represents the last step in the fabrication of nanostructures prior to semiconductor etch and deposition. With dimensions shrinking to sub-50 nm, control of line-edge roughness becomes more important and contributions to roughness from the development step requires an improved framework. In the development step, the aqueous base TMAH developer shifts the local chemical equilibrium from an unionized form to the ionized form, for instance in the 248 nm material poly(hydro-xy-styrene). SANS data, in Fig. 4, demonstrate the origin of the miscibility in aqueous base is due to the ionization of the photoresist leading to polyelectrolyte behavior. The identification of the presence of polyelectrolyte behavior during the development process provides an improved framework to understand the roles of added electrolytes, such as low molecular weight organic (tetramethylammonium chloride) and inorganic salts (NaCl, KCl). The addition of salts reducing the influence of polyelectrolyte behavior. Current experiments with different developing and rinsing protocols demonstrate that the pH of the rinse step is very important. This suggests the surface layer may contain polyelectrolyte effects even after development as demonstrated by an increase in

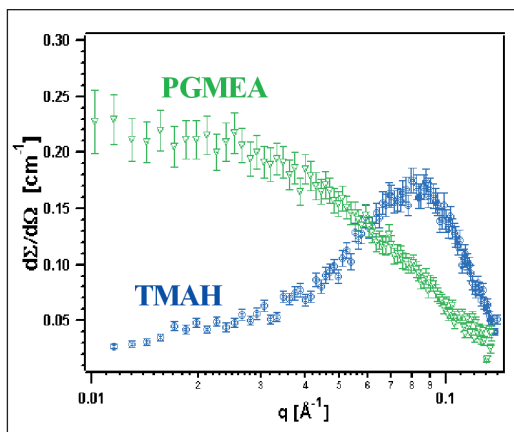


Figure 4. SANS data from a model photoresist polymer in organic solvent (PGMEA) and the developer base solution (TMAH). The scattering peak in TMAH solution is representative of the polyelectrolyte behavior.

surface RMS roughness for the development of bilayer samples with 0.26N TMAH followed by water rinse and 0.01 M HCl rinse.

■ Characterization of local bulk scale mixing is necessary for understanding future photoresist materials as feature dimensions are reduced to sub-65 nm. The intimacy of mixing of PAG and photoresist was probed by solid state proton NMR methods based on inversion-recovery, solid-echo-spin-diffusion, and chemical-shift-based-spin-diffusion pulse sequences. The effect of PAG concentration on the dispersion and phase separation within bulk blends was found to depend strongly on the photoresist chemistry (see Fig. 5). In model 248 nm materials PFOS was found to mix on the molecular scale for loadings between 9 and 45 %; hence the two components are thermodynamically miscible in this range. These results were extended to a challenging 157 nm formulation and revealed that while PFOS is miscible within the two photoresists – the ternary system exhibit phase separation into domains exceeding 30 nm.

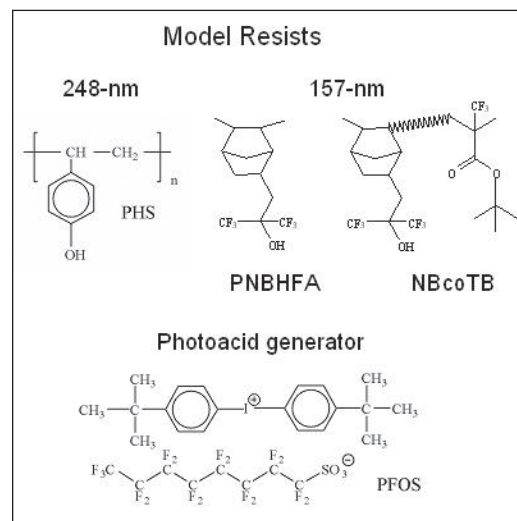


Figure 5. Model 248 nm and 157 nm photoresist materials used to probe the intimacy of mixing of photoacid generator in blends by NMR methods.

COLLABORATIONS

Polymers Division, NIST – Bryan D. Vogt, Shuhui Kang, Ashwin Rao, David VanderHart

Ceramics Division, NIST – Sharadha Sambasivan, Daniel A. Fischer

Center for Neutron Research, NIST – Sushil K. Satija

SEMATECH – Karen Turnquest, Shang-Ho Lin

Intel – Kwang-Woo Choi (Assignee to NIST), George Thompson

IBM T. J. Watson Research Center – Dario L. Goldfarb

IBM Almaden Research Center – Hiroshi Ito

AZ Electronics – Ralph Dammel, Frank Houlihan

DuPont Electronic Polymers L.P. – Jim Sounik, Michael T. Sheehan

SEMATECH – Agreement 309841 OF

Intel – CRADA 1893

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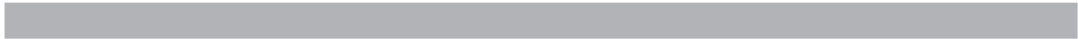
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CRITICAL DIMENSION AND OVERLAY METROLOGY PROGRAM

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes $\approx 35\%$ of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

WAFER-LEVEL AND MASK CRITICAL DIMENSION METROLOGY

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason the project is presented in a number of sub-sections, each focusing on a single technology. These are:

- Scanning Electron-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Electrical-Based Dimensional Metrology and Critical Dimension Reference Material Development
- Optical-Based Photomask Dimensional Metrology
- Model-Based Linewidth Metrology
- Atom-Based Dimensional Metrology

SCANNING ELECTRON-BASED DIMENSIONAL METROLOGY

GOALS

Provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

CUSTOMER NEEDS

The scanning electron microscope is used extensively in many types of industry, including the more than \$200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 100 nm or less with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size known as critical dimension (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accu-

rate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for this sub-100 nm metrology.

TECHNICAL STRATEGY

The Scanning Electron Microscope Metrology Project a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for large amount of good quality samples produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm . In order to make this artifact available (while the final certification details are being completed) the artifact will be released as Reference Material (RM) 8120.

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“Scanning Electron Microscopy (SEM) – continues to provide at-line and inline imaging ... and CD measurements. Improvements are needed ... at or beyond the 65 nm generation ... Determination of the real 3-D shape...will require continuing advances in existing microscopy ...”

International Technology Roadmap for Semiconductors, 2003

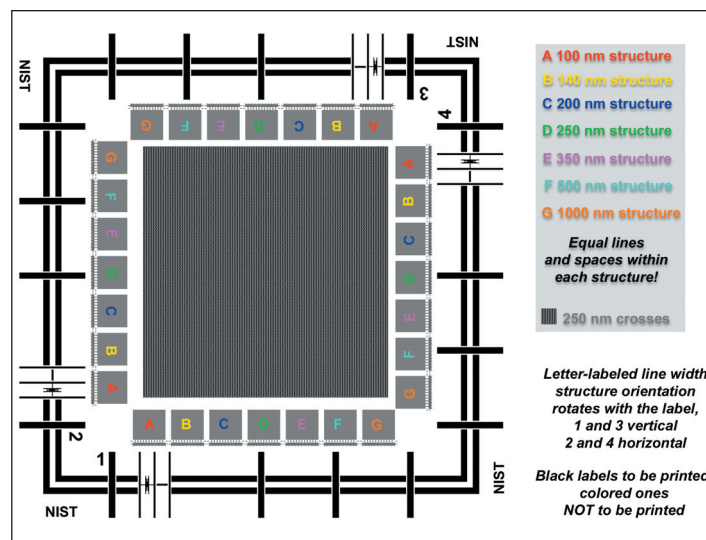


Figure 1. The final design of the SRM 2120 magnification calibration standard reference material.

DELIVERABLES:

- Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask.
- Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples.
- Upon availability of suitable quality samples, quality assessment and delivery of a batch of RM 8120.
- Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples. 4Q 2005

2. SEM Performance Measurement Artifacts:

This effort included the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. New methods and suitable samples are being sought to further improve this type of metrology. Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

3. SEM Linewidth Measurement Artifacts:

Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with a few nm of accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited

relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200-mm and 300-mm Si wafer with polySi features with sizes from 1 μm to down to 70 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

DELIVERABLES:

- Design and preparation of line width metrology artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples.
- Completion of preliminary measurements on samples made by SEMATECH with the new "NISTMAG" metrology mask. 4Q 2005

ACCOMPLISHMENTS

■ SEM Magnification Calibration Artifacts

Samples for Reference Material 8090 have been made in the past once successfully, but later several attempts with e-beam lithography yielded no further useful samples. We now have a new, final mask designed and fabricated at International SEMATECH to get samples made by 193 nm UV light lithography. The use of this conventional lithography and a somewhat modified design provides a chance for large amount of good quality samples produced inexpensively. Because of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm . There are a large number of 250 nm wide crosses for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. The fabrication of the first large batch of samples will be finished in the summer of 2005. With the arrival of the new metrology SEM these will be calibrated.

■ **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered

to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use.

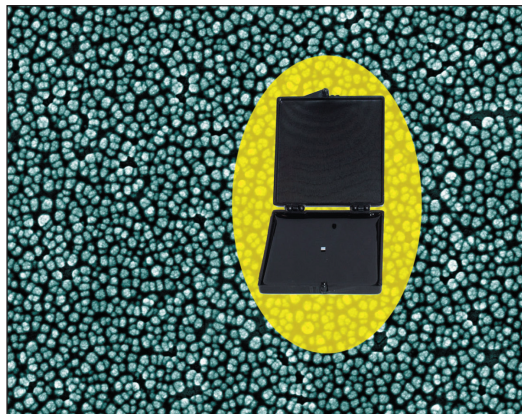


Figure 2. The RM 9081 Sharpness Reference Material.

■ SEM Linewidth Measurement Artifacts

– For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view, using our high-accuracy modeling and fitting methods a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of SEMATECH/NIST mask have been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2005 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ Development of High Accuracy Laser Interferometer Sample Stage for SEMs

– The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.2 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 3 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field-of-views are 2 nm by 2 nm for each images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

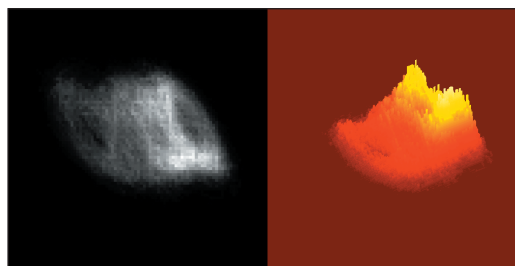


Figure 3. Short-term motion of the SEM sample stage, the stage location (left) and its density distribution during a 1 minute of dwell time, 2 nm by 2 nm field-of-views.

■ Development of Line Edge Roughness Metrology for Integrated Circuit Technology

– The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general

because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to SEMATECH.

■ **Development of Ultra-High Resolution Nano-tip Electron Gun for CD-SEMs** – The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source. Nano-tips, by comparison to conventional cold field, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. Figure 4 proves that the nano-tip electron gun can deliver 6 nm resolution images while the original gun's specification for the test microscope was only 15 nm. Therefore, in an optimized electron optical column, substitution of a CFE source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size,
- Better signal-to-noise ratio and resolution, and
- Faster scan rate and better charge control.

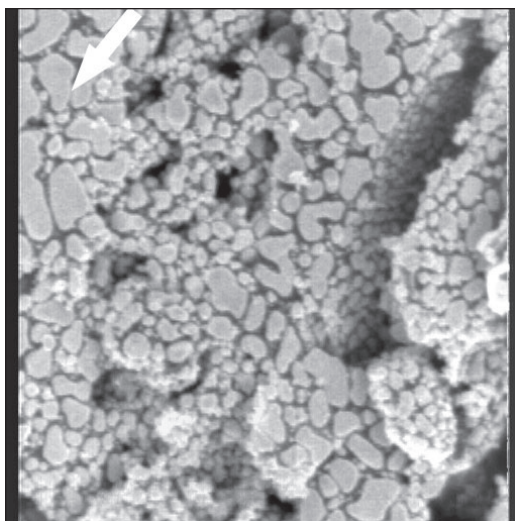


Figure 4. Nano-tip electron gun image showing 6 nm resolution taken on a gold-on-carbon resolution sample at 900 V accelerating voltage. The SEM original specification resolution is 15 nm. The field-of-view is 1.75 μm .

This work has proved that nano-tips indeed improve the resolution performance of SEMs and can be used for longer periods of time. Currently further experiments are conducted to assess the optimal setting of the electron gun and the electron optical column and life time and stability parameters of the nano-tips.

COLLABORATIONS

International SEMATECH, Metrology Council.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

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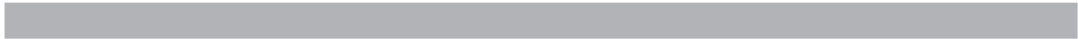
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SCANNING PROBE MICROSCOPE-BASED DIMENSIONAL METROLOGY

GOALS

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2003 edition, the goal in 2004 for critical dimension (CD) measurement precision for isolated lines was ± 0.8 nm; this demand tightens to ± 0.4 nm by 2009. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

CUSTOMER NEEDS

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities, which may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

TECHNICAL STRATEGY

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through two in-house research instruments, a calibrated atomic force microscope for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width. The C-AFM has

metrology traceable to the wavelength of light for all three axes of motion and has provided calibrated pitch and height measurements for nanoscale applications. Pitch, ranging up to 20 μm has been measured with standard uncertainties (u_c) as low as ≈ 0.5 nm at submicrometer scales and relative standard uncertainties of ≈ 0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with u_c on the order of 0.5 % at the largest scales. Calibration procedures have been developed for linewidth measurements using the CD-AFM acquired in FY04. As part of the project, we have also begun to pursue research in the measurement and standardization of line edge roughness.

DELIVERABLES: Presented paper at 2005 ULSI conference on a two sample inter method comparison of image stitching linewidth metrology using carbon nanotube tips with CD-AFM measurements. 2Q 2005

DELIVERABLES: Completed analysis of CD-AFM data to complete the single crystal critical dimension reference material (SCCDRM) project with EEEL and presented paper on methodology at SPIE Microlithography meeting. 2Q 2005

DELIVERABLES: Perform C-AFM measurements to participate in an international Supplementary Key Comparison in Nanometrology on two dimensional pitch measurements. 4Q 2005

DELIVERABLES: Publish Final Report to SEMATECH on the development of a CD-AFM Reference Measurement System (RMS) – the work performed during Ronald Dixon's tenure as a NIST Guest Scientist at SEMATECH. 3Q 2005

DELIVERABLES: Perform SXM measurements of pitch and height on OMAG3L wafer to support the SRM2089 release in FY06. 4Q 2005

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or dry etching. We are also developing an instrument that integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and

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M. T. Postek

surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (IV) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

DELIVERABLES: Develop a predictive model for SPM oxidation kinetics for optimized linewidth control of latent oxide features. This model will include the influence of electronic and ionic transport on the intrinsic thickness growth and lateral spreading due to space charge.

DELIVERABLES: Investigate anomalous features on the growth and breakdown of Group 4 metal films (Ti, Zr, Hf) and their nitrides during local oxidation.

ACCOMPLISHMENTS

- Ronald Dixon completed a three year tenure as the first NIST Guest Scientist at SEMATECH, and returned to NIST in 4QFY04. During his tenure, he developed the CD-AFM reference measurement system (RMS) at SEMATECH for traceable measurements of pitch, height, and width. Measurements were also performed to support the EEEL linewidth standards project which is discussed below. In 3QFY05, George Orji became the second NIST Guest Scientist and will build upon the partnership that NIST and SEMATECH have established.

- We are collaborating with other NIST divisions and external partners such as SEMATECH to develop linewidth standards. A major component of this effort has been the single crystal critical dimension reference materials (SCCDRM) project initiated by NIST researchers in EEEL (Cresswell and Allen). The 2004 release of SCCDRM samples to the SEMATECH Member Companies was recently completed, and CD-AFM dimensional metrology played a central role. The measurements on the SCCDRM samples were performed by NIST scientist Ronald Dixon during his tenure as a Guest Scientist at SEMATECH. A current generation CD-AFM (a Veeco Dimension X3D) which had been implemented as an RMS was used for the SCCDRM measurements. Prior to the measurements, the X3D was characterized and calibrated, and implemented as a reference measurement system (RMS) for traceable measurements of pitch, height, and width. High resolution transmission electron

microscopy (HRTEM) was used as an indirect method of tip width calibration for the SCCDRM samples. The AFM and HRTEM results that were used for the tip calibration are shown in Fig. 1. Features on the distributed samples ranged in width from approximately 50 nm to 250 nm with expanded uncertainties of about 2 nm ($k = 2$) on most features. As a result of this project, CD-AFM linewidth measurements can now be performed with a 1 nm ($k = 1$) standard uncertainty.

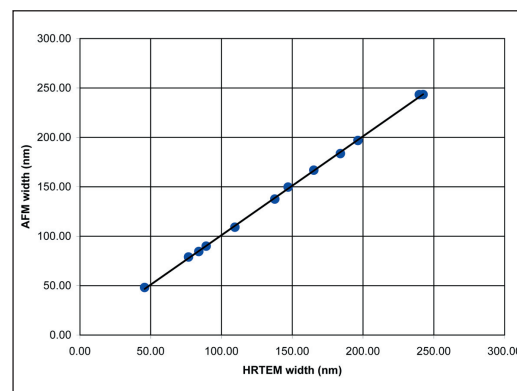


Figure 1. Regression of CD-AFM width values on HRTEM values. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to correct the tip width calibration.

- We are participating in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of NIST-traceable measurements of dimensional quantities important to the semiconductor industry. The results from NIST and other national measurement institutes (NMIs) for step height and grating pitch have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. A comparison of 2-D pitch is presently underway, with NIST participation scheduled for Sept. 05, and a linewidth comparison is in the planning stage.

- Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2004 we developed a draft standard for AFM z-calibration using the single atom steps for the ASTM Sub-

committee E42.14 on STM/AFM. It is currently undergoing review.

- We are developing a technique for AFM linewidth metrology based on image stitching. This involves the acquisition of paired images using a carbon nanotube probe. The nanotube tip enables data acquisition at high resolution on one side of the line in each image, and the specimen is rotated 180 degrees between the two measurements. Stitching these two images into a composite offers the potential of accurate linewidth metrology. We have completed two generations of an experiment in which the stitching result is compared with CD-AFM. The composite image used in one of our published comparisons between image stitching and CD-AFM is shown in Fig. 2. Currently, we are assessing the uncertainties and continuing to refine this approach.

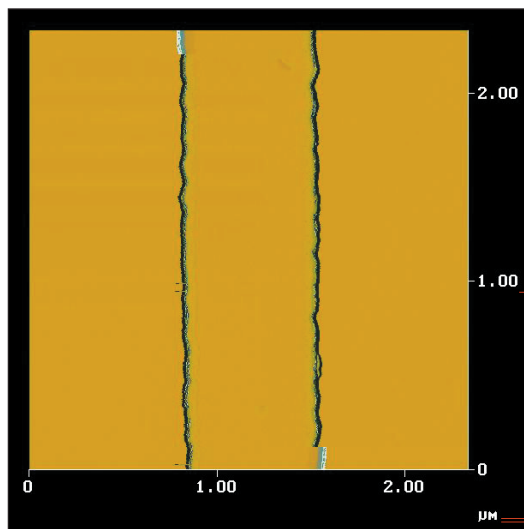


Figure 2. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.

- The commonly used AFM-based method of linewidth metrology in industry is CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. As a consequence of Ronald Dixon's tenure as a NIST Guest Scientist at SEMATECH, we were able to acquire an older generation CD-AFM when SEMATECH purchased a newer one. An image of a SCCDRM specimen taken with this instrument is shown in

Fig. 3. We have developed pitch, height, and width measurement uncertainty budgets for this instrument. As a consequence of the completion of the SCCDRM project, we can now calibrate CD-AFM tip width with an uncertainty of 1 nm.

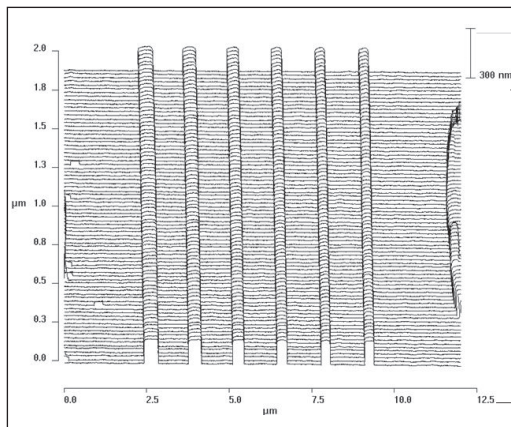


Figure 3. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration. Measurements performed by R. Dixon, sample developed by M. Cresswell and R. Allen.

- We are also working on development of AFM-based techniques for traceable measurement of physical standards for line edge roughness (LER), a potential showstopper in the ITRS.

- In the integrated SPM probe-station thrust, we have completed systematic low-noise (sub-pA) measurements of current flow during SPM oxidation of silicon substrates. Two methods of data acquisition were employed, measurements made directly as a function of voltage, humidity, and exposure time during contact-mode oxidation and those made during a (so-called) force vs. distance curve in which a biased SPM probe tip approaches, contacts, and retracts from a substrate (see Fig. 4, pg. 32). In the latter, electrostatic bending of the SPM cantilever can be easily modeled and the bending capacitance calculated. Electronic and ionic currents have been identified and their consequences for oxide growth and space-charge buildup during lithography have been determined. The role of the water meniscus as a conduit under noncontact oxidation has been clarified.

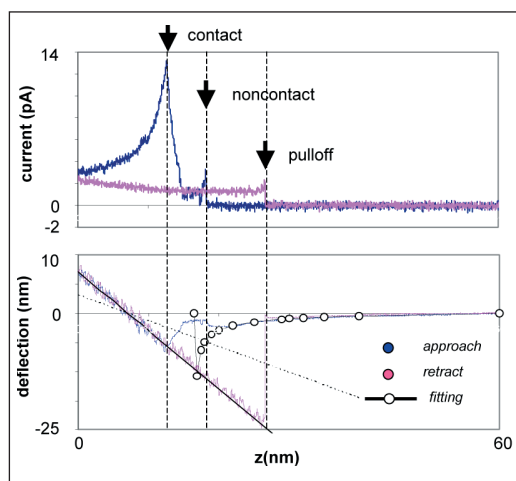


Figure 4. Simultaneous SPM current vs. distance (a) and force vs. distance (b) curves for an 18.5-V biased silicon probe tip approaching, contacting, and retracting from a silicon substrate at 65 % RH. A small 2-pA current flows through the nanometer-scale water meniscus that forms at the junction. A much larger 12-pA current flows when the tip makes hard contact with the substrate.

■ As part of the integrated SPM probe-station thrust, we have also begun studying anomalous oxide growth kinetics in the Group 4 metal films (Ti, Zr, Hf) and their nitrides. In addition to insight into potential defect behavior in alternative dielectrics, SPM kinetic studies of these films reveal new insight into ionic and electronic transport in local oxides that are quite different than in other systems (see Fig. 5).

COLLABORATIONS

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Department of Physics, National Tsing-hua University,
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SEMATECH, Austin TX

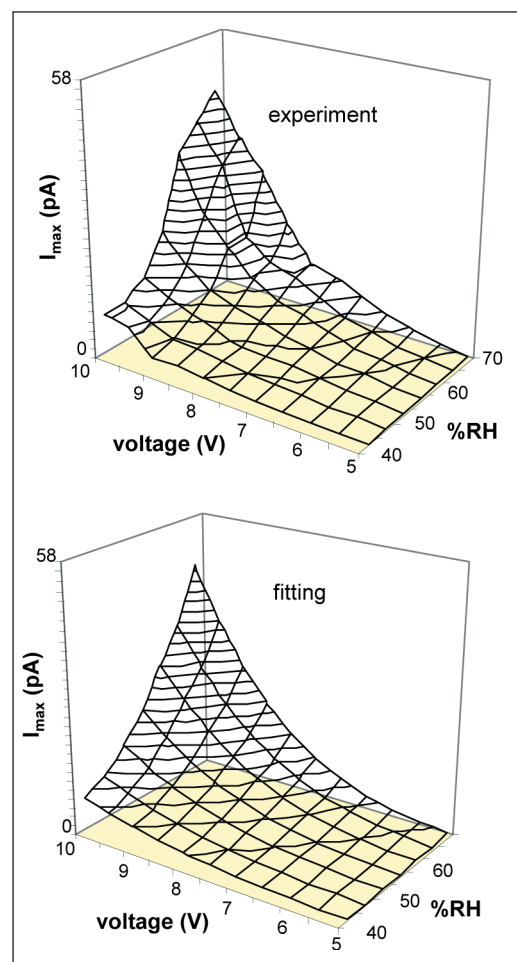


Figure 5. Experiment (a) and modeling (b) of the maximum current achieved during SPM local oxidation as a function of voltage and humidity. The SPM tip used in these experiments was coated with a PtRh metal film and the substrate was hydrogen-passivated n-type Si(100).

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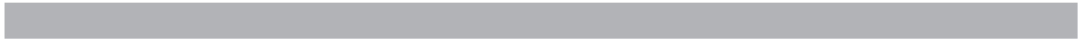
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SMALL ANGLE X-RAY SCATTERING-BASED DIMENSIONAL METROLOGY

GOALS

To develop a small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. Quantities of interest include critical dimension, sidewall angle, and statistical deviations across large areas. Of particular focus is delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, in dense high aspect ratio patterns possessing sub-50 nm critical dimensions. In addition to addressing the metrological needs of future technology nodes, the sub-Angstrom wavelengths utilized by SAXS based measurements well complement current metrological tools based on optical scatterometry, SEM, and AFM.

CUSTOMER NEEDS

The drive to reduce feature sizes to sub-50 nm technology nodes outlined by the SEMATECH Roadmap continues to challenge metrology techniques for pattern characterization. As pattern sizes decrease, existing techniques such as CD-SEM face significant technical hurdles in imaging quantities such as Line Edge Roughness (LER). Emerging metrologies based on techniques such as atomic force microscopy are still being evaluated, providing a lack of clear definition in suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle x-ray scattering as a metrology tool for both process development and the production of standards for industrially practiced metrologies such as CD-SEM.

TECHNICAL STRATEGY

1. Exposure systems capable of sub-50 nm patterning are expected by 2009, requiring control of CD on the level of nanometers and in some cases sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of angstrom level precision in critical dimension

evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission (see Fig. 1) using a sub-Angstrom wavelength. The high energy of the X-ray allows the beam to pass through a production quality silicon wafer, and is therefore amenable to process line characterization. As with optical scatterometry, the measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors suggest that the technique is portable to a laboratory scale device capable of high precision measurements. NIST has designed and expects to implement the world's first laboratory scale CD-SAXS device.

DELIVERABLES: Install and evaluate laboratory scale CD-SAXS instrument 4Q 2005

Technical Contacts:

Ronald L. Jones

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Wen-li Wu

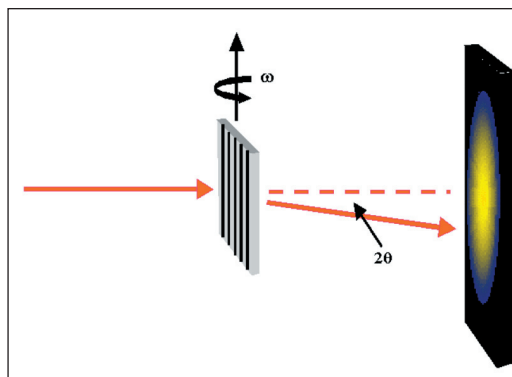


Figure 1. Schematic of the SAXS transmission geometry. Shown is the x-ray beam (solid line) as it passes through the patterned sample and scattered at an angle 2θ . For a precisely aligned sample with known composition, a 3-d lineshape is obtained in one transmission measurement. Unknown samples can also be characterized through measurements at a variety of sample angles.

2. Characterization of pattern quality includes shape factors such as the sidewall angle and curvature. Using the above protocol for scattering, measurements taken at a series of angles of incidence allows the reconstruction of the line shape. We have performed tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1 degree. Ongoing analysis and technique refinement will provide

additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition to a “high speed,” model dependent characterization performed in a single measurement, a second method will be developed based on measurements at multiple sample orientations. This method provides a more precise picture of the entire pattern cross section analogous to cross sectional SEM in a non-destructive and model independent manner. In the current technology node, this measurement will be critical to the evaluation of optical scatterometry models for line shape, while providing a general capability to measure a pattern of arbitrary cross section in future technology nodes.

DELIVERABLES: Develop and publish methodology for sidewall angle measurements with CD-SAXS. 3Q 2004

3. Current LER and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Metrologies such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of optical scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. In cooperation with the Advanced Metrology Working Group at SEMATECH, NIST has designed a series of structures to model different types of roughness. CD-SAXS data from these structures will help further develop modeling protocols.

DELIVERABLES: Design, procure, and measure LER model structures with CD-SAXS. 4Q 2005

4. As circuit designs increase in complexity, next generation metrologies require capabilities to characterize patterns that deviate substantially from line/space patterns. As an example, a capability to precisely characterize dense arrays of high aspect ratio vias non-destructively is needed. The use of a 2-D collimated beam and a 2-D detector in the CD-SAXS technique provides a natural capability to characterize patterns such as vias, posts, and via pads. While the capability to observe such structures has previously been demonstrated, routine analysis of this class of structures has not been achieved. Using a series of patterns including vias of diameter less than 60 nm, we are developing specific experimental

protocols, extending those developed for line/space patterns, to provide a data set capable of describing a precise pattern shape in 2-D arrays of patterns.

DELIVERABLES: Provide measurements and model describing the measurement of 2-D arrays of 60 nm vias patterns. 4Q 2005

5. CD-SAXS measurements can be applied towards several other important problems for both semiconductor and next-generation nanofabrication technologies. CD-SAXS measurements are being evaluated as a potential measurement method capable of determining the densification of the sidewall of plasma etched, patterned nanoporous low- κ dielectric films. Electron microscopy has been used, but has been unable to measure the densification profile with sufficient resolution. In addition, CD-SAXS measurements can be used to evaluate the fidelity of pattern transfer with the nanoimprint lithography (NIL). In NIL, the pattern from a hard, master mold is transferred into an underlying organic material through mechanical pressure and elevated temperature or curing with ultraviolet light. CD-SAXS measurements of both the mold and the resulting pattern can be compared to evaluate the quality of the NIL structure.

DELIVERABLES: Determine feasibility of SAXS measurement methods for sidewall damage characterization in plasma etched patterned low- κ dielectric materials. 4Q 2005.

DELIVERABLES: Apply CD-SAXS measurements for the evaluation of the fidelity of pattern transfer in nanoimprint lithography and to measure the properties of nanoimprinted polymer nanostructures. 3Q 2005.

ACCOMPLISHMENTS

■ We have provided the first measurements of sidewall angle using small angle X-ray scattering (SAXS). Using a series of photoresist gratings produced at the IBM T. J. Watson Research Center (Q. Lin), CD-SAXS was performed using at the Advanced Photon Source (Argonne National Laboratory) to measure photoresist patterns with well-defined sidewall angles. The protocol involves measurements of the sample over 20 degrees of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle (see Fig. 2). The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as

a T-topped line, will produce different scattering patterns. The protocol is generalizable to other pattern shapes.

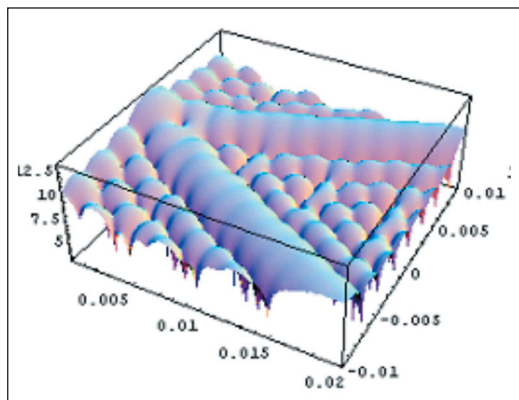


Figure 2. Model of the expected scattering in the plane parallel to the line cross section. Calculation assumes a trapezoidal cross section. The sidewall angle is obtained by the half angle between the prominent ridges.

■ Demonstrated a capability to measure correlated fluctuations in line edge position using CD-SAXS measurements of a series of line/space patterns in a “193 nm” photoresist produced at IBM T. J. Watson Research Center (A. Mahorawala) (see Fig. 3). These samples are believed to possess systematic, small shifts in the pattern. These shifts provide insight into measurements of line edge roughness (LER) where the roughness is highly correlated. The resulting data shows distinct streaks of intensity emanating from the diffraction peaks, particularly strong in the lower order peaks. These represent the first evidence of a capability of CD-SAXS to measure different types of defects related to the overall line edge roughness.

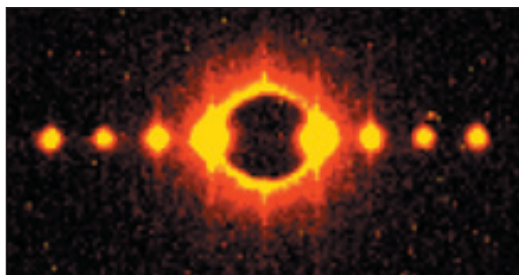


Figure 3. Detector image of a 193 nm photoresist of an approximately 1:1 line/space pattern with a total repeat of 240 nm. In addition to the typical diffraction spots characterizing pitch and linewidth, streaks of intensity are observed emanating from the diffraction peaks. The streaks are a result of correlated roughness.

■ Demonstrated a capability to measure a dense array of vias where the diameter of the vias were etched into a plastic substrate are less than 60 nm (see Fig. 4). Vias were etched into a plastic substrate at the IBM Almaden research center (M. Sanchez). The result demonstrates the capability of CD-SAXS to probe dense vias of sub-100 nm size. Ongoing work will attempt to provide a protocol for the evaluation of the full 3-D via shape as demonstrated for line/space patterns.

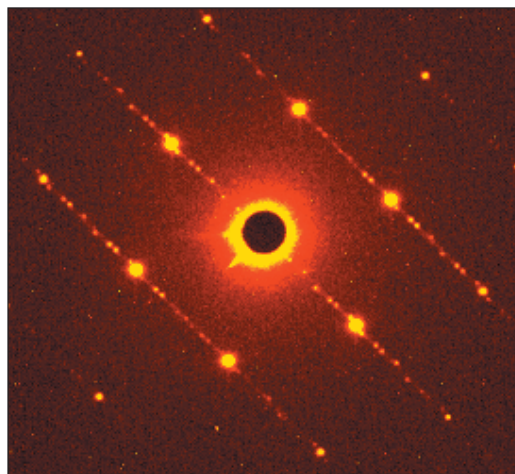


Figure 4. CD-SAXS detector image resulting from a dense array of 60 nm vias. The array of diffraction patterns suggests an approximately hexagonal packing of the vias.

■ Initial feasibility studies have demonstrated the potential of CD-SAXS to detect and to estimate the extent of sidewall damage of nanoporous low- κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low- κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ , it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low- κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low- κ material, then backfilled the trenches with the same candidate low- κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height,

and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature (T_G). Heating these patterns below T_G does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above T_G , the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

COLLABORATIONS

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

SEMATECH, Youfan Liu, Metrology of low- κ patterns using CD-SAXS.

Advanced Photon Source, Argonne National Laboratory, Diego M. Casa and John Quintana, Small Angle X-ray Scattering Instrumentation Development.

University of Michigan, Stella Pang, Ronald M. Reano, Nanoimprinted polymeric structures.

Intel Corporation, Kwang-Woo Choi, Bryan Rice, sub-50 nm structures.

Motorola, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

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ELECTRICAL-BASED DIMENSIONAL METROLOGY AND CRITICAL DIMENSION REFERENCE MATERIAL DEVELOPMENT

GOALS

Develop test-structure-based electrical metrology methods and related reference materials with emphasis on developing physical standards for tool calibration; contribute to standards organizations supporting the development of metrology standards for the semiconductor industry; target the specific near-term goal of fabricating a quantity of reference-features with nominal critical dimensions (CDs) in the range 40 nm to 240 nm and having 2σ (expanded CD uncertainties) of less than 2 nm by July 2006.

CUSTOMER NEEDS

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (*ITRS*), 2003 p. 40, states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels to 25 nm for the 65 nm node. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding *ITRS* specifications for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

TECHNICAL STRATEGY

The technology that the project staff has developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implemen-

tation. Patterning SOI device layers with lattice-plane selective etches of the kind used in silicon micro machining provides reference features with quasi-atomically planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the technology implementation include starting silicon SOI (Silicon on Insulator) wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification originates with High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is totally destructive and thus is not practical for supplying reference features to end users. The project's traceability strategy now features state-of-the-art Atomic-Force Microscopy (AFM) as a transfer metrology. Since use of available and qualified AFM tools is very costly due to the heavy demand of other metrology applications, an elaborate candidate-reference-feature selection protocol has been established. Multiple reference features on a large set of as-patterned chips are identified initially by high-power optical inspection. This procedure checks primarily for reference-feature continuity, cosmetics, and apparent uniformity of the narrowest-drawn features on the test chip which are replicated by the i-line imaging process. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to replicated-CDs of between 50 nm and 300 nm. The "best" 10 % of the features passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20KX. Lateral profiles of the CDs of the captured top-down SEM images are then extracted from them at 25 nm pitch. The measurements are transferred to a custom-designed database, which is then interrogated to identify sets of chips, and the reference-features on them, that are the most uniform at the narrower CDs

Technical Contact:

Michael W. Cresswell

I would like to thank you and NIST for your pioneering work on silicon pocket wafer technology. We have now incorporated this technology in one of our products. We also regard very highly your work on the single crystal linewidth standard. We see this as the first and only attempt by anyone in the world to produce a linewidth standard traceable to the fundamental units of measure, in the sub-100 nm range, for use in the semiconductor industry.

This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips.

We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D., Engineering Manager,
VLSI Standards, Inc.

– typically less than 150 nm. Candidate reference-features so identified on chip are CD-profiled by AFM. The AFM CD-profiles of several features on each chip are examined and the chips are then partitioned into a *calibration* sub-set and a *product* subset.

Scatterometer and OCD (Optical CD) gratings and electrical CD test structures are among the various other patterns on the test chip now being used for CD reference-feature fabrication, Fig. 1. However, the subject of all chip- and feature-selection criteria for SCCDRM transfer metrology has recently become based on some special structures called “HRTEM targets.” There are several hundred of these on each chip. Their design allows the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation, Fig. 2a, Fig. 2b, and Fig. 2c.

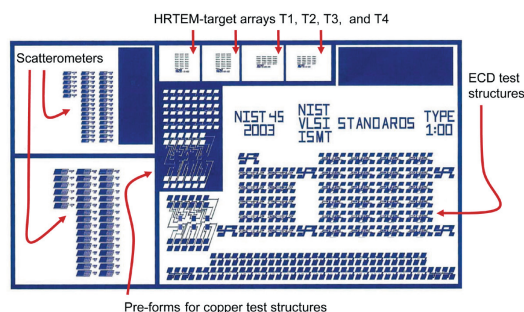


Figure 1. Structure groupings on upper section of NIST45 SCCDRM Chip including HRTEM-target arrays T1, T2, T3, and T4.

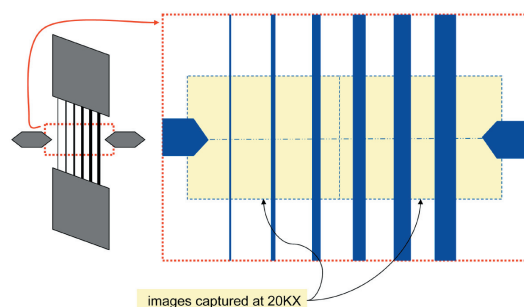


Figure 2a. The new HRTEM-Target Layout provides images from six features having different drawn linewidths from a single FIB cut at precisely known locations along the segment lengths.

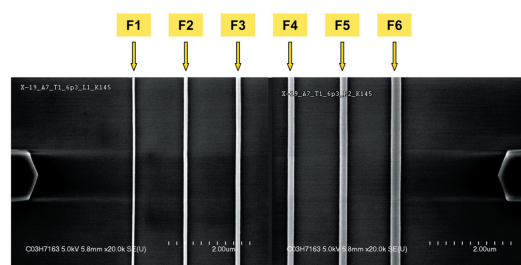


Figure 2b. Composite of two 20KX SEM images of an HRTEM Target with annotated feature numbers. The FIB cut is made between the extremities of the markers on either side of the reference-feature grid.

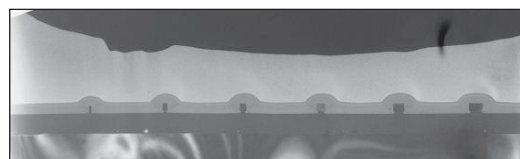


Figure 2c. Low-magnification TEM cross-section of all six features of an HRTEM target.

Since such operations are very costly, this capability is financially advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve.

An important measure of the progress and success of the project is the level of uncertainty attributed to the product CD reference features. A composite 2-target 12-point calibration curve, from which the sub-4 nm uncertainties attributed to the chips that were recently delivered to SEMATECH were extracted, is shown in Fig. 3. In comparison, the units that were delivered to International SEMATECH four years ago typically exhibited in excess of 14 nm uncertainty. This uncertainty was attributed to average CD over several micrometers of reference feature. This macro uncertainty level is not necessarily of interest to the user who needs a value applicable to an order-of-magnitude less segment length. In addition, the cited uncertainty levels were considered to be four to five times higher than what is desired for the roadmap out years. Therefore, the main goal of the project during the current calendar year was reducing the uncertainty to 5 nm or better over reference-feature micro-segment lengths of the order of several tens of nanometers.

To facilitate achieving the stated goal, last year's effort was focused on reducing the macroscopic variations of the physical CDs of the reference features by refinements to the starting-material specifications and to the wafer-fabrication process. The uniformity of fabricated reference features with a nominal 100 nm dimension consequently improved to less than 2 nm per micron of reference-feature segment-length. This improvement is closely tied to the 1.5 nm to 4 nm uncertainties that was ultimately attributed to features on chips comprising the recent delivery.

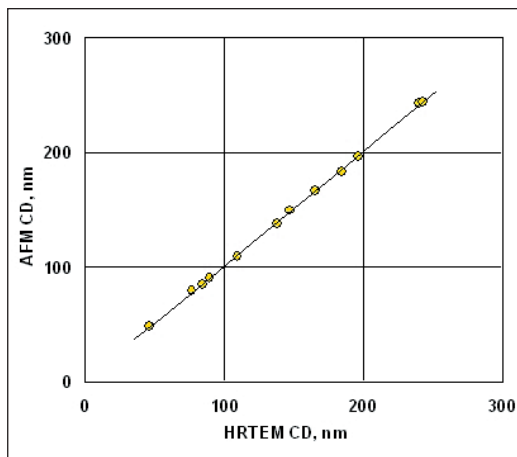


Figure 3. "Example of AFM Transfer-Calibration from a single HRTEM target."

Since 200 mm (110) starting material is virtually unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm wafers to accommodate the product reference-feature chips. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The chips that were delivered in January 2005 were mounted in 200-mm carrier wafers for distribution.

DELIVERABLES: Design a new reference-material test chip having multiple targets each having features with varying ranges of drawn line widths that substantially reduce the cost of HRTEM imaging. Provide new navigational tools to facilitate referencing along lengths of reference features in excess of one micrometer. Include a new segmentation mask level that partitions reference features into multiple shorter segments after patterning without adversely affecting essential reference feature properties, such as sidewall planarity, and provide all necessary on-chip navigational aids to facilitate identification of segments so produced under high-power imaging. 1Q 2006

DELIVERABLES: Evaluate improved reference-feature properties by locating the etch reflux systems in inert atmospheres. The motivation for this process change is to reduce the CD non-uniformity along the reference feature to sub-nanometer from present several-nanometer levels. The model is that more control of reference-feature sidewall-surface cooling, and the ambient to which it is exposed during withdrawal from the hot etch solution, will result in superior CD uniformity and, ultimately, in still lower uncertainty levels. 2Q 2006

DELIVERABLES: Reduce reference-feature sidewall asperities by developing separate processes that target sidewall contamination by organic materials and by residual moisture. These processes may include immersion of the patterned chips in ultra-sonically agitated solvents, extensive pre-cleaning of quartz-ware, and vacuum baking. Construct a relational database to archive all measurements and processing conditions. Add report generators to rank reference features on the basis of measured properties such as CD uniformity, both lateral (along the feature) and vertical (from base of feature to its top surface.) 3Q 2006

DELIVERABLES: Design and perform an experiment to identify the factors that affect the fabrication and cleaning of silicon test features with nano-scale CDs. Eight factors that are known to be potentially-important have been identified and their effects on the test features will be compared on the bases of yield, cleanliness, uniformity and narrowness of feature linewidth. 2Q 2006

DELIVERABLES: Select reference features on a set of 30 chips that are judged to have superior potential for providing sub-40 nm CDs with sub-2 nm expanded uncertainties. Select a sub-set of 3 chips to be submitted for HRTEM imaging to establish an 18-point calibration curve for referencing AFM measurements on the other 27 chips to the lattice-spacing-based absolute measurements. 4Q 2006

DELIVERABLES: Apply project's recently-developed protocol for extracting consistent HRTEM-CD measurements by multiple observers from the features that are submitted for imaging. Reconcile the HRTEM and AFM measurements of each respective feature on a single calibration curve for the purpose of assigning calibrated CDs and their 2σ expanded uncertainties to 10 chips that will be assembled into carrier wafers for delivery to industry clients. 4Q 2006

DELIVERABLES: Fabricate scatterometry targets using the single-crystal reference-material implementation. Invite industry partners to evaluate performance. 4Q 2005

ACCOMPLISHMENTS

■ A selection of SIMOX (Separation by IM-plantation of Oxygen) (110) 150 mm wafers was procured, pre-processed by p-dopant implantation and annealing, and circulated between outside contractors for implantation, hard-mask deposition, and lithography. After lithography,

the wafers with patterned hard-mask films were delivered to NIST for dicing prior to their being patterned at the chip level and inspected by optical and SEM microscopy. During this period, a prototype cleaning process was developed to eliminate particulate and chemical contamination that formerly severely limited the features' usefulness. This procedure was generally successful in preventing 'skipping' of the CD-AFM boot-tip probe, which was essential for AFM imaging. However, it appears that further development of this cleaning process would be advantageous as far as totally removing the SEM-induced hydrocarbon contamination and/or all other residues that are sometimes left on the reference-features' surfaces after patterning.

■ *As a consequence of implementing the wafer-processing improvements described above, and in collaboration with SEMATECH, VLSI Standards, Inc., and Accurel Systems, Inc., the uncertainties attributed to critical dimension (CD) reference features having calibrated CDs in the range of 40 nm to 100 nm were significantly improved.* The improvement in uncertainty results from further technical innovations such as the implementation of a new type of HRTEM-imaging (High-Resolution Transmission Electron Microscopy) test structure, the extensive use of SEM (Scanning Electron Microscope) inspection to identify targets with superior CD uniformity, and the introduction of CD-AFM (CD-Atomic Force Microscopy) to serve as the transfer metrology. A selection of the reference materials was distributed to SEMATECH Member Companies for evaluation.

■ *Questionnaires Distributed, Workshop Held, News Release Issued, and Papers Presented:* These activities were undertaken to contribute to orderly and effective Technology Transfer to industry of the project's outputs. A questionnaire on the use and usefulness of the SCCDRMs that were distributed to SEMATECH member companies was compiled and distributed to the recipients. A proportion has already been returned and the remainder are being actively sought with the assistance of SEMATECH as the summary results are being compiled. A Workshop, which was open to the public, was co-sponsored by NIST and SEMATECH to inform the general public of the availability of sample SCCDRMs. It was held in conjunction with a major semiconductor technical conference and trade show in San Jose, California, in March 2005. The workshop was pre-announced in News Release issued by NIST

after which approximately 12 different trade-magazine editors interviewed project engineers and published their own reports. These were generally complimentary and upbeat. This year alone, Project engineers have made no fewer than five conference presentations. One conference has asked for a new paper from us for an upcoming special issue of the IEEE Transactions on Semiconductor Manufacturing.

■ *ATP Program Award:* The Project engineering team, which is drawn from three different OUs at NIST, bid on, and was awarded, a \$1.5M program to produce a third generation of SCCDRM artifacts.

FY OUTPUTS

COLLABORATIONS

- NIST MEL: Development of AFM CD-profile extraction
- NIST ITL: Traceability statistics and procedures
- Accurel Systems: Design of HRTEM targets and formulation of appropriate imaging procedures.
- The Scottish Microelectronics Centre at the University of Edinburgh, U.K. We are collaborating with this organization, which has received other-agency funding for the purpose of working with us on this project. Their principal contribution at this time is wafer fabrication and related technical contributions.

STANDARDS COMMITTEE PARTICIPATION

- Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)
- SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

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OPTICAL-BASED PHOTOMASK DIMENSIONAL METROLOGY

GOALS

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

CUSTOMER NEEDS

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in Table 115 of the 2003 SIA ITRS as a difficult challenge for <45 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 45 nm. In fact, Table 117b shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 117a, the problems are more acute for CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

TECHNICAL STRATEGY

There are two main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth mea-

surement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties.

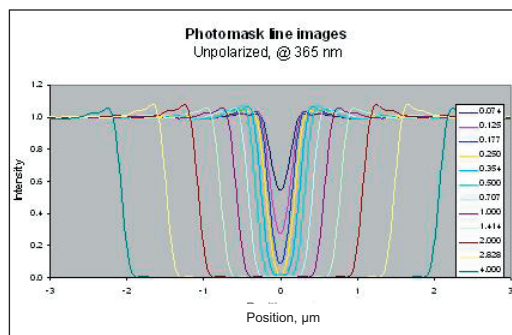


Figure 1. Modeling results for linewidth photomask samples showing CDs down to 0.25 μm .

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 μm to 30 μm have been certified on the previous NIST green light optical calibration system. Linewidth uncertainties have been reduced to 20 nm, $k=2$. The next generation in this line of standards is SRM 2059 (Fig. 2), printed on a standard size $1.4 \times 10^{-4} \text{ cm}^3$ substrate with calibrated linewidths and space-widths ranging from nominally 0.25 μm to 32 μm , and pitch patterns from 0.5 μm to 250 μm .

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology through modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising

Technical Contact:

R. Silver
J. Potzick
T. Doiron

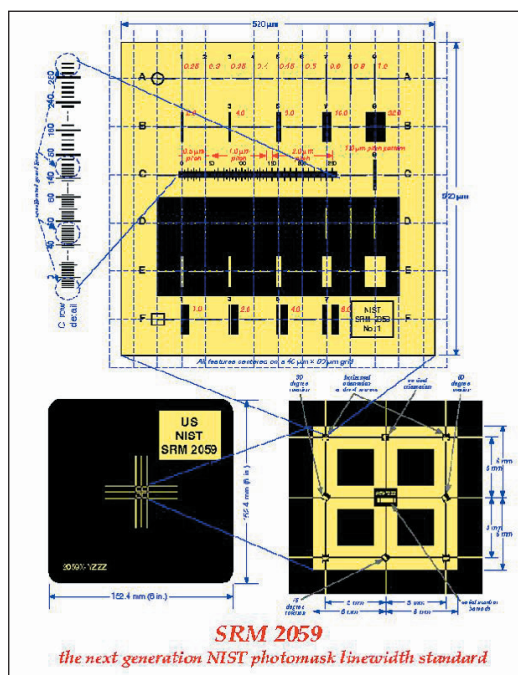


Figure 2. The new linewidth photomask standard.

the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes.

DELIVERABLES: Compare and improve the accuracy of the NIST optical scattering code with new scattering models developed by Spectel and Panoramic Technologies for use in transmission. 3Q 2005.

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is now available as a NIST Standard Reference Material, # 5001. The artifact can be used by the semiconductor industry to standardize 2-D measurements. The SRM 5001 was developed

as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements..

A new generation of grid for the SRMs has been fabricated and another round of measurements is in process. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on the new Nikon5i two-dimensional metrology tool at NIST. The Nikon 5i has been fully characterized and is now in a calibration verification sequence for use in future grid calibrations.

To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES: Use a new advanced algorithm to flag automated focus and positioning control system errors to improve measurement system performance. Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. 2Q 2005.

DELIVERABLES: Implement the standard scale correction and new mapping software for the Nikon 5i system. Measure the new set of two-dimensional calibration grids with a complete uncertainty. 4Q 2005.

DELIVERABLES: Complete the second round of calibrations of SRM 2059 and complete the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 3Q 2005.

ACCOMPLISHMENTS

■ **SRM 2800 Microscope Magnification Standard** is a standard-size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock has been sold.

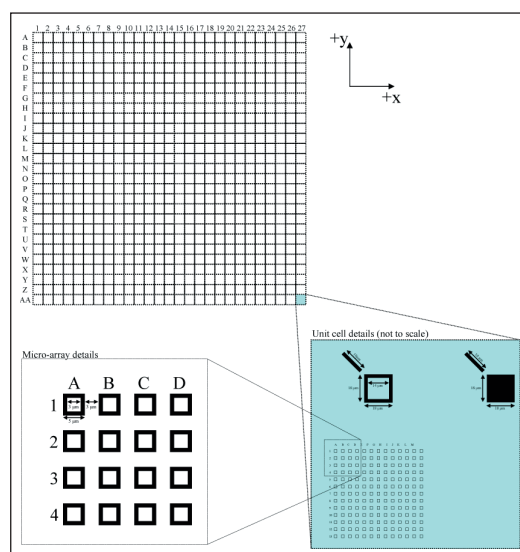


Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

■ NIST currently is completing the uncertainty analysis and documentation for **SRM 2059 Photomask Linewidth Standard**, which will enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

■ The first set of two-dimensional grid artifacts, known as SRM 5001, and has been calibrated and delivered to the SRM office. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. A second set of re-designed 6-inch feature placement standards has been fabricated and measured in the close collaboration between

NIST and Photonics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements has been completed.

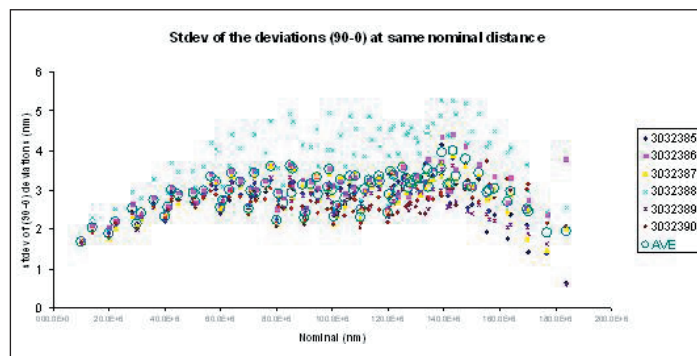


Figure 4 shows tool repeatability and mapping data for the two-dimensional mask calibration procedure.

■ Work closely with SEMATECH to complete a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection.

COLLABORATIONS

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

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MODEL-BASED LINEWIDTH METROLOGY

GOALS

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

CUSTOMER NEEDS

"Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects unless they are accurately modeled and corrected increase measurement variation and, therefore, total uncertainty of CD-SEM measurements." **International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2003).**

"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies." **International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2003).**

"...the exponential rise in value of each nanometer, as nominal gate dimensions shrink, can be estimated... Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds \$10 per nanometer." **C.P. Auschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).**

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had approximately \$213 billion in worldwide sales in 2004.¹ As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 65 nm technology node."

To support present and future semiconductor technologies, industry needs to measure gate widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 3 nm and with measurement repeatabilities of better than 0.6 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth variation, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2003 ITRS specified that LWR, measured as three standard deviations of the CD, must be less than 2.6 nm in 2005 and be measured with better than 0.5 nm repeatability.²

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices. Barriers to accurate LWR measurement include poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness") and random errors due to noise or sampling.

TECHNICAL STRATEGY

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate

Technical Contact:
John Villarrubia

"[The] theoretical work on the behavior of the probe-sample interaction has had a profound influence on our ability to quantitatively analyze probe microscope images."

*Joseph Griffith, Bell Labs,
Lucent Technologies*

"The modeling work ... for electrical CD, AFM, and CDSEM is of value to us ... The current crisis in CD offset uncertainty may be partially answered by this work."

*Anonymous industry feedback
to NIST*

¹ Semiconductor Industry Association press release, January 31, 2005.

² The 2004 update omits a LWR specification, saying only that a proposed new definition for LWR is under consideration.

the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have been developing a model-based library method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories. This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 1). In practice there may be more than two parameters, and the library may be interpolated.

In recent years we have reported encouraging results for this method. Results for polycrystalline Si are shown in Fig. 2a and Fig. 2b. Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fab-

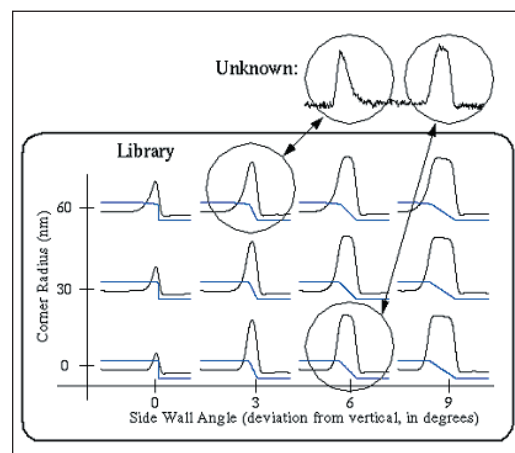


Figure 1. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

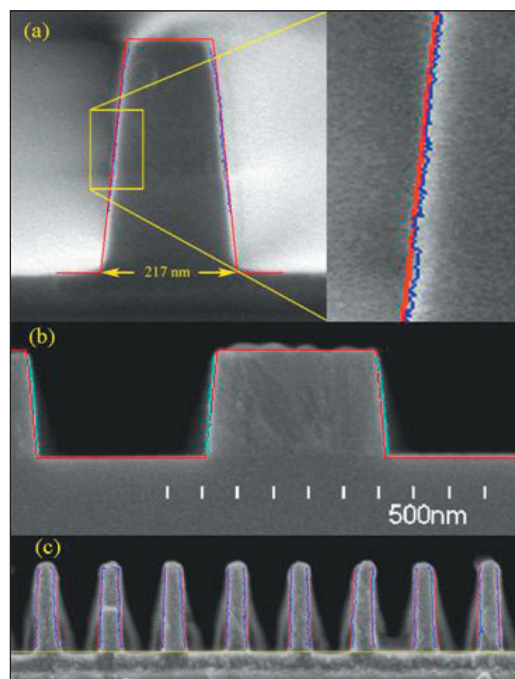


Figure 2. Agreement between MBL and cross-section measurements (a) for isolated polycrystalline ("poly") Si lines in which top-down measurements were performed with a laboratory SEM, (b) for dense poly lines measured with a commercial CD-SEM, and (c) for dense UV resist lines measured with a commercial CD-SEM. In all cases the red lines are the cross sections predicted by the MBL technique based upon top-down measurements, and the blue lines are edges assigned based upon the cross sections (See "Recent Publications" 1, 2, & 3).

ricated in Si rather than resist because resist geometry is too unstable for a long-term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination, charging, and shrinkage when imaging nonconducting resists may result in poorer accuracy for resist samples than for Si samples. Results for a UV resist were obtained in 2003 and are shown in Fig. 2c. One manufacturer of CD-SEMs is now marketing a microscope, announced in summer 2003 at SEMICON WEST, with their own implementation of a MBL method. Others are investigating the method.

In 2005 we are improving the capabilities of the underlying modeling tools used to generate libraries. The existing simulation codes are limited to certain classes of sample shapes, essentially lines uniform along their length and with cross sections characterized by a small number of geometrical parameters, *e.g.*, width, sidewall angle, and corner radius. Improvements to the modeling code would permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, and line footing. We are also encouraging further adoption of this method by CD-SEM suppliers by further publication of the method, by making modeling software freely available to CD-SEM manufacturers, and by collaboration with their engineers.

DELIVERABLES: New more general sample shapes will be added to those capable of being simulated by NIST's MONSEL Monte Carlo SEM modeling code. These shapes will permit extending the MBL method to line edge roughness, contact holes, and other industrially relevant samples. Results will be reported 4Q 2005.

DELIVERABLES: Publication of a review of the method and its results in an archival journal (4Q 2005) and presentation at SPIE of a collaborative paper with a CD-SEM supplier (1Q 2005).

With regard to linewidth roughness measurement issues, we are collaborating with colleagues at International SEMATECH, where we can obtain CD-SEM images of specially fabricated test samples. Such images analyzed at NIST in late 2003 and early 2004 revealed a number of measurement artifacts when roughness is measured using standard methods. For example, noise-induced measurement bias was determined to be significant for samples as smooth as required by the ITRS (see the upper, "standard metric" curve in Fig. 3). In 2005 we are investigating a proposed

alternative measurement method that is not subject to this source of bias.

DELIVERABLES: Presentation at SPIE (1Q 2005) and publication in its proceedings (3Q 2005) of the results of a test of our proposed unbiased LWR metric.

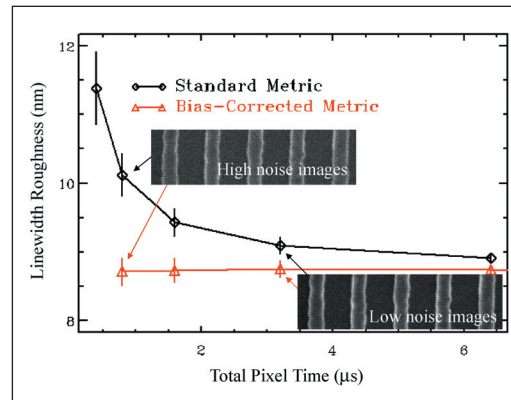


Figure 3. Measured LWR vs. pixel integration time for two different LWR metrics. Lower pixel integration time corresponds to higher noise in the image. Vertical bars are ± 1 standard deviation of the observed repeatability. These were repeated measurements at the same location—therefore all measured values ought to be the same and any observed dependence of LWR upon pixel integration time must be a measurement artifact. Figure based on "Recent Publication" 4.

ACCOMPLISHMENTS

- In cooperation with another NIST division, we organized and held an International Workshop on "Modeling Electron Transport for Applications in Electron and X-Ray Analysis and Metrology." We presented a review paper on "SEM Dimensional Metrology Using a Model-Based Library," that will be published in *Surface and Interface Analysis* (see "Recent Publications" 5).

- In collaboration with the Production Engineering Research Laboratory of Hitachi, Ltd. (which researches CD measurement algorithms for Hitachi CD-SEMs), we compared the sensitivity of several linewidth measurement methods to SEM focus variation (see "Recent Publications" 6). The results indicated that MBL is less sensitive than the current standard methods. However, some sensitivity at large defocus was observed. This sensitivity was attributed to approximations in the beam shape model.

- Our proposed unbiased LWR metric (lower curve in Fig. 3) performed very well in comparison to the standard metric. Results will be

published in the SPIE conference proceedings and have already been made available to CD-SEM suppliers (see “Recent Publications” 4).

COLLABORATIONS

International SEMATECH, Benjamin Bunday, Michael Bishop.

Hitachi, Ltd., Maki Tanaka.

RECENT PUBLICATIONS

1. “Scanning electron microscope analog of scatterometry,” J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, *Proc. SPIE* **4689**, pp. 304-312 (2002).
2. “Test of CD-SEM Shape-Sensitive Linewidth Measurement,” J. S. Villarrubia, A. E. Vladár, and M. T. Postek, final report to International SEMATECH, January 2003, available to member companies at SEMATECH Web site.
3. “Dimensional Metrology of Resist Lines using a SEM Model-Based Library Approach,” J. S. Villarrubia, A. E. Vladár, B. D. Bunday, and M. Bishop, Submitted to *Proc. SPIE* **5375**, 199-209 (2004).
4. J. S. Villarrubia and B. D. Bunday, “Unbiased Estimation of Linewidth Roughness,” *Proc. SPIE* **5752** (2005), in press.
5. “Scanning electron microscope dimensional metrology using a model-based library,” J. S. Villarrubia, A. E. Vladár, and M. T. Postek, *Surface and Interface Analysis*, in press.
6. “Influence of Focus Variation on Linewidth Measurements,” M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *Proc. SPIE* **5752** (2005), in press.
7. “Tip Characterization for Dimensional Nanometrology,” J. S. Villarrubia, in *Applied Scanning Probe Methods*, eds. B. Bhushan, H. Fuchs, and S. Hosaka (Springer-Verlag, Berlin Heidelberg 2004) p. 147.
8. “A Simulation Study of Repeatability and Bias in the CD-SEM,” J. S. Villarrubia, A. E. Vladár, and M. T. Postek, submitted to *Journal of Microlithography Microfabrication, and Microsystems*. (This is an updated reprint of the “Metrology Best Paper” at the 2003 SPIE Microlithography Symposium.)
9. “Issues in Line Edge and Linewidth Roughness Metrology,” J. S. Villarrubia, submitted for proceedings of the 2005 International Conference on Characterization and Metrology for ULSI Technology, Richardson, TX March 15-18, 2005.

ATOM-BASED DIMENSIONAL METROLOGY

GOALS

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

CUSTOMER NEEDS

This project responds to the U.S. industry need for length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer tremendous promise for meeting these future measurement, test artifact, and calibration standards needs of

the microelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer (Fig. 1).

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of linewidth metrology tools. We are also developing unique high-resolution interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions at the nanometer scale. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (Fig. 2).

As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of having samples of known geometry and width essential. This project is developing samples of

Technical Contact:
R. Silver

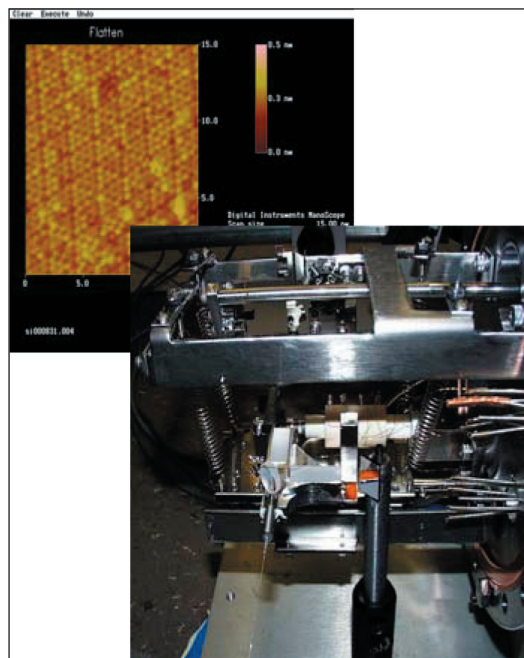


Figure 1. The atomic resolution image above was measured with a 20 pm resolution interferometer system mounted on the UHV STM.

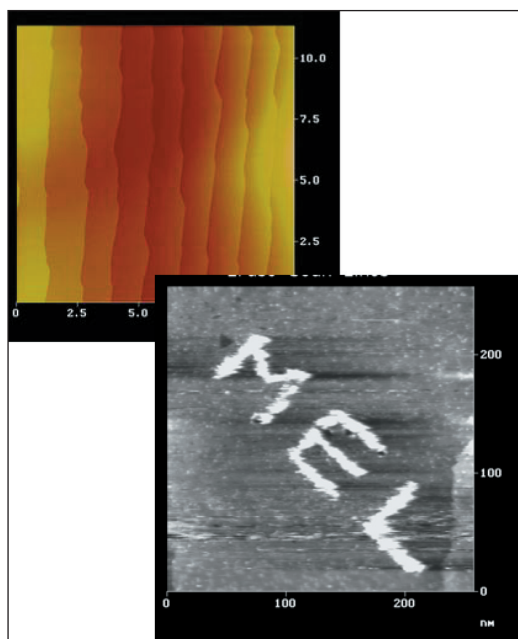


Figure 2. This recent result utilizes the atomically flat surfaces as a substrate for nanomanufacturing. The featured CDs are 10 nm and the entire lateral field of view is 250 nm. The background shows an atomically flat substrate.

known geometry and atomic surface structure which yield well defined dimensional measurements. One goal is a measurement which results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (Fig. 3).

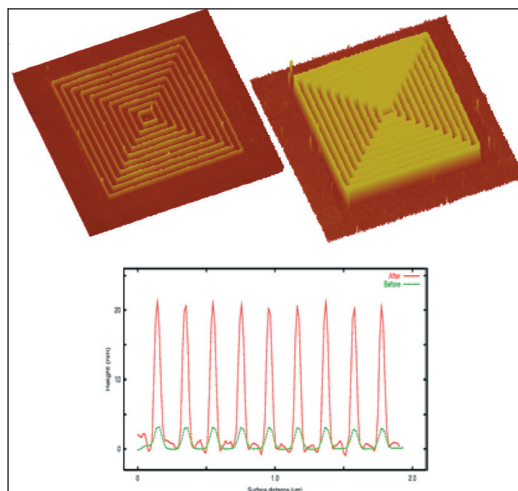


Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

TECHNICAL STRATEGY

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order which is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES: Write features in silicon with critical dimensions smaller than 10 nm. Apply the pattern writing process and etch features for use as optical scatterfield test structures. 3Q 2005.

DELIVERABLES: Work with EEEL to develop improved methods for etching nanostructures written in silicon. Use RIE etching techniques to etch features with sub-10 nm dimensions in silicon. 3Q 2005.

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Investigate nanotubes and alternative W tips as for use in high resolution imaging. Determine the stability of nanotubes for use as STM imaging and fabrication tips. 1Q 2005.

3. Focus on the development of artifacts that can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and have also demonstrated atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing *in-situ* processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures (Fig. 4).

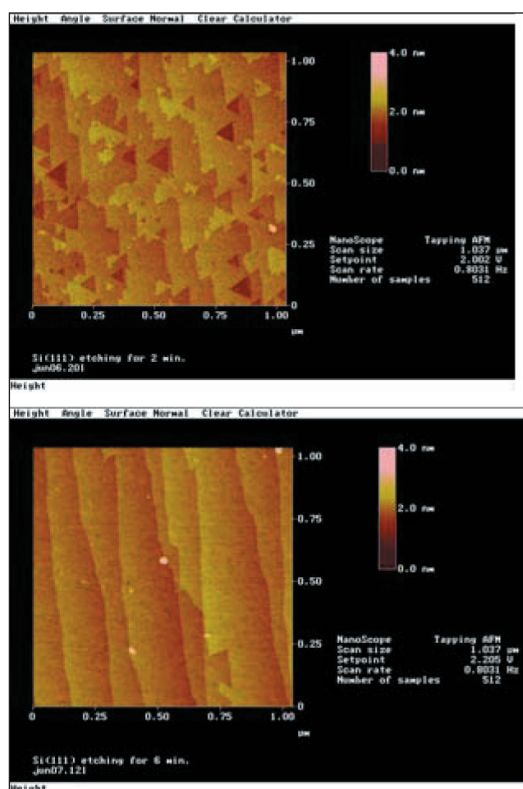


Figure 4. These are atomically flat, chemically prepared surfaces for use in atom-counting and nanomanufacturing.

DELIVERABLES: A new STM which has improved atomic scale imaging capability for atom-based dimensional metrology has been procured and delivered. Implement a transfer mechanism for sample transfer into the UHV environment with the new STM to enable fabrication and metrology on the atomic scale. Install the new STM into the UHV system, test and characterize the new STM and make fully operational. 2Q 2005.

4. The development of a new interferometer system capable of measuring dimensions in the 20 picometer range with high accuracy. Develop an improved system which is also capable of use on the STM so atomic scale measurements can be made with new levels of accuracy. Explore new applications of field ion microscope (FIM) calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

The long term technical objective is the development of *in situ* stabilized, atomically ordered surfaces that can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

ACCOMPLISHMENTS

- We have prepared atomically flat surfaces and obtained atomic order on the wet chemical prepared surfaces. The routine imaging of these surfaces on the atomic scale should be enhanced with the new STM currently being implemented.
- The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been published as an archived journal article.
- Develop the advanced modeling requirements to fully simulate the new STM structure. We have completed finite element analysis (FEA) simulations which test the dynamic modes of the STM and interferometer structure. These results have significantly improved the structural designs.

The results, seen in figure 4, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

- The etching process has been developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A publication recently appeared on this material.

- We have used the FIM techniques to analyze nanotubes and their structure. The nanotubes were directly characterized for use as SPM tips with dimensional analysis on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology (Fig. 5).

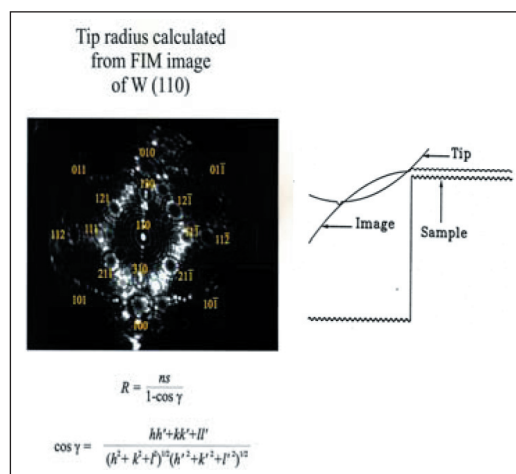


Figure 5. An FIM image showing the atomic order in a W tip is shown. The schematic on the right shows the method of atom counting or high resolution tip-based interferometry.

- We have measured directly the surface atom spacings based on an interferometer measurement. We have fitted our UHV STM with a high accuracy sub angstrom resolution interferometer. We have closed the loop and made atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

ACCOMPLISHMENT: The results for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty have been published in Optical Engineering. These results were also presented at the ASPE conference and SPIE to make the new interferometry methods available to the industry.

COLLABORATIONS

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics., George Washington University.

RECENT PUBLICATIONS

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Satoshi Gonda, Hui Zhou, Joseph Fu and Richard M. Silver, "A new design and uncertainty consideration of a metrology UHV-STM for direct measurements of atom spacings," Proc. SPIE Nanotechnology workshop Vol. 4608 p. 125 (2002).

Hui Zhou, Joseph Fu, S. Gonda and Richard M. Silver "Effects of Etching Time and Wafer Miscut on the Morphology of Etched Si(111) Surfaces," Proc. SPIE Nanotechnology workshop Vol. 4608 p. 168 (2002).

WAFER-LEVEL AND OVERLAY METROLOGY

GOALS

Provide technological leadership to semiconductor equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

CUSTOMER NEEDS

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high throughput, lower cost of ownership metrology tools, which enable more dense sampling strategies has lead to a comprehensive program at NIST to both support and advance the optical techniques needed to make these overlay and photomask/wafer critical dimension measurements (see Fig. 1).

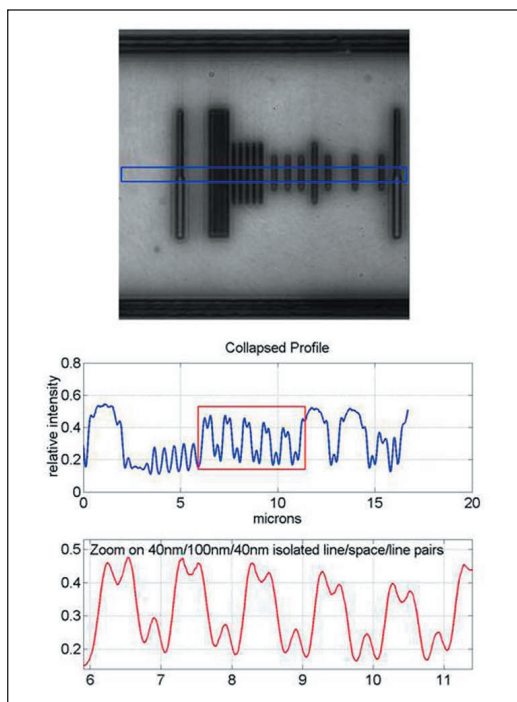


Figure 1. An optical image and profiles of sub-40 nm CD targets used in the development of new advanced high-resolution optical techniques.

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in Table 115 of the 2004 Update SIA ITRS as a difficult challenge for both >45 nm and <45 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 65 nm. In fact, Table 117b shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 118a, the problems are more acute for CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

TECHNICAL STRATEGY

There are two main strategic technical components of this project.

1. NIST has developed an overlay metrology tool that has undergone continuous development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. The technical strategy for overlay metrology is divided into two segments: (a) instrumentation development and the advance of overlay metrology techniques, and (b) the design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS) (Fig. 2, pg. 58).

A set of standard artifacts and procedures, development at NIST, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement

Technical Contacts:

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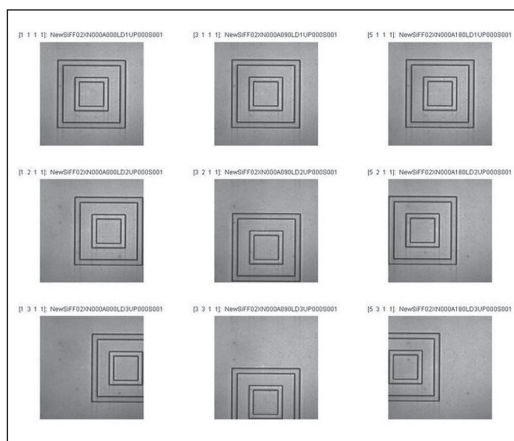


Figure 2. An example of reversal methods applied to determine WIS and the asymmetry of the target itself.

system used for this component is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high resolution image capture with a full field CCD data acquisition system which has been fully characterized and calibrated. This instrument has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems have been evaluated and improved edge detection and CCD array calibration procedures have been implemented. These same methods for two-dimensional CCD array analysis are now being applied to optical component alignment error and aberration analysis.

WIS-free standard overlay artifacts have been fabricated in 200 mm and 300 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for example, Fig. 3 and Fig. 4.

We are also developing a new set of in-chip overlay targets intended to enable the measurement of overlay throughout the active area of a die. These results have been published recently and collaborative work is progressing to develop the commercial capabilities to measure overlay using device sized features in targets of small overall dimension. There is also a comprehensive effort to develop new high resolution overlay targets intended to enable the continued use

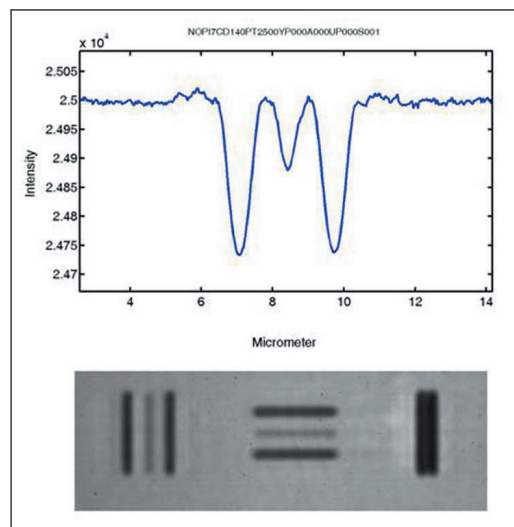


Figure 3. The new in-chip overlay targets.

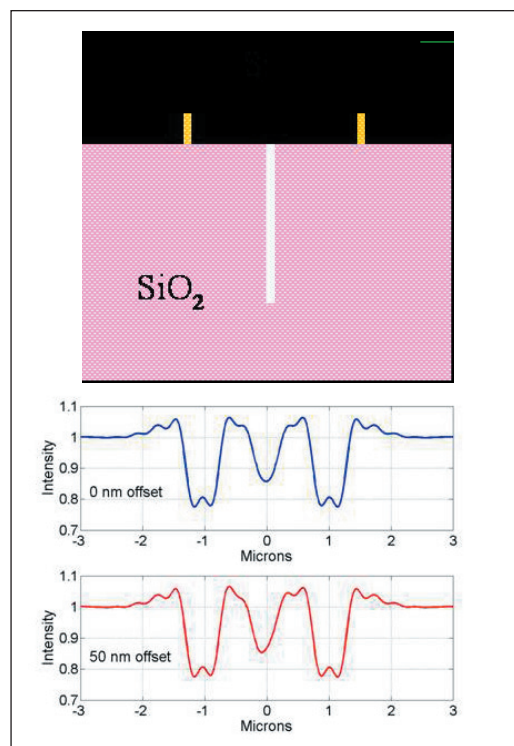


Figure 4. New proposed overlay targets which occupy less than $2\ \mu\text{m} \times 2\ \mu\text{m}$ in total space. This is designed to be an in chip target.

of optical overlay measurements for the 65 nm node and beyond.

DELIVERABLES: Complete an improved set of qualification tests for the overlay microscope, optics, and the x-y metrology stage. Submit the final uncertainties and tabulated combined uncertainty values to the SRM office in an SP260. This includes the characterization and calibration of complex optical alignment effects on overlay output values. 2Q 2005

DELIVERABLES: Use the new metrology reticles from the SEMATECH collaboration to fabricate a new set of overlay calibration targets/wafers. Work with SEMATECH and the Overlay Metrology Advisory Group (OMAG) to determine designs of new high resolution overlay targets. This includes design elements and measurement protocols for using the new high resolution overlay targets to enable optical metrology beyond the 65 nm node. 4Q 2005

DELIVERABLES: Work with SEMI and SEMATECH in the development of new target designs and standards specifications for overlay metrology. This new specification will try to bring some standardization to the growing number of proprietary overlay target designs. 4Q 2005

Modeling the effects of all of the relevant feature properties encountered in overlay measurements and optical critical dimension measurements using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 5. NIST has a world class effort in optical modeling. This includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and the NIST-developed exact integral equation solver method. The latter method has become recognized as the most accurate in existence today.

DELIVERABLES: Compare and test the accuracy of new scattering models for line width evaluation in reflection mode and transmission mode. 3Q 2005

DELIVERABLES: Develop new calculation methods for analyzing asymmetric overlay targets. Compare with modeling results of more standard double-etched silicon structures. 2Q 2005

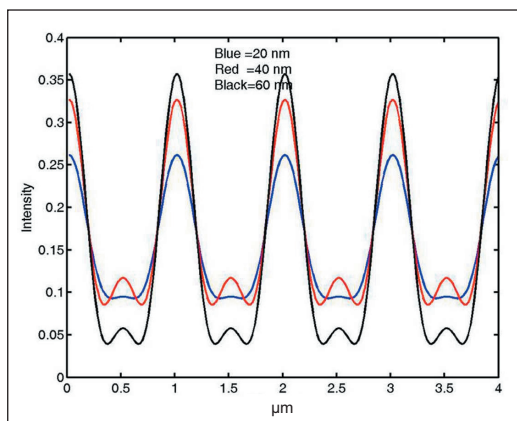


Figure 5. These data are modeling results showing the potential for using high resolution optical methods for wafer level CD metrology.

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This methodology has demonstrated the possibility of using optical methods for line width and overlay metrology with targets smaller than 50 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is well suited to the use of specific metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods which can be suitably applied to device sized features. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are promising, potential solutions to these significant metrology challenges. As a part of this project, we are developing a new optical tool specifically intended to enable this type of scatterfield measurement. This includes comprehensive modeling as well as a new optical configuration designed in house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

DELIVERABLES: Develop a comprehensive set of techniques to accurately measure optical illumination fields. Develop similar characterization methods to measure the collection optics set of aberrations and to perform optimum optical alignment. 3Q 2005

DELIVERABLES: Develop fully automated focus and positioning control systems for the new scatterfield microscope. Complete the optical component design and layout for the new tool and assemble the illumination optics in an open architecture configuration. Implement the existing comprehensive analysis capabilities for data acquisition and edge detection methods. 4Q 2005

ACCOMPLISHMENTS

■ Researchers from the overlay metrology project have submitted two CD 240s for the disclosure of recent potential breakthrough material in high resolution optical metrology. As a part of this disclosure, a new target design which occupies only a few square microns of space was unveiled. The second CD 240 focused on a new proposed method for CD metrology using through-focus

focus-metric signatures which have shown near to nm scale sensitivity to changes in linewidth.

■ **NIST electromagnetic scattering code:** In a further development of the very successful application of the NIST electromagnetic scattering code developed by E. Marx, new results involving arrayed targets have been obtained. These model extensions are providing simulations results and guidance in the optical metrology of targets with features currently down to 70 nm. The model is now capable of simulating targets in array formats as well as illumination at a single angle for analysis and development of scatterfield methods.

■ **Competence proposal successfully funded:** The optics project was successful as champion for the Scatterfield competence proposal. A significant effort to put together and optimize the cross laboratory proposal was successful in landing long term funding for the Scatterfield work. Several companies have shown interest in this work. The funding involves collaboration between the Manufacturing Engineering (MEL) and Physics (PL) laboratories for the evaluation and development of high resolution optical methods involving scatterometry and the new scatterfield methods being developed within Precision Engineering Division (PED). The work also involves technical evaluation of the key issues associated with optical modeling and the n and k input parameters.

■ **Significant industry interest in new high-resolution optical methods being developed under the Scatterfield Microscopy title.** Following invited presentations at SEMATECH OMAG and Advanced Metrology Advisory Group (AMAG) metrology workshops, and discussions at SPIE, there was much interest in the surprising results of 40 nm sized features. These results obtained by optical methods are some of the smallest features shown to these audiences and go well beyond the expected capabilities of these tools.

■ **Reflection mode optical measurements of phase shifting photomasks.** The first round of measurements and model comparisons between profiles from phase shifting reticles has been completed. These results obtained in reflection mode have compared experimental measurements with modeling results obtained using the Egon Marx electromagnetic scattering code. These results were documented and summarized in a SEMATECH final report.

■ **The NIST Overlay Metrology project leader has played a significant role in the (OMAG)**

of SEMATECH. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers and tool suppliers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating in-chip and device sized overlay targets. In addition, CCD array performance and overall optical system characterization and calibration performance measures developed at NIST have been adopted.

■ **Members of the optical metrology project met with several leading optical metrology tool manufacturers** and international measurement laboratories regarding recent advances in the scatterfield microscopy technique. The individual discussions included details about the new high resolution microscopy techniques being developed at NIST and their potential industrial application and implementation. Research in the area of high resolution optical methods is now being pursued at several companies with clear applications in overlay metrology and potential applications in optical based critical dimension metrology. The discussions largely focused on potential technology transfer between the NIST optical projects and development scientists at the optical metrology companies. Details on recent techniques for optical aberration measurements and on methods for evaluating Kohler illumination were covered

■ **NIST researchers have made model comparisons** between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package and the new modeling package from Rsoft. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results have been presented at SPIE Microlithography.

■ **The clean room enclosure for the overlay metrology tool is fully operational.** The metrology tool has been moved to the Advanced Metrology Laboratories and has been returned to its fully operational state in the improved vibration and

cleanliness environment. This allows us to work closely with the industry and make SRMs directly transferable to a clean room environment.

COLLABORATIONS

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

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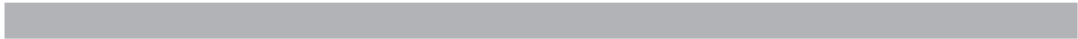
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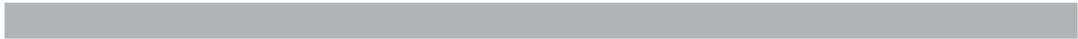
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FRONT-END PROCESSING METROLOGY PROGRAM

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2 , will soon no longer be viable. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.



WAFER AND CHUCK FLATNESS METROLOGY

GOALS

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and technology infrastructure to support the measurement of wafer thickness variation of 300 mm silicon wafers, and surface flatness of chucked wafers.

CUSTOMER NEEDS

Decreasing linewidths and the accompanying reduction in depth of focus, larger wafer diameters for current stepper lithography applications, and the advent of immersion lithography place ever increasing restrictions on wafer flatness and the required measurement uncertainty. The International Technology Roadmap for Semiconductors (ITRS) projects a flatness of ≤ 51 nm at the die site for the 65 nm node by 2010. We are focused on meeting customer requirements for calibrated thickness variation maps of free form wafers and flatness measurements of chucked wafers. We are addressing the need for standard 300 mm wafers with calibrated thickness variation with the NIST Improved Infrared Interferometer (IR³). These independent, traceable wafer thickness calibrations enable manufacturers of wafers and wafer metrology instruments to certify the performance of their metrology instruments. In addition, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometerR" (XCALIBIR). XCALIBIR has a 300 mm aperture for flat measurements and provides a way of verifying models of wafer/chuck interactions.

TECHNICAL STRATEGY

1. The IR² is an infrared phase-shifting interferometer, operating at a wavelength of 1550 nm that measures the thickness of low-doped silicon wafers up to 300 mm diameter (see Fig. 1a and Fig. 1b). The interferometer may be used in several configurations with collimated and spherical test wavefronts. The collimated wavefront mode is the current focus of the project. In this method, the planar infrared wavefront is normally incident on the wafer. A portion of the beam is re-

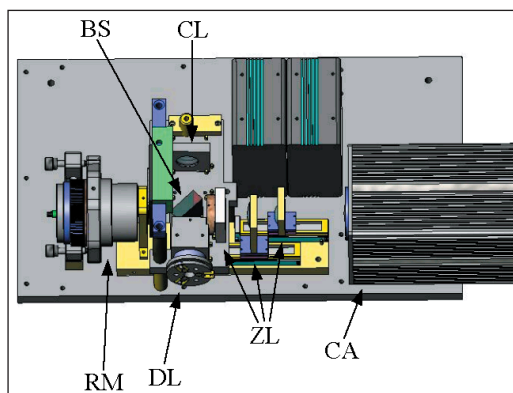


Figure 1a. NIST's infrared interferometer (IR²). The main components of the interferometer are: collimator lens (CL), polarizing beam splitter (BS), phase-shifting reference mirror mount (RM), diverger lens (DL), zoom lens system (ZL), and camera (CA).



Figure 1b. Test end of the IR² setup for TTV measurements of 300 mm wafers. The picture shows the collimator lens together with a silicon wafer and a return flat.

flected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The interference of these two wavefronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation. Figure 2 (pg. 66) shows the thickness variation map for a 300 mm silicon wafer.

Technical Contacts:

U. Griesmann
R. Polvani

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer-chuck interaction studies are enabling advances in the state-of-the-art of wafer chucking that are essential to fully realize the potential of short wavelength lithography. WFSI's ability to collaborate with NIST in this area is critical to us."

T. D. Raymond
Wavefront Sciences, Inc.,
Albuquerque, NM

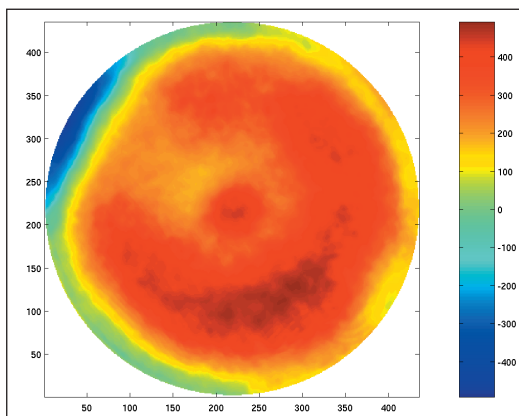


Figure 2. Thickness variation, with piston term subtracted, of a 300 mm double-side polished silicon wafer measured with IR². The height unit is nm, the coordinates in x- and y-direction are detector pixel numbers.

DELIVERABLES: Install interferometer in clean-room for calibration measurements, 4Q 2005. Develop complete uncertainty analysis for thickness and thickness variation measurements, 2006.

2. A component in the evaluation of chucked wafer non-flatness is the characterization of interactions between the vacuum chuck and wafer. We are collaborating with Wavefront Sciences, Inc. (WFSI), Albuquerque, New Mexico and potentially one or more lithographic stepper manufacturers to help understand these interactions. WFSI is carrying out numerical analyses of the chuck/wafer interface for various chuck geometries. Figure 3 shows a model of XCALIBIR, a general purpose 300 mm aperture phase measuring interferometer developed at NIST, which is used to measure the flatness of chucked wafers. The are then be used to evaluate the influence of wafer/chuck interactions on the chucked wafer flatness. (FIGURE 3)

ACCOMPLISHMENTS

■ IR² has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and thus allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty.

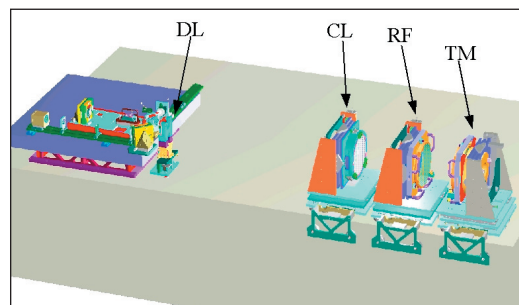


Figure 3. XCALIBIR interferometer configured for flatness measurements. The main components of the interferometer, from left to right, are: breadboard with source and imaging optics, diverger lens (DL), collimator lens (CL), reference flat (RF), and test mount (TM). For silicon wafer flatness measurements a wafer chuck is mounted on the test mount.

■ The optical components in the IR² interferometer were improved to reduce the measurement noise. Wavelength phase-shifting has been implemented and a TTV map repeatability of 5 nm peak-valley has been achieved for 300 mm wafers.

■ The IR² interferometer is being moved to a clean-room which will allow us to make calibration measurements of wafers supplied by industry customers.

■ The flatness of 200 mm and 300 mm diameter wafers in the chucked condition was explored using the XCALIBIR interferometer.

COLLABORATIONS

1. WaveFront Sciences, Flatness measurements of free form and chucked wafers for metrology tool validation.
2. MEMC Electronic Materials, Wafer thickness standard development.
3. Siltronic, Wafer thickness standard development.
4. Intel, Development of very thin silicon thickness standards.
5. Frontier Semiconductor, Flatness metrology for patterned wafers.

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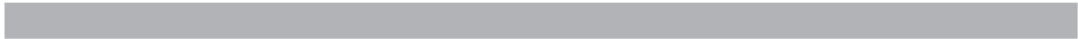
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MODELING, MEASUREMENTS, AND STANDARDS FOR WAFER SURFACE INSPECTION

GOALS

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

CUSTOMER NEEDS

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, nonmetallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem exist now for particles on bare silicon and on non-metallic films, while solutions do not exist for wafer backsides and metallic films in 2007 and 2009, respectively. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by 13 different Scanning Surface

Inspection System (SSIS) indicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8 %. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.

By 2010, at the 45 nm node, particles having diameters 22.5 nm must be detectable on bare silicon and nonmetallic films, 36 nm on metallic films, and 45 nm on the backsides of wafers. No known solutions exist at this time. [2004 ITRS, Yield Enhancement, Table 112b]

TECHNICAL STRATEGY

There are two major strategies for improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvements in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has

Technical Contacts:

T. A. Germer
G. W. Mulholland

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.
VLSI Standards, Inc.

provided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements

– The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLE: Measurement capability for measuring diffuse and diffracted light from a grating. 4Q 2005

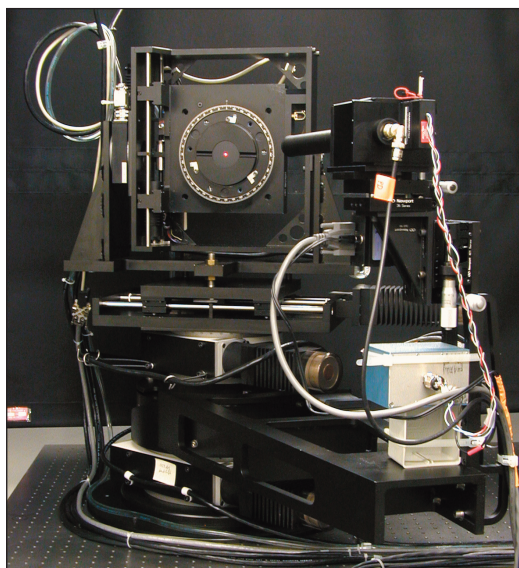


Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

2. Theoretical Light Scattering Calculations

– The focus of our theoretical work is on (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently

and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include: (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLE: Publish computer code for scattering by axially symmetric particles on surfaces. 3Q 2005

3. Size Distribution Measurements – Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle size for 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Certify a 100 nm particle size SRM to replace SRM1963 using the NIST particle sizing calibration facility. 2Q 2005

Certify a 60 nm particle size SRM using the NIST particle sizing calibration facility. 2Q 2005

4. Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be sized by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electrospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes (see Fig. 2).

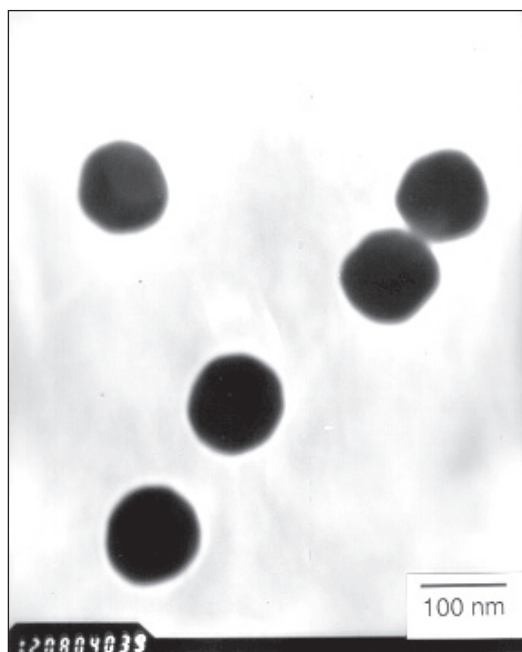


Figure 2. Transmission electron microscope images of 100 nm copper spheres generated by a novel spray pyrolysis method. These particles were developed to test light scattering theories for scattering by particles on surfaces.

DELIVERABLES: Publication of manuscript on the slip correction of nano-size particles based on the DMA. 1Q 2005

5. Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Provide technical support for the development of improved methods for calibrating surface inspection systems through the SEMI Advanced Wafer Surface Inspection System task force. 2Q 2005

ACCOMPLISHMENTS

- Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.

- Developed a NIST Calibration Facility for sizing monodisperse spheres suspended in water in the size range of 50 nm to 400 nm with an expanded uncertainty of 1.5 % of the peak size. This facility has been used for two customers providing calibration particles to the semiconductor community.

- Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

- In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

- Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO₂/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

- Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 2500 copies of the library have been downloaded from the web. The Modeled Integrated Scatter Tool (MIST), a Windows application for calculating scatter, was released in June 2004. In July 2005, Version 5 will be released, which contains a theory for scattering of light by a deformed particle on a surface.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that arise in such measurements. It was found that the uncertainty was dominated by the uncertainty in the shape of the particle on the surface. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

COLLABORATIONS

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

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FRONT-END MATERIALS CHARACTERIZATION

GOALS

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. Major focus is placed on metrology requirements from the 2004 Update to the International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) Structural and elemental analysis at the device level, including SIMS and HRTEM, and (2) Metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project defines optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high- κ and low- κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. High Resolution Transmission Electron Microscopy (HRTEM) is being developed as a chemical tomography tool for determining 3-D elemental distributions in advanced materials.

(3) Determine the work function, band offset, and interfacial structures of high- κ /combinatorial metal electrode stacks systems by implementing a combination of techniques including Scanning Kelvin Probe Microscopy (SKPM), internal photoemission (IPE), backside FTIR, and external photoemission (Soft XPS and Inverse photoemission), and theoretical modeling.

CUSTOMER NEEDS

The Front-End Materials Characterization project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack pro-

cesses and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2004 International Technology Roadmap for Semiconductors (ITRS) near-term (through 2009) difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization, introduction of metal gate electrodes with appropriate workfunctions, and metrology issues associated with 2-D dopant profiling. Metrology needs for Thermal/thin films, Doping Technology, SOI, and strained-silicon are discussed in the 2003 International Technology Roadmap for Semiconductors in the Metrology Section and the 2004 Update.*

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements.

The ITRS identifies structural and elemental analysis at device dimensions (for example 3-D dopant profiling) as one of the difficult challenges beyond 2009. Offline secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving future technology generations. Activated dopant profiles and related TCAD modeling and defect

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profiles are necessary for developing new doping technology. The ITRS requirements are for at-line 2-D dopant profile concentration measurements with spatial resolution of 4.1 nm and precision of 4 % in 2004, increasing to spatial resolution of 2.8 nm and 2 % precision for the 2010 through 2018 timeframe. Complete specifications are given for the short term in Table 119a on page 12, and for the long term in Table 119b on page 13 of the 2004 Update to the Metrology section.

The interface of high- κ gate dielectrics with the metal electrode presents a most critical challenge to the development of a gate stack that meets specifications required by the semiconductor industry. Numerous challenges for these materials exist:

- Defects, as well as interfacial reaction products, at the metal gate electrode/high- κ gate dielectric interface may impact the work function of the gate electrode and the band offset between the gate dielectric and the electrode.
- The thermal stability of the interface strongly impacts the minimum achievable EOT.
- A wide range of binary and ternary compositions for the metal gate electrode are possible.
- A variety of conflicting measurements of the work function and band offsets exist.

TECHNICAL STRATEGY

The 2003 ITRS expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS and HRTEM, and (2) metrology for advanced gate stacks and other thin films. Our focus areas include development of refined metrology methods and standards for SIMS and TEM, developing improved X-ray detection capabilities for SEMs and electron microprobes, and the characterization of high- κ /metal gate interfaces, including band offsets and barrier heights.

STRUCTURAL AND ELEMENTAL ANALYSIS AT THE DEVICE LEVEL, INCLUDING SIMS AND HRTEM

Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We have organized an interna-

tional round robin study through ISO committee TC201 to investigate the parameters that must be controlled to make highly repeatable dose measurements of As with SIMS instruments. In addition to improved repeatability for dopants, the ITRS roadmap also requires increased SIMS detection limits for trace metal and organic contamination analysis of semiconductor devices. We are also working on novel methods to enhance detection limits for common metal contaminants by increasing the ionization efficiency during the SIMS sputtering process.

DELIVERABLE: Evaluate results of international round robin of arsenic dose determination by SIMS. Develop improved methods for high sensitivity analysis of trace surface metals and impurities. 1Q 2005

Analysis of trace metal and organic contamination on silicon surfaces is a high priority of the ITRS roadmap. To utilize effectively tools such as secondary ion mass spectrometry for trace contamination on silicon surfaces, suitable trace standards must be developed. Over the past 20 years, piezoelectric drop-on-demand ink-jet printing has evolved into a precision microdispensing technology with a diverse range of applications. Examples of applications include desktop color printers, printing and synthesis of DNA arrays and printing of molten solder for use as electrical interconnects on integrated circuits. We are exploring the possibility of using ink-jet technology to print elemental and organic contamination standards on silicon. Piezoelectric printers are capable of printing single microdrops of fluid at the rate of thousands of drops per second. Each drop contains a known concentration of the material of interest. Large concentration ranges are possible simply by varying the number of drops printed. Our first attempts will explore ink-jet printing of organic test dyes on silicon with subsequent characterization by SIMS (see Fig. 1). Once standard operating procedures are developed for ink-jet printing, it should be feasible to produce standards, (both organic and trace metal) for quality control and calibration of a variety of analytical techniques including SIMS, XPS, AES, EPMA, TXRF and others.

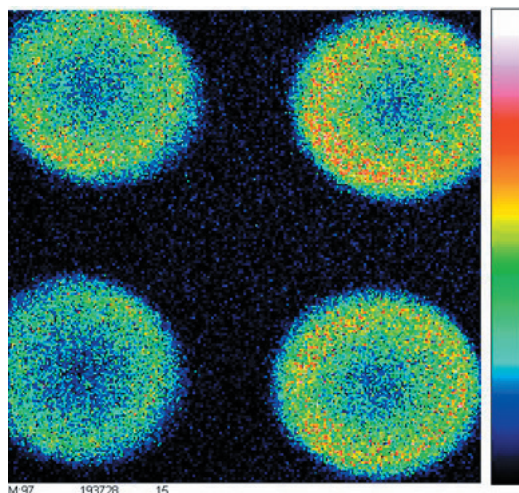


Figure 1. Inkjet Droplets of an organic dye on silicon substrate. NIST TOF-SIMS image, field-of-view 500 μm .

DELIVERABLE: Determine feasibility of ink jet printing of trace organic and metals onto silicon. 2Q 2005

As integrated circuit dimensions shrink to the sub-micrometer regime, there is continued need for accurate and quantitative dopant depth profiling with ultra-high-depth resolution. To probe shallow dopant profiles in Si and other materials, SIMS instruments typically utilize very low energy primary ion beams to bombard the sample surface. In this case, it is difficult to obtain a well-focused and high current density beam, especially in a magnetic sector SIMS instrument. Recently, there has been growing interest in using molecular ion beams for depth profiling. When a molecular primary ion beam impacts the surface, it dissociates into its constituent atoms with each atom retaining a fraction of the initial energy of the cluster. This process can lead to impact energies on the order of a few 10's of electron volts and a corresponding reduction the depth of penetration of the primary ion. This process may potentially allow for ultra high resolution depth profiling. In this project, we will utilize a new C_{60}^+ cluster primary ion beam source at NIST to sputter depth profile Si, GaAs, SiC, and multiple delta-layers test materials.

Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. In these cases, the achievable depth resolution is limited not by the penetration depth of the primary ion but by the topography induced by the sputtering process itself. We will also explore the use of cluster bombardment SIMS for reduction

of sputter induced topography in metal films. This approach will be applied to study depth profiling analysis of gold diffusion in copper and the depth distribution of blanket metals films (copper metalization on silicon).

DELIVERABLES: Improve SIMS depth profile resolution in silicon using large cluster ion beam analysis. Explore the feasibility of reducing sputter induced topography in metal films using cluster SIMS. 3Q 2005

SiGe THIN FILM COMPOSITIONAL STANDARDS

After the need for SiGe compositional standards was discussed at the 14th Annual Workshop on Secondary Ion Mass Spectroscopy (SIMS) in 2001, NIST contacted fabrication and analytical laboratory facilities to develop a reference material using an interactive approach. The typical time frame for an NIST SRM is many years to develop, characterize, and bring to market. The need for SiGe standards was seen as an immediate need, because the current calibration method of Rutherford Backscattering is only accurate from 5 % to 10 % relative and this is insufficient for reliable device production. NIST is collaborating with several semiconductor facilities and analytical laboratories to develop a suite of SiGe compositional standard films. Using an interactive data collection mechanism with collaborators and publishing the data on the web, a faster approach to standard materials production is being developed. This will allow materials to be used and compared even while reference data are being developed.

DELIVERABLE: Develop a suite of SiGe compositional standards to allow accurate and reproducible SiGe thin film production. 4Q 2004

ACCOMPLISHMENTS

IMPLEMENTATION OF C_{60}^+ CLUSTER ION SIMS CAPABILITY

■ Previous efforts with cluster ion sources used for analyzing both organic and inorganic materials have been very successful. Minimization of beam-induced damage in organic materials has allowed depth profiling of polymers such as photoresists and enhanced ion yields for high-molecular weight fragments. Inorganic material analysis has benefitted in the area of ultra-shallow depth-profiling as well as for analysis of some particularly difficult systems such as metal multi-layers stacks. We have investigated the use of a commercially available C_{60}^+ ion source on the NIST

magnetic sector SIMS instrument (see Fig. 2). We have produced stable ion beams of C_{60}^+ and C_{60}^{2+} with typical currents approaching 20 nA under conditions that allow for several hundred hours of operation. The beam can be focused into a spot size of $\sim 1\ \mu\text{m}$ allowing micrometer spatial scale mapping of patterned wafers. Optimal experimental conditions have been defined to allow for depth profiling analysis of silicon wafer samples, delta doped structures and metal multilayers.

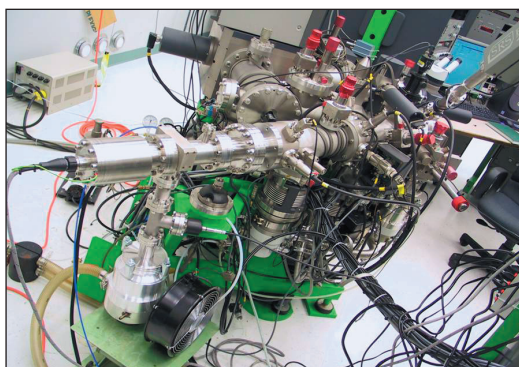


Figure 2. C_{60} ion source mounted on NIST magnetic sector SIMS instrument.

DEPTH PROFILING OF ORGANIC OVERLAYERS USING SIMS

Organic photoresists and low- κ dielectric materials are key components for front end semiconductor processing. There is also a growing interest in the use of organic semiconductor materials for organic light emitting diodes and organic thin film transistors. In anticipation of a growing need for metrology tools to characterize these types of materials, we are developing new approaches to characterize the chemical composition and in-depth distribution of organic thin films on silicon. Typically, the use of ion beam sputtering techniques, such as secondary ion mass spectrometry (SIMS), results in extensive chemical degradation of organic thin films such as photoresists or organic light emitting diodes. However, we have found that cluster primary ion bombardment SIMS can minimize this degradation allowing for intact characteristic ions to be obtained throughout the depth of the film. Furthermore, it appears that analyzing these organic materials at cryogenic temperatures provides further reduction in beam-induced damage. In this project, an SF_5^+ polyatomic primary ion source was used to SIMS depth profile Poly(methyl methacrylate) (PMMA) photo resist at a series of temperatures from 198 K to 398 K where the pri-

mary glass transition for PMMA occurs at 378 K. The depth profile characteristics (*e.g.*, interface widths, sputter rates, damage cross sections, and overall secondary ion stability) were monitored as a function of temperature. It was found that at low temperatures, the secondary ion stability increased considerably. In addition, the interfacial widths were significantly lower. Examples of this increased stability at low temperatures are illustrated in Fig. 3 for the PMMA fragment at $m/z = 69$. Corresponding AFM images indicated that there was also decreased sputter-induced topography formation at these lower temperatures. Higher temperatures were typically correlated with increased sputter rates. However the improvements in interfacial widths and overall secondary ion stability were not as prevalent as was observed at low temperatures. The importance of the glass transition temperature (T_g) on the depth profile characteristics was also apparent. The results of this study demonstrate that it is possible to monitor the chemical composition of photoresist thin layers on silicon by analyzing the samples at cryogenic temperatures.

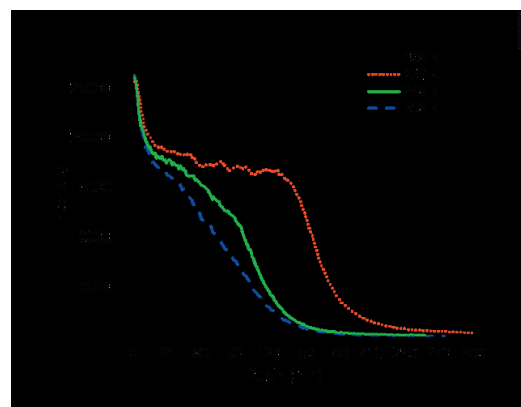


Figure 3. Positive ion intensities of characteristic fingerprint ion of PMMA $m/z = 69$ plotted as a function of depth for a PMMA film on Si ($\sim 160\text{ nm}$): measured at varying temperatures (at and below room temperature).

COMPOSITION DEPTH PROFILING OF Fe/Ni AND Pt/Co MULTILAYERS USING SIMS

Secondary ion mass spectrometry (SIMS) is a powerful technique for the in-depth analysis of solid materials. However, SIMS is difficult to apply for the quantitative analysis of major components due to severe matrix effects. Therefore SIMS is more commonly used for

the quantitative analysis of minor impurities. In this work, a C_{60}^+ ion beam was studied as a sputtering source for the quantitative analysis of binary alloy films and the quantitative depth profiling of multilayer films. Fe/Ni and Pt/Co multilayer thin films were grown on Si (100) wafers by ion beam sputter deposition. Fe-Ni and Pt-Co alloy films were also grown for quantitative surface analysis of major components. The compositions of Fe-Ni alloy thin films were certified by an isotope dilution method using inductively coupled plasma-mass spectrometry (ICP-MS) and those of Pt-Co alloys were certified by ICP-optical emission spectroscopy (OES). Calibration curves were derived from linear fits between the nominal compositions and the SIMS compositions calculated using relative sensitivity factors from reference alloy films ($Fe_{51}Ni_{49}$, $Pt_{40}Co_{60}$) as shown in Figure 4. SIMS depth profiling was performed with a magnetic sector SIMS system using 14.5 keV impact energy C_{60}^+ ions and negative ion detection. The slope of 1.034 and an offset value of -1.89 % in the calibrated SIMS compositions of Fe-Ni alloy films showed a good correlation with nominal compositions. No interface artifacts were found in a depth profile of an Fe/Ni multilayer. However, for Pt-Co alloy films, the calibration line slope was 0.898 and the offset value was 3.04 % due to matrix effects.

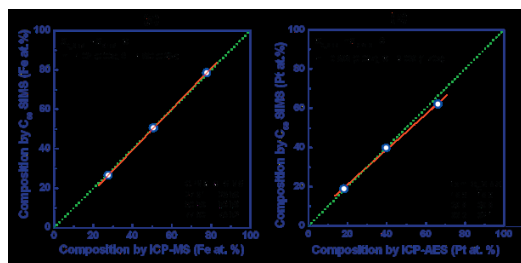


Figure 4. Calibration curves of (a) Fe-Ni and (b) Pt-Co alloy films derived from linear fits using relative sensitivity factors from reference alloy films ($Fe_{51}Ni_{49}$, $Pt_{40}Co_{60}$)

SiGe Compositional Standards – SiGe specimens cut from single-crystal boules normal to the growth axis were obtained from Virginia Semiconductor. The nominal compositions were 3.5 at. % Ge in Si, 6.5 at. % Ge in Si, and 14 at. % Ge in Si. The wafers were evaluated with the electron probe microanalyzer (EPMA) for micro- and macroheterogeneity for use as primary standards for characterization of SiGe thin

films on Si that are needed by the microelectronics industry as reference standards. The specimens were rigorously tested with wavelength dispersive spectrometers (WDS) using multiple point, multiple sample, and duplicate data acquisitions. On each specimen, two 40-point traverses normal to one another were prepared at two randomly selected locations with steps of 2 μm or 5 μm between points. Such traverses are routinely prepared during heterogeneity testing to determine if distinct phases across short distances (5 μm to 100 μm) within specimens are present. In addition random sampling tests on each specimen were run to evaluate the overall specimen heterogeneity. The expanded uncertainties (3σ) in percent mass fraction determined from data for each specimen ranged from 1–2 % in $Si_{.86}Ge_{.14}$ to as high as 15 % in $Si_{.965}Ge_{.035}$. The $Si_{.86}Ge_{.14}$ was chosen as the primary standard for the SiGe films on Si due to the low heterogeneity of this material for which the maximum expanded uncertainty due to heterogeneity is no greater than 1.5 % relative mass fraction for Ge and considerably less for Si.

Round-Robin Study of Arsenic Implant Dose Measurement in Silicon by SIMS – An international round-robin study was undertaken under the auspices of SIMS subcommittee SC 6 of International Organization for Standardization Technical Committee TC 201 on Surface Chemical Analysis. The purpose of the study was to determine the best analytical conditions and the level of interlaboratory agreement for the determination of the implantation dose of arsenic in silicon by SIMS. Motivations for this study were: (a) the relatively poor interlaboratory agreement that was observed in a previous round-robin study before a certified reference material had become available; (b) the observation that the use of Si_3^- as a matrix species combined with AsSi $^-$ detection may result in improved measurement repeatability compared with Si_2^- ; and (c) the observation that point-by-point normalization can extend the linearity of SIMS response for arsenic in silicon beyond $1 \times 10^{16}/cm^2$.

Fifteen SIMS laboratories participated in this study, as well as two laboratories that performed Low energy Electron-induced X-ray Emission Spectrometry (LEXES) and one that made measurements by Instrumental Neutron Activation Analysis (INAA). The labs were asked to determine the implanted arsenic doses in three unknown samples using as a comparator Standard

Reference Material 2134, with a certified dose of 7.33×10^{14} atoms/cm². The use of a common reference material by all laboratories resulted in much better interlaboratory agreement than was seen in the previous round-robin that lacked a common comparator. The relative standard deviation among laboratories was less than 4 % for the medium-dose sample, and somewhat larger for the low- and high-dose samples (see Fig. 5). The high-dose sample showed a significant difference between point-by-point and average matrix normalization because the matrix signal decreased in the vicinity of the implant peak, as previously observed. The average dose from point-by-point normalization was in close agreement with that determined by INAA, indicating that the SIMS relative sensitivity factor approach is valid for arsenic concentrations in silicon as high as 4 atom percent.

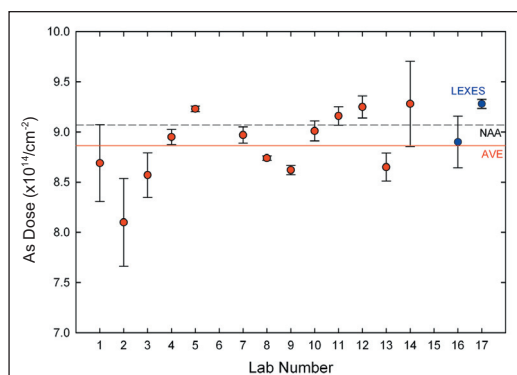


Figure 5. As round robin results for medium dose sample with point-by-point normalization to matrix signal. SIMS lab results shown in red with error bars indicating within-lab repeatability. Relative standard deviation among labs is 3.9 %. Also shown are LEXES results (blue dots), average of SIMS lab results (red line), and NAA result (black dashed line).

Enhanced Performance of Microcalorimeter X-ray Detector – We have previously reported improvements to stability of the microcalorimeter x-ray detector by stabilizing the temperature of the detector to 1 part in 1000. This effort enabled the collection of X-ray spectra over periods of hours which showed resolutions on the order of 12 eV and drifts less than 2 eV. Recently, CSTL scientists working with NIST Boulder have identified the previously observed problem of abrupt jumps in the spectral lines as due to the high-speed pulse feedback loop losing lock and relocking on a different flux quantum. We are investigating hardware improvements to eliminate this problem. We have received from NIST boulder an upgraded microcalorimeter thermometer

including a new Nb superconducting shield. As a result of these modifications, the upgraded CSTL microcalorimeter has obtained a resolution at Mn K α (5.9keV) of 4.39 ± 0.15 eV (see Fig. 6).

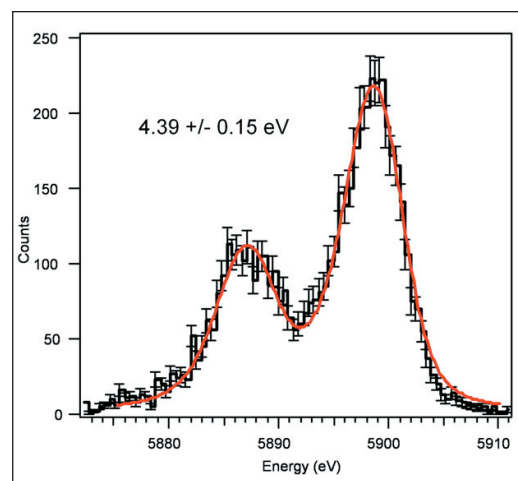


Figure 6. X-ray spectrum taken with the upgraded CSTL microcalorimeter of Mn K α 2 (5.887 keV) and Mn K α 1 (5.898 keV) peaks showing 4.39 eV resolution. Note: No software drift correction has been applied.

Methods for depth-sensitive imaging by Scanning Transmission Electron Microscopy – Recently, researchers have begun to explore the possibility of chemical tomography in the Analytical Electron Microscope (AEM), the determination of 3-D elemental distributions in the sample based on tilt-series of energy-filtered TEM (EFTEM) elemental maps and high-angle annular dark field (HAADF) STEM structural data. One of the chief barriers to this work is that for thicker samples EFTEM maps can show non-monotonic relationships between the observed signal in the 2-D tilt images and the concentration of the analyte in that projected pixel. This violates the projection requirement, a key assumption in many 3-D reconstruction algorithms. Because of this, most successful work to date has been limited to systems that (at least approximately) meet this requirement and do not exhibit the full complexity of interactions possible in the AEM. To get past this hurdle, it is necessary to construct new models for 3-D reconstruction in the AEM that are not based on X-ray tomography predecessors and that explicitly account for effects such as beam spreading, multiple scattering, and through-sample self-absorption. Following the lead of the medical imaging community, one useful step toward the creation of effective 3-D render

construction algorithms is the analysis of synthetic datasets of phantoms with known properties. Figures 7-1, 7-2, and 7-3 show the results from 3-D Monte Carlo simulations of three cylinders (Cu, Al, and SiO₂), each 600 nm in diameter and 1 μ m long. The electron beam (purple line) was rastered over 32 pixels parallel to the x-axis and the resulting X-ray spectra at the XEDS detector were calculated, resulting in spectrum-line profiles for each tilt from 0 degrees to 180 degrees. From the 5,760 spectra calculated, chemical sinograms were extracted by summing the intensities in 130 eV wide windows over the Cu K α , O K α , and Al K α peaks and displaying them as the channels of an RGB image (Fig. 7-4). These data display both beam broadening and pronounced self-absorption effects, but not Bragg scattering or dynamical interactions, two other effects that plague 3-D AEM.

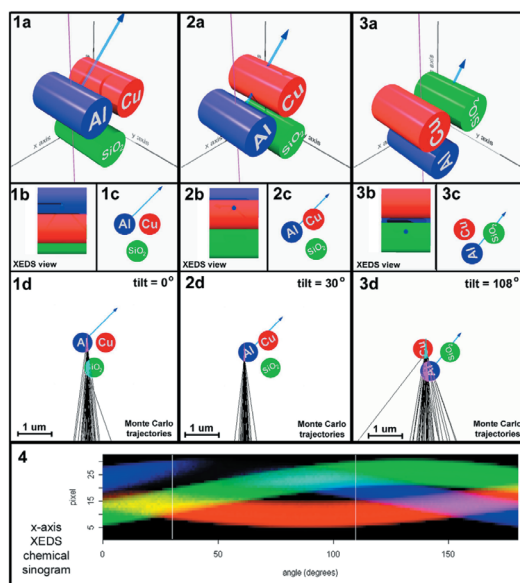


Figure 7. 1(a) 0 degree tilt perspective view of AEM cylinder phantoms (600 nm diameter by 1 μ m long); blue arrow points to XEDS detector. (b) same phantoms as seen by XEDS detector. (c) view along tilt axis. (d) 300 keV Monte Carlo electron trajectories. 100 electrons displayed at 1 of 32 horizontal beam raster locations. Figures 2 & 3 same as Figure 1 but sample tilted to 30 degrees and 108 degrees respectively. Figure 4. "Chemical sinogram" displaying XEDS line intensities vs. sample tilt angle (horizontal axis) and x-axis beam raster position (vertical axis). Red is Cu K α , green is O K α , and blue is Al K α . Vertical white lines denote 30 degrees and 108 degrees. Note attenuation of Al K α by Cu cylinder near 30 degree tilt.

CHARACTERIZATION OF THE HIGH- κ /METAL GATE INTERFACE

Measurement of the barrier height and determination of the band structure is not straightforward. Recent work by numerous researchers has shown that the measured band offset between a metal gate electrode and high- κ gate dielectric is dependent on numerous factors including composition, structure, and thickness of both the metal gate electrode and the high- κ dielectric. Because of limitations associated with any single technique, we believe that determination of band offsets and work functions requires the use of an array of techniques and the broad expertise available at NIST. We will focus our efforts on the following measurements: standard Capacitance-Voltage (C-V) and tunneling current-voltage (I-V) measurements, internal photoemission (IPE), scanning kelvin probe microscopy (SKPM), and soft X-ray and inverse photoelectron spectroscopy (in collaboration with Rutgers University).

Internal Photo Emission (IPE) – An HfAlO film on a p-type silicon substrate was fabricated by Atomic Layer Chemical Vapor Deposition (ALCVD). Targeted film composition, designated by 25 [5 HO : 1AO], was deposited by 5 cycles of H₂O/TMA precursor followed by 1 cycle of H₂O/HfCl₄ precursor and repeated 25 times. The film thickness of 93 Å and the optical bandgaps E_g of 5.76 eV were obtained from modeling the VUV-SE data. MOS capacitors were fabricated for the film by evaporation of 13 nm thick Al electrodes of 0.023 mm² size. IPE measurement was performed in the photon energy range from 1.5 eV to 6.0 eV. The quantum yield (Y) was obtained by normalizing the measured currents to the incidence flux. The spectral threshold was determined by extrapolating $Y^{1/2}$ plot to zero yield. As a result, Fig. 8a shows the negatively biased IPE spectra from which Φ_e (Al), the barrier threshold from the Fermi level to the bottom of the conduction band of HfAlO, was determined to be ~2.4 eV. When positively biased as shown in Fig. 8b, the IPE spectra yield a barrier height of ~3.2 eV corresponding to the threshold from the silicon valence band to the bottom of the HfAlO conduction band. Both of these values agree with the published data within 0.1 eV. Also a slight feature in the positive bias spectra (Fig. 8b) was observed at ~5.7 eV which is attributed to the optical excitation in the HfAlO film; it is the same as the optical bandgap E_g measured by VUV-SE.

DELIVERABLES: Demonstrated the performance of IPE tool on metal/high- κ /Si structure to determined band offsets and compare with values in literature. 1Q 2005.

DELIVERABLES: Complete measurements of a set of HfO₂ and HfSiO using vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), X-ray diffraction (XRD), Atomic force microscopy (AFM), and FTIR Grazing Angle Attenuated Total Refection (FTIR-GATR). 3Q 2005.

DELIVERABLES: Determine Optical constants for Ti-Ni-Pt ternary system using vacuum ultraviolet spectroscopic ellipsometry. 3Q 2005.

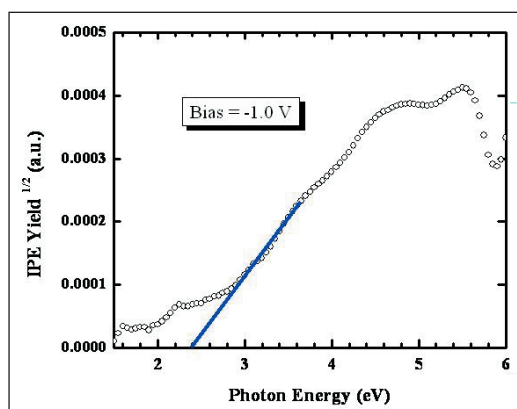


Figure 8a. IPE spectra from a negatively IPE spectra for HfAlO/Al system. Φ_e (Al), the barrier threshold from the Fermi level to the bottom of the conduction band of HfAlO, was determined to be ~ 2.4 eV.

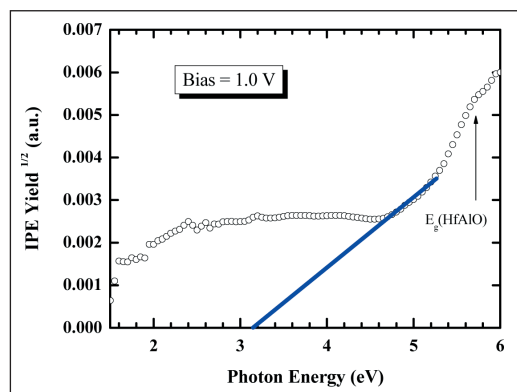


Figure 8b. IPE spectra for a positively biased HfAlO/Al system. A feature was observed at ~ 5.7 eV which is attributed to the optical excitation in the HfAlO film and is the same as the optical bandgap E_g measured by VUV-SE.

Scanning Kelvin Probe Microscopy (SKPM)

– Kelvin probe is a non-invasive, non-contact vibrating capacitor technique, which measures the voltage between a vibrating micro-electrode and a conducting or semiconducting sample with millivolt resolution. The surface potential measurement contains information on the sample's work function. Baseline measurements of well known inert metals such as gold and platinum (on SiO₂/Si) will validate the procedures and interpretation of the scanning Kelvin probe measurements. Unlike C-V, I-V, or IPE, Kelvin probe measures the surface work function of the metal gate electrode. This surface work function may or may not directly relate to the interfacial band offsets. However, a change in the surface work function will provide important clues necessary to understand the band offsets and final device threshold voltage. We are developing a mask set that will permit the comparison of Kelvin probe with standard C-V on a given wafer. We also explored surface treatments necessary to obtain a valid metal work function. The optimization of sample preparation and the careful characterization of the SKPM tip work function have yielded excellent agreement of seven sample metal work functions to literature values as shown in Fig. 9.

DELIVERABLES: Compare metal work functions obtained from SKPM with measurements made by CV technique on a ternary metal/high- κ system fabricated by combinatorial techniques. 3Q 2005.

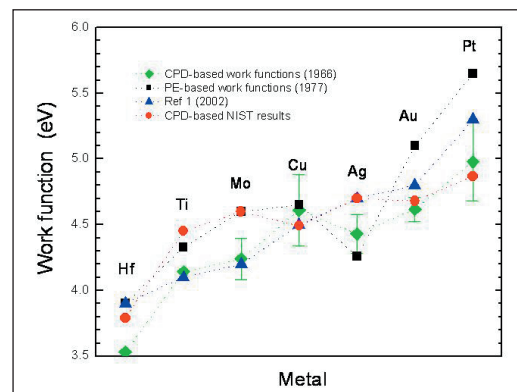


Figure 9. Comparison of metal work function obtained from the NIST SKPM with literature values. The agreement is good after the optimization of sample preparation and analysis procedure.

COLLABORATIONS

FM Technologies – High brightness oxygen ion source for 2-D dopant profiling by SIMS

International SEMATECH, Joe Bennett – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers

Ionoptika – Development of a C_{60}^+ primary ion source for advanced semiconductor technology

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces

Peabody Scientific – Ion source development for Semiconductor SIMS

SEMATECH, Characterization of metal gate/high- κ systems.

University of Maryland, College Park, Ultra-thin gate oxide reliability.

University of Minnesota, Alternate Gate Dielectrics.

MSEL, Characterization of metal gate/high- κ systems.

IBM, Electrical characterization of high- κ systems.

Texas Instruments, Electrical characterization of high- κ systems.

Rutgers University, Characterization of metal gate/high- κ systems.

Yale University, Electrical characterization of high- κ systems.

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E. Windsor, G. Gillen, D. Bright, P. Chi, A. Fahey and J. Batteas, “Techniques for Improving SIMS Depth Resolution: C_{60}^+ Primary Ions and Backside Depth Profile Analysis” Proceedings of the 2005 International Conference on Characterization and Metrology for ULSI Technology, American Institute of Physics Press, Submitted for publication.

K.J. Kim, D.W. Moon, P. Chi and D. Simons, “Development and Applications of Multiple Delta-Layer Reference Materials for Semiconductor Analysis,” *J. Surf. Anal.*, accepted for publication.

D.S. Simons, P.H. Chi and K.J. Kim, “Quantitative Measurement of Arsenic Implant Dose by SIMS,” *J. Surf. Anal.*, accepted for publication.

K.J. Kim, D.W. Moon, P. Chi and D. Simons, “Development of B-doped Si Multiple Delta-Layer Reference Materials for SIMS Profiling,” *Surf. Interface Anal.*, submitted for publication.

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CHEMICAL METROLOGY OF MATERIALS

GOALS

To provide industry with new and improved measurements, models, data and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. Major focus is placed on metrology requirements from the 2004 update of the 2003 International Technical Roadmap for Semiconductors expressed as difficult challenges: (1) Measurement of complex materials stacks and interfacial properties including physical and electrical properties, (2) Structural and elemental analysis at device dimensions, and (3) Nondestructive production worthy wafer and mask level microscopy for critical dimension measurement for 3-D structures, overlay, defect detection, and analysis.

CUSTOMER NEEDS

Materials with high dielectric constants such as HfO_2 , ZrO_2 , HfSiO_4 , and ZrSiO_4 are candidate "high- κ " gate-dielectric materials in future semiconductor devices. These materials can have larger physical thicknesses than SiO_2 in order that the equivalent oxide thickness (corresponding to an SiO_2 dielectric) can be reduced. For devices produced between 2006 and 2009, the equivalent oxide thickness will be between 0.7 nm and 1 nm for high-performance logic and between 1.6 nm and 1.9 nm for low-operating-power logic. These thicknesses need to be measured with an uncertainty (3σ) of $\pm 4\%$.

X-ray photoelectron spectroscopy (XPS) is a frequently used technique for characterizing thin-film materials and for measuring thicknesses of gate-oxide films. Commercial tools are now available for such XPS measurements on 300 mm wafers. The material parameter needed for measuring thicknesses of overlayer films by XPS is the effective attenuation length (EAL). EAL data are needed for candidate high- κ materials for common XPS measurement conditions.

Auger-electron spectroscopy (AES) is extensively used for the characterization of defects on wafers. Although commercial AES instruments have a lateral resolution of about 10 nm, the detected Auger signal will typically originate from much larger regions due to the effects of backscattered electrons. Part of the detected signal arises from ionizations created by the primary beam while

another part comes from ionizations by backscattered electrons. An analyst often needs to make a compromise between making AES measurements at a relatively high beam energy of 25 keV (to optimize the lateral resolution) and making these measurements at much lower beam energies (to reduce the fraction of the detected Auger signal due to backscattered electrons or to reduce charging). Data are needed for the dependence of the analytical area on beam energy for common analytical situations. Such data require more reliable information on electron stopping powers over a wide range of electron energies (typically 100 eV to 30 keV) so that calculations of backscattering factors and analytical areas can be made by efficient Monte Carlo simulations.

TECHNICAL STRATEGY

Calculation of Electron Effective Attenuation lengths – NIST is developing a new database (SRD 100) Simulation of Electron Spectra for Surface Analysis (SESSA) to be used for AES and XPS analyses of thin-film structures. SESSA can be used for two main applications. First, data are provided for many parameters needed in quantitative AES and XPS (differential inverse inelastic mean free paths, total inelastic mean free paths, differential elastic-scattering cross sections, total elastic-scattering cross sections, transport cross sections, photoelectric cross sections, photoelectric asymmetry parameters, electron-impact ionization cross sections, photoelectron line shapes, Auger-electron line shapes, fluorescence yields, and Auger-electron backscattering factors). Second, Auger-electron and photoelectron spectra can be simulated for layered samples. The simulated spectra, for layer compositions and thicknesses specified by the user, can be compared with measured spectra. The layer compositions and thicknesses can then be adjusted to find maximum consistency between simulated and measured spectra. In this way, AES and XPS can provide more detailed characterization of multilayer thin-film materials.

SESSA is being used to compute EALs for thin films of HfO_2 , ZrO_2 , HfSiO_4 , and ZrSiO_4 on a Si substrate. These EALs are determined as a function of film thickness and photoelectron emission angle (*i.e.*, to simulate the effects of tilting the sample in so-called angle-resolved XPS). The calculations were made for excitation by Al K α X-rays on an XPS instrument with a fixed angle

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of 54 degrees between the X-ray source and the analyzer axis, a common experimental configuration.

DELIVERABLES: Determine electron effective attenuation lengths for XPS thickness measurements of candidate high- κ gate-dielectric materials. 2Q 2005

Calculation of Electron Stopping Powers

– Electron stopping powers are being calculated for groups of elemental solids and selected compounds for electron energies between 100 eV and 30 keV. These calculations are based on the same algorithm as that used successfully to compute electron inelastic mean free paths.

A simple equation developed by Bethe has frequently been utilized to describe the dependence of the stopping power on electron energy and material parameters. Although it is known that this equation is invalid for electron energies lower than about 10 keV, the Bethe stopping-power equation has often been used in Monte Carlo simulations of electron transport in solids on account of its analytical simplicity. Efforts are currently underway to fit alternative expressions to the new set of calculated electron stopping powers.

DELIVERABLES: Test candidate analytical expressions for electron stopping powers. 4Q 2005

ACCOMPLISHMENTS

■ **Calculations of Electron Effective Attenuation Lengths** – A new NIST database for the Simulation of Electron Spectra for Surface Analysis (SESSA) has been developed for applications in AES and XPS. Electron effective attenuation lengths (EALs) were computed from SESSA for XPS experiments in which the attenuation of substrate Si 2p photoelectrons is measured through thin overlayer films of HfO_2 , ZrO_2 , HfSiO_4 , and ZrSiO_4 as a function of film thickness and photoelectron emission angle. These EALs were compared to similar values obtained from the NIST Electron Effective-Attenuation-Length Database (SRD 82). Generally good agreement was found between corresponding EAL values, but there were differences for film thicknesses less than the inelastic mean free path of the photoelectrons in the overlayer film. These differences are due to a simplifying approximation in the algorithm used to compute EALs in SRD 82. SESSA, with realistic cross sections for elastic and inelastic scattering in the film and substrate materials, is believed to provide more accurate EALs than SRD 82 for thin-film thickness measurements

by XPS, particularly in applications where the film and substrate have different electron-scattering properties (such as the high- κ materials considered here).

Calculations of Electron Stopping Powers

– Electron stopping powers (SPs) were calculated for ten elemental solids (Al, Si, Cr, Ni, Cu, Ge, Pd, Ag, Pt, and Au). These calculations were made for electron energies between 100 eV and 30 keV. The calculated SPs were compared with measured values, with results of other calculations, with the non-relativistic Bethe SP equation, and with an empirical modification of the Bethe equation. Generally satisfactory agreement of the calculated SPs was found with measured values for some solids (Ni, Cu, Pd, and Pt) and limited agreement for others (Al, Si, Cr, Ge, and Ag). There was similarly agreement between the calculated SPs and some results of others, while there was some disagreement in other cases. The calculated SPs agreed with values from the Bethe equation only for energies above 10 keV (for $Z \leq 32$) and about 30 keV for $Z \geq 46$. Satisfactory agreement was found between the SPs and values from an empirical modification of the Bethe equation for Al, Si, Cr, Ni (for energies above 1 keV), Cu, and Ge but there was less agreement for Pd and appreciable disagreement for Au. As an example, Fig. 1 shows the recent NIST results (designated

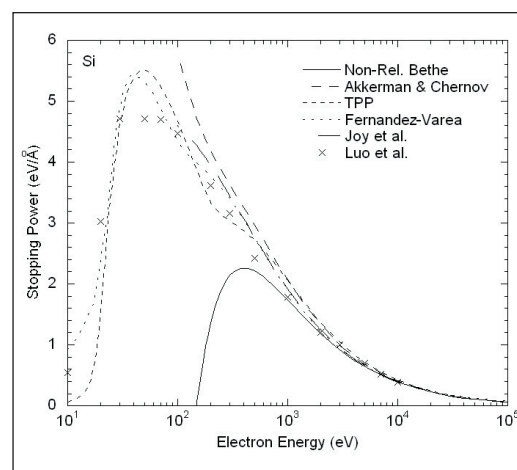


Figure 1. Stopping power for silicon as a function of electron energy. The short-dashed line designated TPP denotes the NIST calculated stopping powers; the dashed lines designated Akkerman and Chernov show results of other calculations; the solid line shows results from the non-relativistic Bethe equation; the long-dashed line denoted Joy et al. shows results from an empirical modification of the Bethe equation; and the symbols denoted Luo et al. show experimental results of Luo et al.

TPP) together with SP data from other sources. In addition, an analysis of the calculated SPs for Al was made to show why the Bethe equation is not expected to be valid unless the electron energy is larger than about 10 keV.

COLLABORATIONS

Institute of General Physics, Technical University of Vienna, Prof. Werner and Mr. Smekal, development of the new NIST database for simulation of electron spectra for surface analysis by AES and XPS, and calculation of electron effective attenuation lengths for XPS measurements of thicknesses of high- κ gate dielectrics on silicon.

Institute of Physical Chemistry (Warsaw), Dr. Jablonski, calculations of electron backscattering factors (for scanning Auger microscopy), and analyses of electron stopping powers.

National Institute for Materials Science (Tsukuba), Dr. Tanuma, calculations of electron stopping powers, and analyses of stopping-power data.

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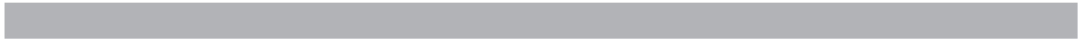
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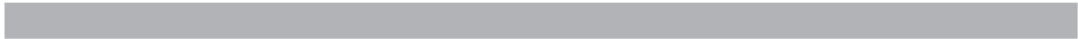


INTERCONNECT AND PACKAGING METROLOGY PROGRAM

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.



ATOMIC LAYER DEPOSITION – PROCESS, MODELS, AND METROLOGY

GOALS

Develop validated, predictive process models and *in situ* metrologies for atomic layer deposition processes.

CUSTOMER NEEDS

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high- κ gate dielectric layers, diffusion barrier layers, copper seed layers, and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the 2003 *International Technology Roadmap for Semiconductors (ITRS)* as “one of the few enabling methodologies that can reduce development cycle times and costs.” [2003 ITRS, *Modeling and Simulation*, page 1] Important aspects of TCAD include “simulation tools that predict physical properties of materials and, in some cases, the subsequent electrical properties”; and a “hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings.” [2003 ITRS, *Modeling and Simulation*, page 1] Further, it is expected that “Simulations that can predict the impact of process conditions of film morphology as well as interface characteristics will become increasingly important.” [2003 ITRS, *Modeling and Simulation*, page 15] However, many difficult challenges to development of validated, predictive ALD process models that allow prediction of equipment influences on film properties have been identified, including “Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high- κ metal gate); reaction mechanisms, and reduced models for complex chemistry.” [2003 ITRS, *Modeling and Simulation*, Table 121, page 2] In addition to a lack of quality fundamental physical and chemical data, experimental validation has been identified as a “key difficult challenge across all modeling areas.” [2003 ITRS, *Modeling and Simulation*, page 1] Further, with respect to experimental

validation, “The major effort required for better model validation is without doubt sensor development.” [2003 ITRS, *Modeling and Simulation*, page 15] This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and associated *in situ* metrologies for ALD processes.

TECHNICAL STRATEGY

ALD process models are being developed by incorporating the detailed chemical reaction mechanisms developed in the course of this project into commercially available computational fluid dynamics (CFD) codes that simulate the flow and temperature fields in an ALD reactor. Experimental validation of the overall process model is accomplished by modeling the performance of custom-built, research-grade ALD reactors with optimized optical accessibility and benchmarking the numerical results with experimental data. These data are obtained using various measurement techniques, including vibrational spectroscopies and mass spectrometry. The focus of this work is on Al_2O_3 and HfO_2 ALD. The experimental component of this project is directed at HfO_2 ALD. However, the initial chemical mechanism development has focused on a different system: deposition of Al_2O_3 from trimethyl aluminum and water. This initial system was selected for two reasons. First, there has been significant work on Al_2O_3 ALD, and consequently, there are adequate experimental data for use in chemical mechanism validation. Second, aluminum is more amenable to quantum calculations than hafnium, a transition metal. The chemical mechanism work will be extended to the HfO_2 system, once a good understanding of detailed chemistry for Al_2O_3 ALD is developed.

This project involves two primary directions: development of *in situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that the important reaction species will be identified as the understanding of a particular ALD reaction im-

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proves, thus facilitating the design of improved process metrologies. While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

1. The first step in providing validated ALD process models is evaluating the suitability of diagnostics that are sensitive to ALD chemistry. Mass spectrometry and optical spectroscopic techniques are of particular interest because of their potential for *in situ* monitoring. While sensors that are sensitive to gas phase species (*e.g.*, mass spectrometry and Fourier-Transform infrared (FTIR) spectroscopy) are easier to integrate into commercial reactors (*e.g.*, in the gas exhaust line), these techniques are only sensitive to volatile species. Hence, it is sometimes difficult to relate the species detected with such techniques to mechanisms of interest on the growth surface. Therefore, in addition to gas phase sensors, surface-sensitive techniques are also being evaluated to directly probe ALD surface chemistry. The suitability of Raman spectroscopy and FTIR spectroscopy for probing ALD surface processes under actual deposition conditions is being investigated. In addition, the suitability of mass spectrometry and FTIR spectroscopy for probing gas phase ALD processes and how best to relate gas phase species to important surface processes is being investigated. Research-grade ALD reactors with optimized accessibility for the various gas-phase-sensitive and surface-sensitive techniques have been designed and constructed. After various diagnostics are evaluated in these test ALD reactors, a more industrially relevant ALD reactor will be designed and built. Suitable diagnostics will be integrated into this reactor to provide data that will aid in chemical mechanism development and overall process model validation.

DELIVERABLES: Complete evaluation of *in situ* Raman spectroscopic measurements for probing ALD surface processes [3Q 2005]. Complete evaluation of *in situ* FTIR measurements for probing ALD gas phase processes [3Q 2005]. Complete evaluation of *in situ* FTIR measurements for probing ALD surface processes [4Q 2005]. Interface mass spectrometer with ALD chamber [4Q 2005].

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD and chemical vapor deposition (CVD) is an important aspect of this project and is an ongoing process. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity compiles and evaluates currently available thermochemical and chemical kinetic data for organometallic compounds and related precursors. The second activity supplements available data by using *ab initio* and semi-empirical quantum calculations coupled with transition state calculations to develop detailed chemical kinetic models from computed molecular structures, thermodynamic properties and spectroscopic properties of relevant compounds. The third activity utilizes the experimental and computed thermochemical and chemical kinetic data to develop detailed chemical kinetic models for the decomposition of organometallic precursors and deposition processes leading to thin film growth.

DELIVERABLES: Compilation of bibliography pertaining to ALD and CVD systems. Make this information available through the Standard Reference Data website [ongoing]. Utilize and refine detailed chemical kinetic model for ALD of Al_2O_3 from trimethyl aluminum (TMA) and water based on reactor flow simulations and additional quantum calculations [3Q 2005]. Include steps in detailed chemical kinetic model to simulate carbon incorporation in Al_2O_3 ALD [3Q 2005]. Perform high level *ab initio* quantum calculations for small AlH_2X species ($\text{X}=\text{H}, \text{F}, \text{Cl}, \text{OH}, \text{NH}_2, \text{CH}_3$) to benchmark heats of formations and bond dissociation energies [3Q 2005]. Develop simple model for HfO_2 ALD from tetrakis(dimethylamino) hafnium and water [4Q 2005]. Investigate possibility of using shock tube measurements to determine bond dissociation energies of metal precursors used in ALD [4Q 2005].

3. An effort is also being made to investigate the relationship between ALD reactor conditions and concomitant HfO_2 film properties. This relationship is being investigated by correlating the results of a variety of *ex situ* film characteriza-

tion measurements to reactor conditions as determined by *in situ* measurements and numerical modeling of the temperature and flow fields in the reactor. *In situ* measurement techniques include those techniques being developed for model validation. *Ex situ* measurement techniques include vacuum ultraviolet spectroscopic ellipsometry (VUV-SE), FTIR spectroscopy, X-ray photoelectron spectroscopy, X-ray diffractometry, and ultraviolet Raman spectroscopy. The data provided by these measurements, spatially resolved when possible, would include such film characteristics as thickness, stoichiometry, HfO₂ phases present, and degree and type of impurity incorporation.

DELIVERABLES: Complete a preliminary investigation of relationship between ALD process parameters, reactor flow and temperature fields, gas phase species identities and concentrations, and resulting ALD film characteristics [4Q 2005].

ACCOMPLISHMENTS

■ **ALD Reactor Construction** — Research-grade, optically-accessible ALD reactors have been designed and constructed with full optical access for surface and gas-phase Raman and FTIR spectroscopic measurements.

■ **HfO₂ ALD** — A pulsed gas delivery system was designed and constructed. ALD HfO₂ films were deposited under a variety of process parameters using tetrakis(dimethylamino) hafnium, Hf[N(CH₃)₂]₄, and water. Films have been characterized with a number of techniques, including VUV-SE (Fig. 1).

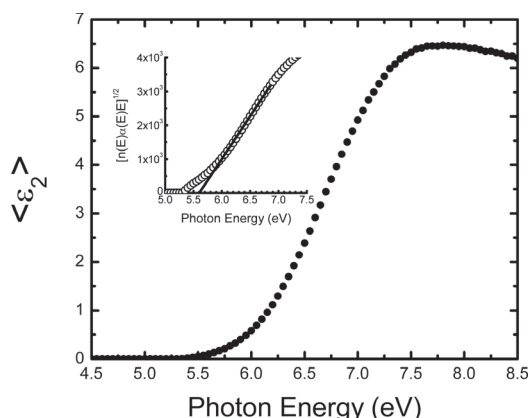


Figure 1. Imaginary part of the complex dielectric function as a function of photon energy for HfO₂ ALD film as determined using VUV-SE. The inset illustrates determination of band gap energy by extrapolation of the expression $[n(E) \cdot \alpha(E) \cdot E]^{1/2}$ to zero (data courtesy of N.V. Nguyen).

■ ***In Situ* Optical Measurements** — *In situ* surface Raman spectroscopic measurements are on going. Excitation wavelengths are being varied to evaluate maximum sensitivity to ALD species. The *in situ* gas phase and surface FTIR systems have been assembled and preliminary measurements have begun.

■ **Chemical Properties Calculations** — Molecular structures and energies for precursors, adsorbates, intermediates, and transition states have been calculated using ab initio and density functional theory quantum calculations for ALD of Al₂O₃ from TMA and water. Prototypical small cluster (Al_xO_yH_z) species have been utilized to represent the surface layer. Rate expressions based on calculated structures and energies have been derived using transition state theory (Fig. 2).

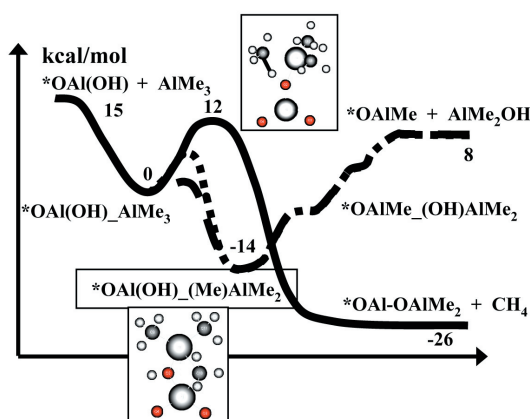


Figure 2. Calculated potential energy surface for reaction of trimethyl aluminum with a hydroxylated aluminum oxide cluster.

A detailed chemical kinetic model for ALD of Al₂O₃ from TMA and water has been constructed based on these rate expressions. This model is being refined based on further reactor model simulations, comparison with experimental observables, and supplemented with additional quantum calculations, where necessary. High level ab initio calculations, up to CCSD(T)/aug-cc-pVnZ (n=2-4) have been done for small species to benchmark heats of formation and bond dissociation energies for AlH_nX species (n = 0-2, X = H, F, Cl, OH, NH₂, CH₃). Additional calculations will be done to provide higher level corrections (*e.g.*, core-valence, relativistic, etc).

■ **Database Website** — A Website <http://srdata.nist.gov/ckmechx/> (external) and <http://h105097.nist.gov/ckmechx> (internal) has been made available through the NIST Standard Reference

Data website. This site currently contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, Al_2O_3 , and other related ALD systems (e.g., Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions.

■ **ALD Reactor Modeling** — A two dimensional CFD model has been developed based on the dimensions of the experimental ALD reactor(s). Numerical solutions have been obtained for flow and a heated substrate with and without full chemistry for ALD of Al_2O_3 from TMA and water.

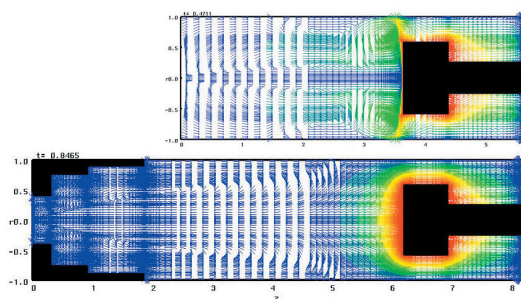


Figure 3. Two numerical simulations of the flow fields in the ALD reactor with different chamber flow geometry. Flow is from left to right. The gas temperature and velocity is represented by the color scale and vector diagrams, respectively. The top figure shows a simulation with plug gas injection and the bottom figure shows a simulation of gas injection with a conical transition region. The top figure exhibits significant gas recirculation zones while the bottom figure exhibits much more uniform flow and temperature fields.

Simulations of OH and CH_3 surface coverages agree well with experimental measurements reported in the literature. Work is ongoing in adjusting rate expressions to reproduce experimental growth rates.

■ This ALD project relies heavily on experience obtained in the course of a previous project investigating silicon thermal CVD via silane pyrolysis. That CVD project also involved development of chemical reaction mechanisms and experimental measurements to support mechanism development and process model validation. Multiple CVD process models were constructed employing the silane pyrolysis mechanisms, including gas phase nucleation of silicon particles, developed during this project and validated using the experimental results obtained in the course of this project. The

different models employed reaction mechanisms of varying complexity and reactor geometries of varying dimensionality. Experimental measurements were performed in a vertical flow, rotating disk reactor under various process conditions. Gas temperature profiles were determined using rotational Raman spectroscopy. Gas phase silicon particle spatial distributions were determined with elastic light scattering. The extent of precursor decomposition and the chemical composition of the gas-phase-nucleated particles were investigated with vibrational Raman spectroscopy. A Website (<http://www.cstl.nist.gov/div836/836.02/cvd/top-page.html>) has been established in order to disseminate the numerical and experimental results obtained from this investigation

RECENT PUBLICATIONS

J. E. Maslar and W. S. Hurst, "In Situ Optical Diagnostics of Silicon Chemical Vapor Deposition Gas-Phase Processes," *Characterization and Metrology for ULSI Technology: 2003 International Conference*, edited by D. G. Seiler et al., AIP Conference Proceedings 683, Melville, NY: American Institute of Physics, 2003, pp. 748-752.

D.R. Burgess, Jr., J.E. Maslar, W.S. Hurst, E.F. Moore, W.A. Kimes, and N.V. Nguyen, "Atomic Layer Deposition – Process Models and Metrologies," *Characterization and Metrology for ULSI Technology: 2005 International Conference*, AIP Conference Proceedings, 2005, in press.

SUPERCONFORMAL DEPOSITION COPPER AND ADVANCED INTERCONNECT MATERIALS

GOALS

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity metallizations, examining the generality of the superconformal filling mechanism and exploring processes utilizing novel barriers and/or seed geometries.

CUSTOMER NEEDS

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to “superconformally” fill high aspect ratio features has made electrodeposited copper the interconnect material of choice in silicon technology. However, the move to ever smaller dimensions has led to the rise of new challenges, including fabrication of ever thinner copper seeds that are required for the copper superfill process and increased resistivities of the metallizations due to size effects. To overcome these hurdles the National Institute of Standards and Technology (NIST) has a program focusing on new fabrication techniques such as seedless processing, and evaluation of the factors affecting electrical resistivity of sub-100 nm wires as well as enhancing existing copper technology through improved understanding of the fundamentals of the superfill process.

Interconnect metallization issues are discussed in the Interconnect section of the 2004 update of the International Technology Roadmap for Semiconductors

TECHNICAL STRATEGY

To meet future industrial needs, we have developed the metrology and fully disclosed copper electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. We have also developed electrolytes and metrology for superconformal deposition of advanced interconnect materials such as silver (the only metal with a higher conductivity than copper) and gold (metallization for compound semiconductors) as well as alternative processing schemes such as chemical vapor deposition (Fig. 1A).

Current metallization technology employs three layers, a barrier metal, typically tantalum, a PVD copper seed and electrodeposited copper. As feature sizes continue to shrink the resistive barrier materials may account for an increasing portion of the cross-sectional area and thus negatively impact electrical performance. These difficulties have driven a search for alternative barrier materials and processes. Ruthenium is a particularly attractive candidate because its electrical and thermal conductivities are approximately twice those of conventional tantalum barriers and ruthenium and copper are immiscible. Substitution of a noble metal barrier/seed layer for the current Ta/Cu technology promises the combined advantages of process simplification and enhanced performance.

Our preliminary work in this area revealed an interesting sensitivity of trench filling behavior to the manner in which the ruthenium barrier layer was treated prior to plating.

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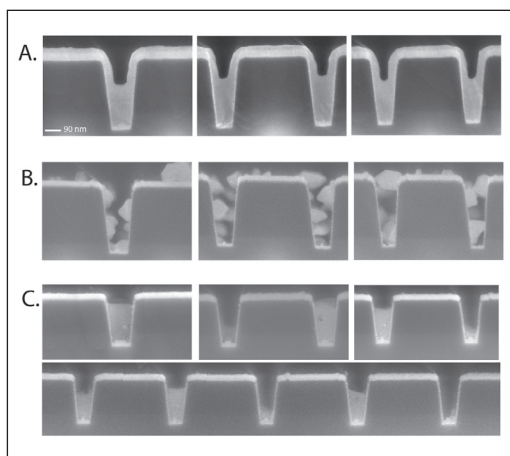


Figure 1. Nucleation and growth of copper on ruthenium is a sensitive function of the initial surface state. Three limiting behaviors are shown: A. Exemplifies the desired result, namely, early coalescence of the electrodeposited copper followed by superfilling that is characteristic of growth on conventional a copper seed-layer; B. Volmer-Weber growth mode characteristic of poor copper wetting on oxidized ruthenium and consequently poor trench filling; and C. Selective growth within the feature that is observed sporadically in a few specimens.

DELIVERABLES: Publications detailing copper superfilling directly on ruthenium barriers (2Q 2005).

A clear understanding of these observations will be required to establish a robust manufacturing process. Voltammetry is a particular powerful tool for examining the surface state of ruthenium and the effect of various surface pretreatments on superfilling behavior. As shown below (Fig. 2), a two-dimensional wetting layer or “underpotential deposited copper” rapidly forms on a ruthenium surface that is first activated by reduction at negative potentials. In contrast, on an oxidized ruthenium surface copper deposition proceeds by the undesirable Volmer-Weber growth mode and poor trench filling results (e.g., Fig. 1B).

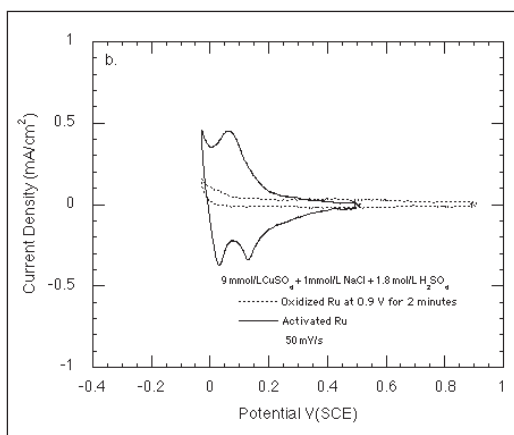


Figure 2. The deposition and stripping of a 2-D copper layer on an oxide-free ruthenium surface. Oxidation of ruthenium at high potentials inhibits this process with negative consequences for morphological evolution during bulk copper deposition as well as poor interfacial adhesion.

As feature widths and seed-layer dimensions decrease a move to Atomic Layer Deposition (ALD) of the barrier layer is anticipated. Successful process integration will require close control of the surface chemistry of the barrier and consideration of the terminal effect (potential drop associated with highly resistive seed-layer) and the consequences of potential-dependent morphological evolution during copper electroplating. Formative steps examining these issues are underway in collaboration with the University of Helsinki (Fig. 3).

DELIVERABLES: Publication on seedless trench superfilling of copper directly deposited on ALD barrier layers. (4Q 2005).

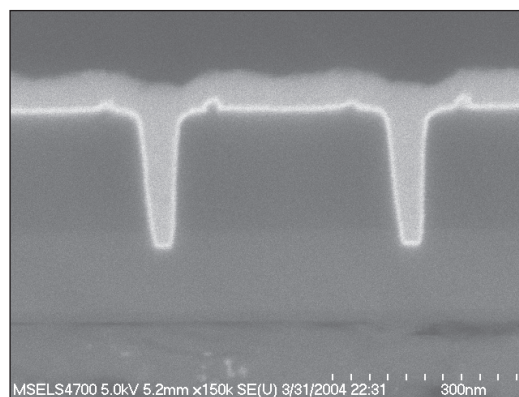


Figure 3. Trenches superfilled with copper electrodeposited directly on an ALD iridium layer (thin bright layer).

A new effort this year focused on exploring gold metallization for III-V semiconductors such as GaAs and GaN. In analogy to silicon technology the push to higher device density may require a move to Damascene processing of compound semiconductors. The first demonstration of void-free bottom-up filling of trenches by gold electrodeposition was recently published by NIST. Further work is underway to quantitatively describe the process (Fig. 4).

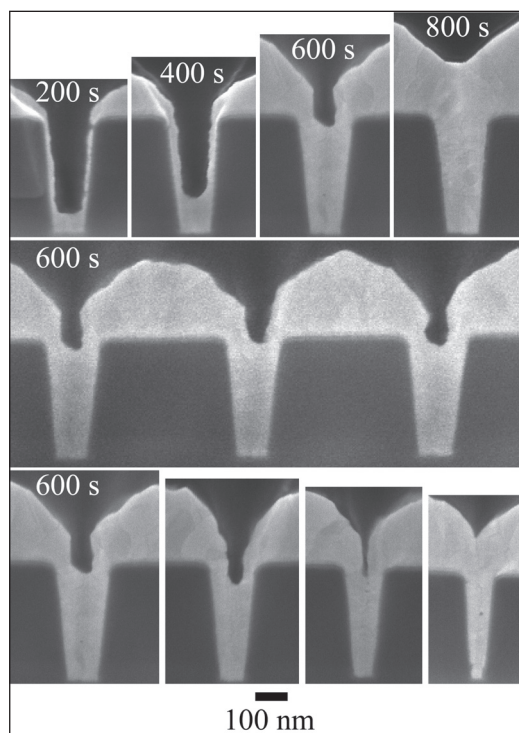


Figure 4. Void-free filling of trenches with gold. The gold seeded substrates were first derivatized with a sub-monolayer of lead followed by electrodeposition in gold cyanide electrolyte for the times shown.

DELIVERABLES: Publication detailing void-free trench filling with gold (2Q 2005).

One of our newest publications extends our Curvature Enhanced Accelerator Coverage (CEAC) mechanism to include the impact of catalyst consumption. While such consumption degrades superfilling ability of the electrolyte, and leads to undesirable incorporation of impurities in the deposit, it is a very real phenomenon.

DELIVERABLES: Published two invited papers; IBM Journal of Research (2Q 2005) and The Electrochemical Society's news journal Interface (1Q 2005). These papers present a synopsis of the substantial output of the NIST superfill effort to the most relevant industrial audience.

Further surface analytical and electroanalytical experiments are underway to provide a deeper understanding of competitive dynamics between multicomponent adsorption, consumption and the connection with microstructural and morphological evolution.

DELIVERABLES: Present the first study that uses surface analytical probes to quantify the coverage of active surfactants for comparison with the predictions of the CEAC mechanisms derived from electroanalytical kinetic measurements (4Q 2005).

Theoretical and experimental work is also underway to probe the coupling of the CEAC mechanism with the traditional diffusion-adsorption-consumption model of leveling. The robust modeling of the competitive dynamics between catalytic brightener and poisoning leveling additive represent one of the current strategies employed by industry to circumvent the negative effects of bump formation (also called "momentum plating") that hampers conventional post-plating planarization technologies. A new code has been developed that details the effect of competition between a suppressor, catalyst, and leveler for surface sites and the subsequent effect on metal deposition and shape change. The code operates on the freeware Python platform, to ensure greater access, and to be more efficient and user friendly. The code has been downloaded by research groups around the world.

DELIVERABLES: Develop and make available advanced software for modeling superconformal filling of vias and trenches. The (3Q – 4Q 2005).

ACCOMPLISHMENTS

We have demonstrated void-free bottom-up filling of trenches with gold that may find use in

the formation of contacts and metallizations for compound semiconductors.

We have demonstrated the use of ruthenium barriers to obtain superconformal electrodeposition of copper metallizations without the need for a copper seed layer. Established metrics for effective seedless superfill.

Developed a protocol for quantifying the kinetics of catalyst consumption on the electrodeposit surface and the (detrimental) impact of such consumption on the superconformal feature filling process.

COLLABORATIONS

D. Wheeler, R.R. Keller, Y.-W. Cheng, J.E. Bonevich, D.R. Kelley, L.J. Richter, M.L. Walker, W.F. Egelhoff, J. Mallett, G.B. McFadden, S.R. Coriell, NIST.

International SeMaTech, Christian Witt; fabrication of patterned substrates with electrical test structures including sub-100 nm wire widths.

T. Aaltonen and M. Ritala, University of Helsinki; ALD deposition of Ru and Ir seed layers.

Clarkson University, Y. Li and C. Burkhard; chemical mechanical planarization of electrical structures.

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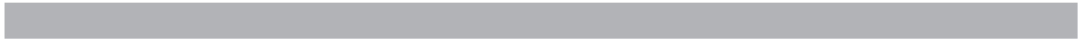
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NANOPOROUS THIN-FILM METROLOGY FOR LOW- κ DIELECTRIC MATERIALS

GOALS

In this project, we are developing measurement methods of the structure and properties of nanoporous thin films for low- κ dielectric applications. We work closely with industrial collaborators to develop and apply these methods to advanced materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include X-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, providing high quality data and measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

CUSTOMER NEEDS

As integrated circuit (IC) feature sizes continue to shrink, new low- κ interlevel dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low- κ dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant as discussed in 2004 ITRS, Interconnect, pages 1 and 2. However, the pore structure of these low- κ dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to optimize and to develop future low- κ materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to understand correlations between processing conditions and the resulting physical properties.

TECHNICAL STRATEGY

■ The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A unique suite of measurement techniques, Fig. 1, has been developed at NIST using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μm thick deposited on a 1 mm thick substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for X-rays and neutrons.

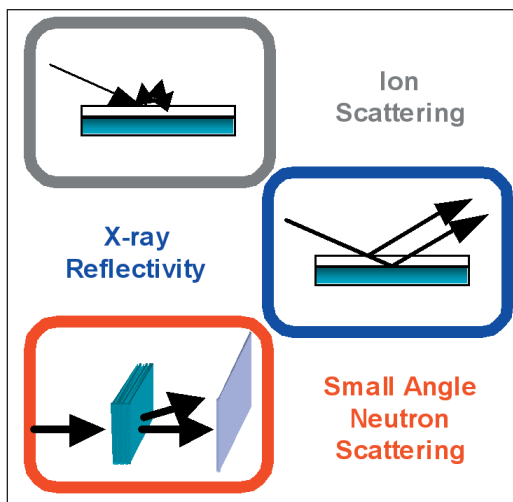


Figure 1. Three thin film measurements that are combined for complete characterization.

The XR experiments are performed at grazing incident angles on a modified to θ -2 θ X-ray diffractometer at the specular condition. With the modified configuration, reflectivity fringes

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"The SANS/SXR measurements have become a key metric in our low- κ dielectric materials characterization and screening process"

Jeffrey Wetzel –
International SEMATECH

"The NIST X-ray reflectivity program is useful, perhaps even critical, to the industry"

Abner Bello –
Applied Materials

can be observed from films up to 1.2 μm thick. High-resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed at the NIST Center for Neutron Research (NCNR). Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements are initially performed under ambient conditions to determine the structural characteristics of the pore structure. The scattering data are initially analyzed using a simple random two-phase description of the film, the Debye model. This model is appropriate for a class of films having random pores that makes up a majority of the samples measured. Other models are applied where appropriate such as a polydisperse collection of non-overlapping spherical pores. An additional method has been developed in which the Debye model is extended to include more complex distributions of pore sizes that need not be spherical in shape.

DELIVERABLES: Measure and report on up to 20 films for pore volume, pore size, and matrix density associated with ISMT. 3Q 2005

■ Further developments in the determination of pore size distributions have focused on the adaptation of conventional probe molecule porosimetry methods to the NIST experimental techniques. For example, XR was done on films that have been measured in vacuum in a conventional way, and then exposed to saturated toluene vapor for several hours (Fig. 2). Capillary action fills the pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average mass density that is a combination of the walls and the solvent-filled pores. By comparing the results of the sample in air or vacuum with the toluene results, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angles provide a measurement of the total film thickness before and after exposure to toluene and give a measure of

the solvent resistance of the material and rigidity of the walls.

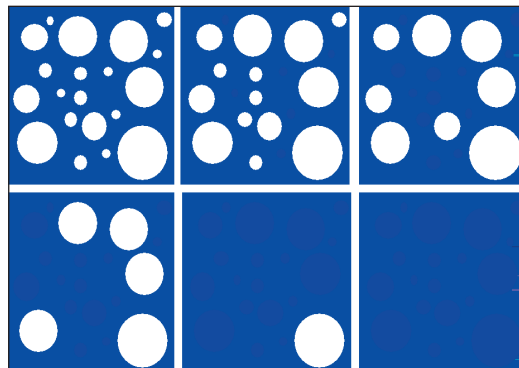


Figure 2. Schematic of the porosimetry measurement, increased solvent vapor pressure fills increased pore sizes.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.

DELIVERABLES: Publish Recommended Practice Guide for X-ray Reflectivity: X-ray Porosimetry for distribution to interested parties. 4Q 2004

■ The use of deuterated and hydrogenated probe molecules enables the powerful use of contrast match methods with the SANS technique. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene- h_8 and toluene- d_8 . If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosimetry can be determined.

We have developed a combination of contrast match SANS and XR porosimetry. A match solvent mixture at controlled vapor pressures deposits the contrast match liquid in the pores through capillary action. SANS would provide an additional measure of PSD.

DELIVERABLES: Develop measurement methods for SANS contrast match porosimetry technique. 1Q 2005

ACCOMPLISHMENTS

■ We continue to work with SEMATECH (SMT) on a project in which 20 thin films have been characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or X-ray porosimetry.

■ A NIST special publication was released that provides details of recommended practice guidelines for the use of X-ray porosimetry for the characterization of nanoporous thin films. X-ray porosimetry measurements were developed utilizing the controlled infusion of toluene into the open pores of a film through mass flow controllers and computer control. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES. Further, pore size distributions may be extracted using conventional thermodynamic equations from obtained absorption/desorption curves.

■ A contrast match method using saturated solvent vapor was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method.

The contrast SANS method was further advanced by performing SANS porosimetry measurements to determine pore size distributions that may be compared with the X-ray porosimetry data.

■ The structural evolution of pore formation in low- κ dielectric thin films (with a deuterated porogen) at various stages in processing was investigated using a combination of specular X-ray reflectivity (SXR) and small angle neutron scattering (SANS). SXR provides information as to the porosity and the density of the wall. SANS data show that the neutron scattering decreases during processing as the deuterated porogen degrades and pores are formed. The pore size and pore size distribution were estimated by fitting the SANS data to a structural model that describes the scattering intensity from a population of polydisperse spheres that includes hard sphere interactions between the particles and uses a Schultz distribution to describe the polydispersity. The porosity was found to decrease, while the pore size increased, during processing. A practical method of transforming phase size distributions into density correlation functions has been demonstrated. The computations are rapid and can produce density correlation functions, and hence scattered intensities to any necessary degree of accuracy. Phase size distributions other than the exponential ones described by Debye *et al.* can be transformed into density correlation. The transformation of scattered intensity into model phase size distributions is possible by this method.

■ Initial feasibility studies have demonstrated the potential of Small Angle X-ray Scattering (SAXS) to detect and to estimate the extent of sidewall damage of nanoporous low- κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low- κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in κ , it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low- κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low- κ material, then backfilled the trenches with the same candidate low- κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

DELIVERABLES: Determine feasibility of SAXS measurement methods for sidewall damage characterization in plasma etched patterned low- κ dielectric materials. 4Q 2005.

COLLABORATIONS

Polymers Division, NIST – Hae-Jeong Lee, Bryan D. Vogt, Christopher L. Soles, Hyunwook Ro, Da-Wei Liu, Ronald L. Jones, Center for Neutron Research, NIST – John Barker, Charles J. Glinka, Derek L. Ho

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Seoul National University – Kookheon Char, Do Yoon

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University of Michigan - David Gidley

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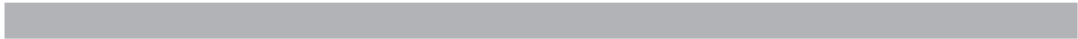
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INTERCONNECT MATERIALS AND RELIABILITY METROLOGY

This is a large project that involves parts that are not reasonably combined in a single document. For this reason, the project is presented in two sub-sections, each focusing on a single aspect. These are:

- Basic Materials Properties
- Interconnect Test Structures



BASIC MATERIALS PROPERTIES

GOALS

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin interconnect conducting and insulating films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; and (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

CUSTOMER NEEDS

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 10 thin-film layers now, and will soon reach 12 layers (*International Technology Roadmap for Semiconductors, 2004, Interconnect, Table 81a*). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low- κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2003, unchanged for 2004), Interconnect, p. 34, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. The 2003 NEMI (National Electronics Manufacturing Initiative) Research Priorities document reports a similar need. In a section beginning on page 24, entitled Modeling, Simulation and Design Tools, Emerging Areas for Electronics Packaging, Table 3, Projected Development and Research Needs for Simulations in Emerging Areas, in-*

cludes nanoscale modeling and simulation as an area, experimental tools capable of measuring electrical, thermal, and mechanics phenomena/material properties at smaller scale as a need, and "Issue: how is the property and behavior different from bulk behavior/macro-scale?" as a comment. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition or spin-on deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology. We held a workshop entitled Reliability

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Issues in Nanomaterials, 17–19 August 2004, to gauge customer interest in the available tools for characterization of nanomaterials, which, of course, encompasses advanced interconnect structures at both current and foreseen size scales. Microelectronics manufacturers were represented, along with universities, national laboratories, and more general commercial interests.

DELIVERABLE: Report, 2Q 2005, on workshop: Reliability Issues in Nanomaterials, held August 17–19, 2004.

The report to be published in 2005 gives the details, but two key messages for this research project were the widespread adoption of nanoindentation for material characterization, and the serious consideration given to atomic-scale materials engineering.

TECHNICAL STRATEGY

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Oc-

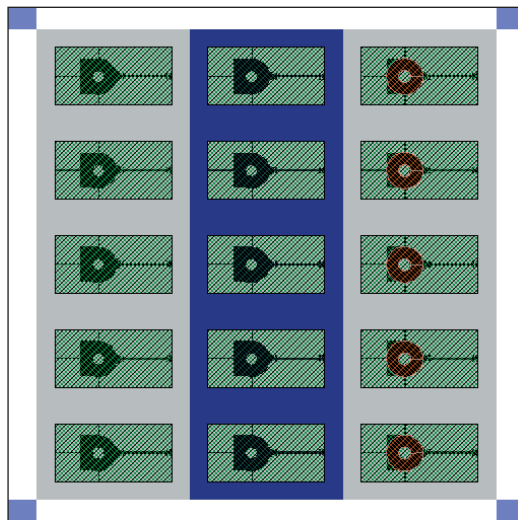


Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

casionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry.

DELIVERABLE: Microtensile test results on a new variety of electrodeposited copper will be reported to an industry collaborator, 2Q 2005

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. thermomechanical fatigue measurements, and resonant structure measurements. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm , a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material. The use of advanced analytical techniques including electron back scattering diffraction (EBSD) and transmission and scanning electron microscopy (SEM and TEM) has revealed surprisingly similar microstructural damage and failure mechanisms in a.c.-stress and microtensile tests. This indicates at least the possibility that electrical tests may be exploited to produce information about the mechanical

characteristics of thin films. If this electrical-mechanical test can be made to produce relevant data, it will be of significant benefit because of the experimental convenience of electrical stressing on specimens of a wide range of sizes, including very small.

We have work in progress, with the NIST Metallurgy Division, to address reliability of advanced interconnect materials with linewidth less than 100 nm. In addition to the challenges associated with electrodeposition into extremely narrow trenches, we expect significant influences of the interconnect sidewalls on electrical resistivity and possibly on thermomechanical fatigue resistance.

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

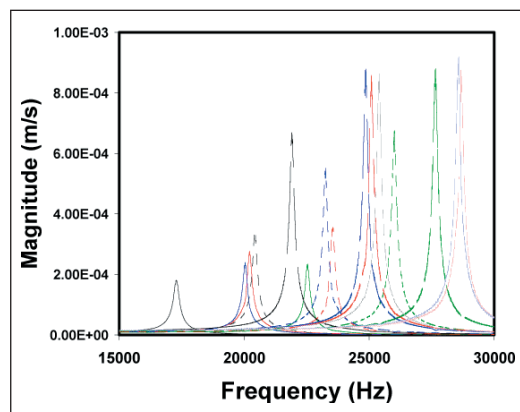


Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams and measurements of residual strain

and strain gradient can be made. With the residual strains, from the fixed-fixed beam method, the elastic constant, from the resonant method, and the strain gradient, from the curvature of cantilevers, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

ACCOMPLISHMENTS

Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement techniques and an understanding of the results. Currently we are placing major focus on the comparison of stress-to-failure a.c. electrical tests vs. microtensile tests. Figure 3 shows the effect of line width on current density at failure in ramp-to-failure tests.

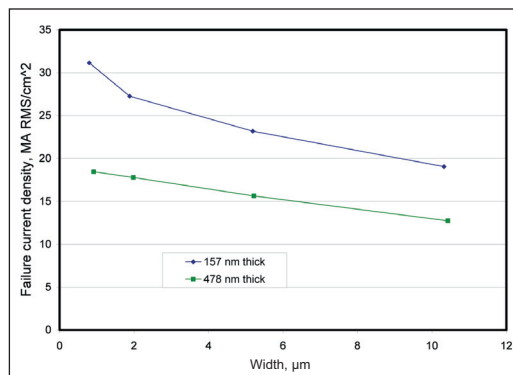


Figure 3. Effect of line width on current density at failure in ramp-to-failure tests in PVD copper films.

Such scale-related effects will have to be factored into analysis procedures for deducing material properties from a.c. tests. We are also running an interlaboratory round robin on the use of nanoindentation to measure hardness and modulus in a copper film on a silicon wafer. Specimens have been fabricated, characterized, and distributed to over 20 laboratories.

DELIVERABLES: Four technical presentations on the comparison of electrical and mechanical stress effects have been presented at technical conferences, 2Q 2004 to 2Q 2005, and three were submitted for publication in the respective technical conference proceedings. Three journal papers appeared in the past year. See Recent Publications, below.

A key experimental tool for understanding the sources of mechanical weakness is fractography of broken specimens. A new scanning electron microscope, with a field-emission source and an in-lens detector, is allowing us to obtain very clear images of the fractures surfaces of microtensile specimens. This aluminum CMOS contact metal had low elongation, and variable tensile strength with some very low values. We have made progress in mounting tested tensile specimens on silicon-nitride membranes for observation in the TEM. An image of a failed specimen is shown in Fig. 4.

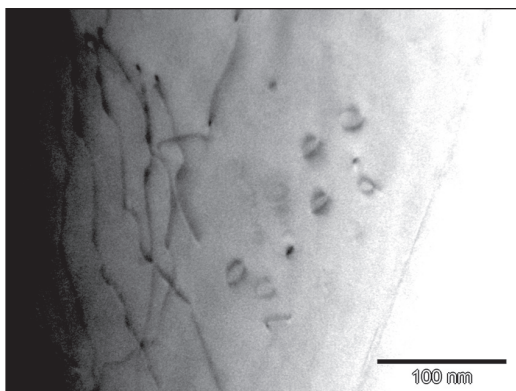


Figure 4. TEM image of failed edge of a MOSIS thin film aluminum tensile specimen, showing prismatic dislocation loops, but no mobile dislocations, in the region near the edge.

Recently, we have been working to demonstrate the applicability of these techniques to materials recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5. We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 μm to 10 μm , increases the ductility from around 1 % or less to 5 % or more. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 $^{\circ}\text{C}$. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

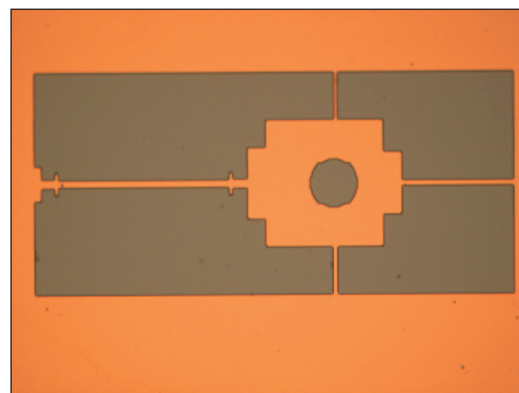


Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

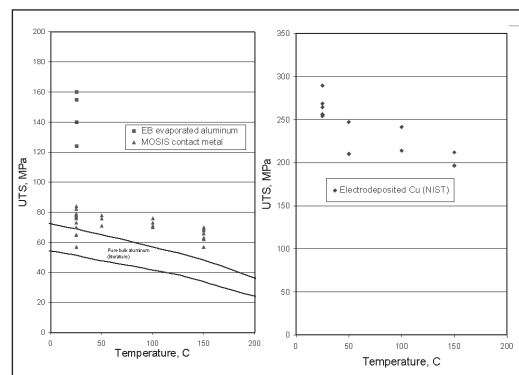


Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic model that simulates the mechanical behavior of this morphology, though at a smaller scale. The at-

oms shows as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for our measured values of the elastic constant of ED copper, which are lower than the bulk value. We have extended our atomistic modeling to the mechanical behavior of quantum dot structures such as germanium in silicon and indium arsenide in gallium arsenide, specifically, the strain in and around the heterogeneous inclusion. Strains surrounding the quantum dot structures play an important role in creating the confined electron states and in providing a driving force for self-assembly of arrays of dots.

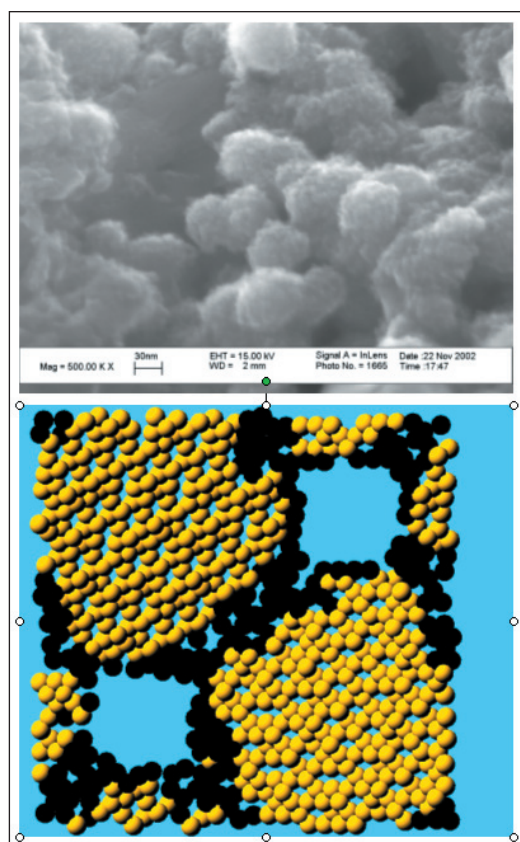


Figure 7. a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper “balls” are 30–50 nm in diameter. b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal face-centered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000-atom model simulates a specimen of indefinite size.

Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. Figure 8 shows the large difference in lifetime seen under the AC and DC test conditions. We have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 9, pg. 108). Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

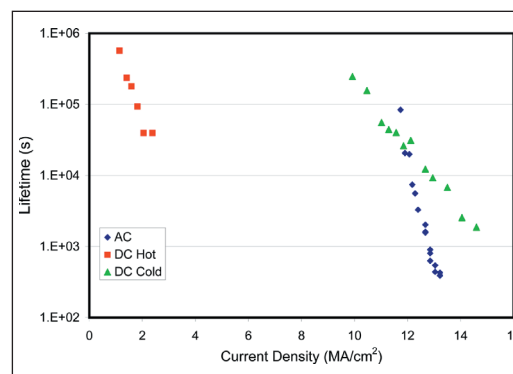


Figure 8. Time to open circuit under various electrical testing conditions. “AC” and “DC Cold” data obtained with specimen nominally at room temperature. “DC Hot” tested at nominal specimen temperature of 227 °C. “DC Hot” data from U. E. Möckl, M. Bauer, O. Kraft, J. E. Sanchez, Jr., and E. Artz, MRS Symp. Proc. Vol. 338, 373 (1994).

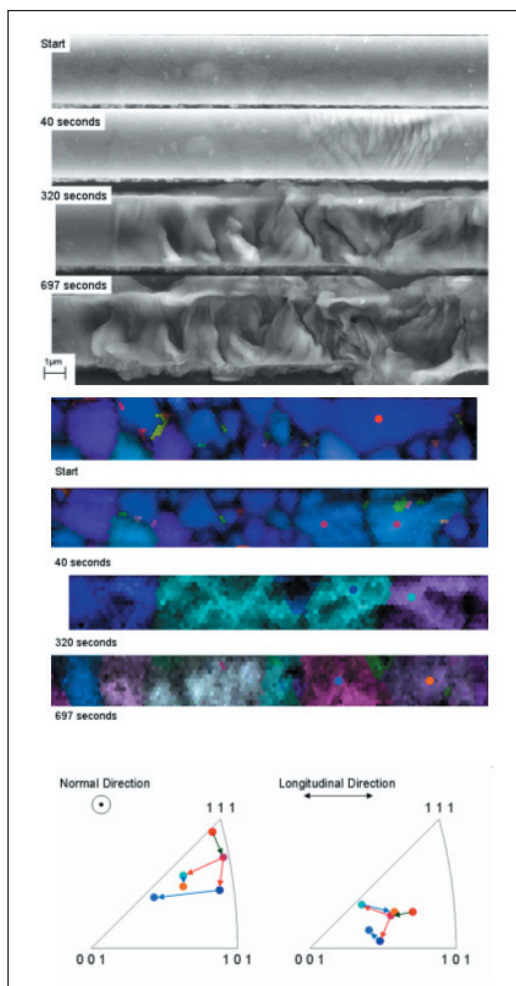


Figure 9. AC testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of AC cycling at about 12 MA/cm². Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole.

The Matlab optimization procedure to extract the Young's modulus values of the various interconnect and oxide layers has been automated. This procedure includes the calculation of the thicknesses of the various layers given inputs such as capacitances, sheet resistances, resistivities, and step height measurements.

Also, a sensitivity analysis has been semi-automated where each of the Matlab inputs gets varied $\pm 10\%$ or ± 3 standard deviations. The resulting Young's modulus values are then recorded. The important conclusion is that even if the various inputs are off by $\pm 10\%$, reasonable Young's modulus values can still be obtained. The optimization technique is not as sensitive to layer thicknesses as originally believed. The technique is proving to be solid and reliable.

The latest test chip design (see Fig. 10) includes cantilevers ranging in length from 100 μm to 400 μm . A procedure was developed using the optical vibrometer to obtain the resonant frequencies of the shorter length cantilevers. Plots of Young's modulus versus length for each layer exhibit phenomenal results. *The optimized Young's modulus results are stable as a function of length and within the realm of acceptability!* Figure 10 shows these plots for metal1 and metal2. The data points given at $L=500\text{ }\mu\text{m}$ represent the averages from two previous chip submissions. The error bars on the data points represent a plus or minus one sigma variation. The minimum and maximum bounds represent values given in the literature. The line represented by 'Eguess' is the initial value used in the optimization. An ini-



Figure 10. Test chip design fabricated on the AMI 1.5 μm CMOS process.

tial result from the tensile tests found an average metal1 and metal2 Young's modulus value of 63 GPa, which falls nicely between the metal1 and metal2 lines in Fig. 11. Journal articles are being prepared on both the Young's modulus results and the thickness results.

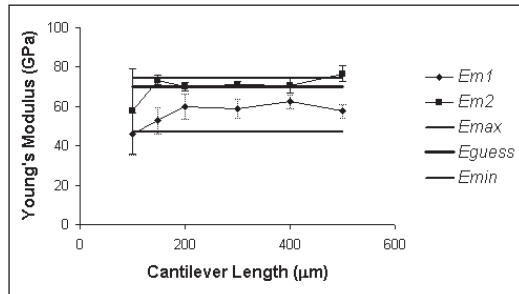


Figure 11. Young's modulus plotted versus cantilever length for metal1 and metal2.

COLLABORATIONS

University of Karlsruhe, Germany, Prof. Eduard Arzt, Dr. Cynthia Volkert

Intel Corp., Hillsboro, OR, Dr. Brad Sun

Motorola, Inc., AISL, Tempe, AZ, Betty Yeung, and MATC, Schaumburg, IL, Dr. Andrew Skipor

MOSIS Integrated Circuit Fabrication Service, 4676 Admiralty Way, Marina del Rey, CA, Dr. Tom Veriner.

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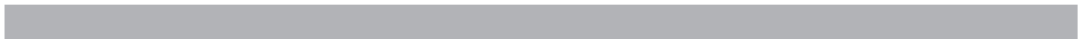
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INTERCONNECT TEST STRUCTURES

GOALS

The overall goal is to make essential contributions to a test-structure infrastructure that is responsive to state-of-the-art interconnect-system fabrication needs. Test-structure metrology applications can be classified into two groups: 1) selection of materials for developing fabrication processes for new interconnect systems that comply with always-increasing device density needs and maintaining those processes in wafer production 2) parameter extraction for modeling and predicting the performance of interconnect systems for particular fabrication implementations. The project's test structures for process development will allow the extraction, by electrical means, of key dimensional parameters such as etched-feature CD. This is a key unsolved problem when copper conductors are embedded in barrier metals. In this case, an as-yet unresolved issue is the adverse interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features. A near-term goal in related materials studies is the fabrication of electrically testable, all copper, features having lateral dimensions in the 20- to 100-nm range. This project's unique approach assesses the impact of feature-dimension scaling on the fundamental physics of electron transport in features built from single metal species, such as copper, without the metrology complications resulting from having other metal species incorporated into interconnect features. The information so provided is to enable modeling the performance of features that are replicated with two or more metals and is designed to aid in the verification of dimensional parameter extraction for process-control purposes. Another class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. Among the test structures that will be implemented for modeling the performance of particular fabrication implementations will be strip lines that will be rf-tested from DC to 10 GHz, consistent with clock speeds of road-map integrated circuits over the next several years.

A related facet of this work is the measurement of the sheet resistance of planar films of preferred interconnect metals, such as copper, having thicknesses in the 20-to-100 nm range. The purpose is to relate electrical performance to material properties such grain-size distribution and the films' thicknesses. It is anticipated that this ap-

proach will make major contributions to the correct interpretation of the electrical measurements of the narrow features described above.

CUSTOMER NEEDS

Interconnect is becoming the principal factor that determines the maximum performance that can be attained with emerging generations of gigascale chips. This means that future advances in IC performance will be governed increasingly by the advances in interconnect technology, rather than by advances in active devices. In particular, at technology nodes of 0.13 μm and below, the attainable rate of signal propagation through the IC chip is dominated by the interconnect implementation. As aluminum is replaced by hybrid copper/barrier-metal conductors, the initial benefits of the higher conductivity, which are real at the 130-nm node, are becoming problematic at the 90-nm node and below, as a result of the predominance of contributions of the barrier metal to the conductor resistance. Whereas there is no simple global solution to the challenge at this time, it is certain that advances in metrology science applied to process and materials management, such as those being pursued by this project, will play a central role in assuring maximum performance from copper-based interconnection systems until such time that innovations, such as optical interconnects, are introduced. Meanwhile, a manufacturing challenge that is as attributable scaling *per se* rather than the materials selected for interconnect implementation is overlay. Overlay metrology is being challenged by exacerbation of the tool- and wafer-induced shifts that are generally manageable for technology generations introduced prior to the 130-nm node.

TECHNICAL STRATEGY

The four-part current technical strategy is to build on opportunities afforded by the project's unique SCCDRM experience. The same substrates that have been developed for CD reference-material applications are being applied to the fabrication of single-metal, initially copper-only, test structures with features having lateral dimensions in the 20- to 100-nm range. The process-flow is illustrated in Fig 1 (pg. 112). The approach shown there will provide a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the resistance

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M. W. Cresswell

metrology complications resulting from having other metal species serve as barrier layers. The information so provided will enable modeling the performance of features that are replicated with copper-cored binary-metal technology and will aid in the verification of dimensional parameter extraction for process-control purposes.

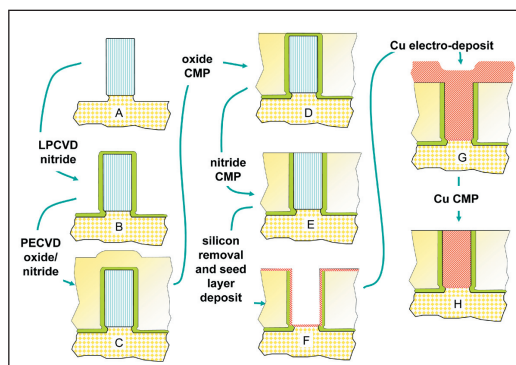


Figure 1. Scheme for fabrication of single-metal, test structures with features having lateral dimensions in the 20-to-100 nm range.

The project's test structure is one that will allow the extraction, by electrical means, of key dimensional parameters for process-control purposes such as copper-cored interconnect feature CD. This responds to an unsolved problem when copper conductors are embedded in barrier metals. The solution is sought after by companies marketing interconnect-system modeling software tools and their industry clients. Our strategy is based on a test structure we first proposed four years ago but have not yet been implemented.

To validate CD and interconnect feature resistance extraction from test structures, we are initiating a study of the interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features. There is an absence in the scientific literature of any report of analyses of this central issue.

Another class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. This project has successfully filed for a patent on an electrically calibrated test structure to serve as a process- and tool-specific overlay standard that avoids all the limitations of other approaches.

Among the test structures that are being designed for modeling-parameter extraction are strip lines that will be rf-tested from DC to 10 GHz, consistent with clock speeds of road-map integrated

circuits over the next several years. The strategy is the computation of rf-impedance properties that are employed in interconnect-system modeling from S-parameter measurements. An important spin-off from this activity is the application of similar rf-measurement techniques to traceably validating key dimensional parameters of masks which are patterned for interconnect fabrication, another application which has been long sought by the mask-vendor and mask-user industries. This work will be done initially on binary masks but, if successful, will be extended to the examination of opportunities in dimensional metrology for more complex binary-mask applications.

A related facet of this work is the measurement of the sheet resistance of planar films of preferred interconnect metals, such as copper, having thicknesses in the 20- to 100-nm range. The purpose is to relate electrical performance to material properties such grain-size distribution and the films' thicknesses. It is anticipated that this approach will make major contributions to the correct interpretation of the electrical measurements of the narrow features described above.

DELIVERABLES: Complete an analysis of the effects of surface and grain-boundary scattering that characterize dc conduction through planar films. 3Q 2005

DELIVERABLES: Design, and verify by simulation, the performance of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication. 3Q 2005

DELIVERABLES: Design, fabricate with SCCDRM technology, and make initial ECD measurements on a test chip having chemically stable copper-only features. 4Q 2005

DELIVERABLES: Design, fabricate, and make initial ECD measurements a second-generation SCCDRM test chip having chemically stable copper-only features and perform silicon-feature silicidation process. 4Q 2005

DELIVERABLES: Design an interconnect test chip for extracting s-parameters and rf-impedance components over frequency ranges up to 20GHz. 1Q 2006

DELIVERABLES: Fabricate, test, and calibrate a selection of overlay test chips designed for high-density interconnect applications. 2Q 2006

DELIVERABLES: Fabricate a strip-line interconnect test chip for s-parameter extraction, and measure rf-impedance components over frequency ranges up to 20GHz interconnect-modeling applications. 3Q 2006

ACCOMPLISHMENTS

Since this project has only been at full strength for several months, the major accomplishments are largely of a preparatory and logistical nature. However, several important ones have been attained.

- *The first draft of a paper on effects of surface and grain-boundary scattering that characterize dc conduction through thin planar films has been completed.* The thrust of this work is to provide essential input for modeling conductor resistance as influenced by electron scattering by the conductor's surfaces and grain boundaries, and the effects of barrier layers on copper line resistance.

- **Standards Leadership:** Project member served on JEDEC Committee JC14.2 to update one existing JEDEC standard and complete a new JEDEC standard.

Both of these standards deal with interconnect reliability. The existing standard, JEP139, is for characterizing the resistance of interconnects to stress voiding damage and previously only applied to aluminum interconnect. JEP139 is being modified to include applicability to copper interconnects and has completed two rounds of balloting. The new standard will also deal with copper interconnects, and is a test standard for electromigration and is in the process of undergoing first ballot.

- *The CAD of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication has been completed.* A program to simulate and validate the calibration of the standard is nearing completion.

- *The fabrication with SCCDRM technology of the first test structures having chemically stable, copper-only, features has completed copper seed-layer deposition and the first wafers are being electro-plated.* The approach shown there will provide a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the resistance metrology complications resulting from having other metal species serve as barrier layers.

- *The CAD of a second-generation SCCDRM test chip for the fabrication chemically stable copper-only features has entered planning stages.*

The principal goal is to reduce the CDs we are presently fabricating with i-line lithography to the 20- to 40-nm level with the use of Imprint and direct-write e-beam lithography. These are the features that will eventually be used for silicidation experiments. The collaborating partner has already been supplied project test chips having silicon features with 50-nm CDs for familiarity and preliminary process tests.

- *The project competed for, and was awarded, an intra-mural program to conduct further research into SCCDRM fabrication and calibration.* This program is providing major infra-structure benefits in the meeting the deliverable item schedule above/.

COLLABORATIONS

The leading collaborators are three Universities.

The Scottish Microelectronics Centre at the University of Edinburgh (SMC) is now providing almost all wafer the project's wafer fabrication operations. More importantly, the staff there are highly and broadly experienced in interconnect fabrication materials, processes, and issues. Audio teleconferences are exchanged between Project and SMC staff at least once a week. Its wafer-fabrication facility is very well equipped to meet many of the project's needs and will continue doing so for the foreseeable future with government funding. Its receiving the latter was an early product of our collaboration.

The Electrical-Engineering and Computer-Sciences Department at George Washington University has been funding the studies of Ph.D students, and a Professor, to work on this NIST Project for almost a decade. The present collaboration contributes special skills in rf parameter extraction and the physics of electron transport.

A new collaboration with the **Department at The University of Texas at Austin** is in the formative stages. UT-Austin's role will be to conduct experiments on the transformation of narrow SCCDRM features to silicide material and to contribute very desirable ultra-narrow-line lithography for the next-generation SCCDRM fabrication.

The project has collaborated over the past several years with personnel at **Cadence Systems, Inc.** The collaboration initially involved in refining ECD test-structure metrology to address the binary-metal conductor problem described earlier in this document. More recently, the collaboration attention has been shifted to parameter extraction

from rf test structures for modeling interconnect-system performance of 90-nm generation devices.

Important collaborations with **two different major semiconductor-industry players** are in the formative stages. The respective and separate topic fields are electrically-calibratable overlay standards and non-contact CD metrology for interconnect features. The two companies are not identified here because both sets of CRADA negotiations are in a sensitive stage.

This project has always benefited from very active collaboration with Litho-Metrology Operations at **SEMATECH**. Although the project's focus has only recently shifted away from litho-metrology to interconnect, we are actively pursuing a parallel shift in our collaboration.

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WIRE BONDING TO COPPER/LOW- κ SEMICONDUCTOR DEVICES

GOALS

The overall objective is to determine optimal conditions for achieving high yield reliable fine-pitch wire bonds to advanced technology semiconductor chips with copper/low- κ interconnect structures.

CUSTOMER NEEDS

The introduction of copper metallization interconnect structures in advanced integrated circuit manufacture has forced changes in wire bonding. The process should be invisible to the current wire bonding machines. However, bare-copper bond pads oxidize, requiring an oxygen-protective/bondable coating. The current solution of using a tantalum barrier, capped with aluminum, for bondability is unsatisfactory for fine pitch due to increased Au-Al intermetallic failures. Also, when low-modulus low-dielectric materials lie below the pad, a support structure is necessary to prevent damage to the interconnection/dielectric layers. There are many approaches to solving these various problems; the NIST program is attempting to optimize and develop new bond pad solutions where necessary (Fig. 1).

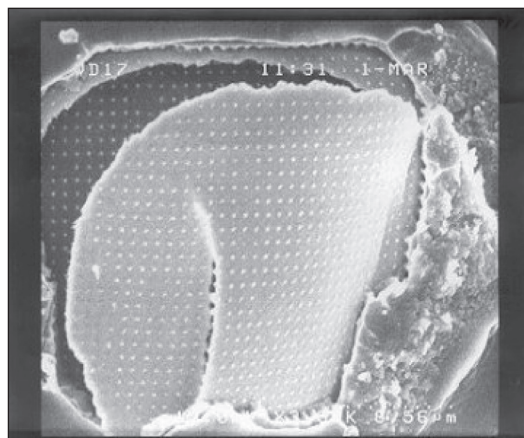


Figure 1. Pad peeling is a common problem with Low- κ under the bond pad.

TECHNICAL STRATEGY

1. The industry is generally using a tantalum barrier with an aluminum cap for wire bonding. Such an approach requires several expensive (deposition, mask, etch, clean) wafer preparation steps. It also suffers from serious intermetallic failure problems as the pad pitch is reduced be-

low 50 μm . A better approach to protecting the copper is to coat the bond pads with a bondable gold layer. This is more direct and eliminates the intermetallic problem in the process. For this approach, the first objective is to determine the diffusion coefficients of copper through gold, because copper can diffuse to the surface during thermal processes, and will oxidize, preventing good bond formation. Literature values on various gold platings are contradicting and have been performed on non-damascene structures, often with undefined plating conditions. A more classical approach, but also a more difficult process, using SIMS has been proposed. We have developed several gold deposition process over the damascene process copper metallization chips. Even without the actual diffusion coefficients, a pragmatic approach is being carried out by heating gold coated samples (with various grain refiners) and doing extensive wire bonding and evaluating with ball shear tests. A subset of this work will be to determine the minimum thickness of gold necessary to prevent copper diffusion/oxidation in normal bonding/processing temperatures. Several inorganic coatings for protection have been evaluated. Sandia has applied thin deposited SiO_2 coatings on copper wafers and they were evaluated. Results indicated that all coatings were nonuniform, but bonding did occur on the better pads. This evaluation is continuing, but preparing uniform coating that are thin enough to bond through has proven difficult (Fig. 2, pg. 116).

2. Another objective is to measure the nano-hardness and modulus of the damascene copper in order to optimize bonding, [hardness should be minimized (80 Knoop to 100 Knoop)]. This was successful, and results indicate that annealing in argon produce the softest most bondable copper surface for bonding.

Problems occurred when sawing the bare copper chips in which the saw particles stick to the bare copper. Several approaches to curing this problem were pursued and one has been adopted. (Wafers are sawed face down on tape within $\sim 10 \mu\text{m}$ of completion. They are snapped off upon removal from the tape, resulting in clean chips. Copper damascene process samples have been supplied by IBM and SEMATECH for this effort.

Technical Contacts:

G. G. Harman
C. Johnson

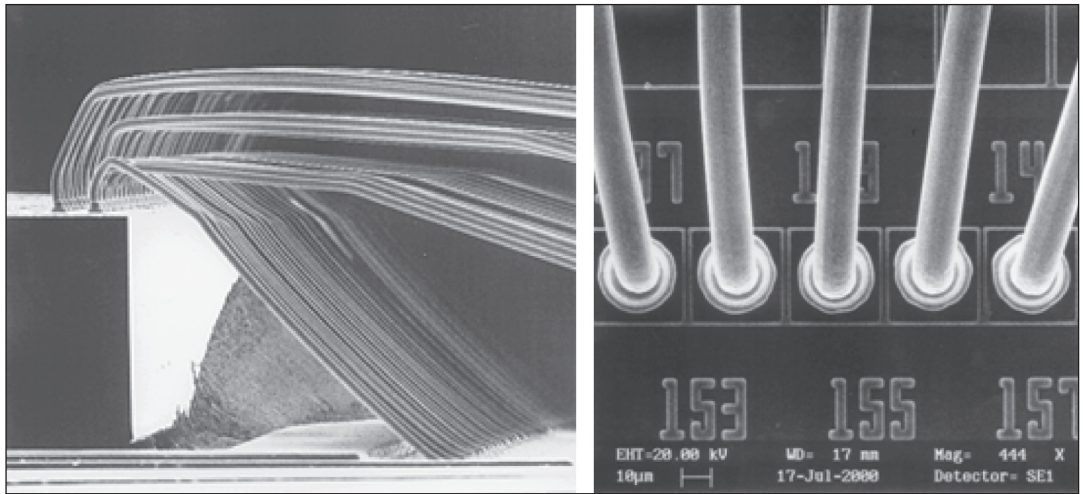


Figure 2. Area Array wire bonds at 35 μ pitch (ASM bonder)

DELIVERABLES: The desired thickness of gold deposition will be determined, as well as the most desirable grain refiners for the purposes. A nickel strike coating also was developed. Two different plating additives are being evaluated. Diffusion studies of copper into gold will be made after evaluating the surface morphology. The applicability to fine pitch bonding to the gold surfaces will be evaluated. 3Q 2005

satisfactory and bonded well. Currently, wafers from another source with thicker copper are being plated. Copper diffusion through the gold is being measured.

ACCOMPLISHMENTS

- Knoop hardness measurements have been accomplished with a series of annealing experiments made with copper chips, and pragmatically verified by actual bonding experiments. Values of measured nanohardness have been dependant on the annealing gas (argon is best) and have been as low as 60 GPa (about 120 GPa unannealed) and the modulus as low as 20 GPa. Problems have occurred in early diffusion studies and several different methods are being initiated.

- Papers published, entitled “Wire Bonding To Advanced Copper-Low- κ Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations,” by George G. Harman and Christian E. Johnson, Proc. 2001 IMAPS Symposium, Oct 9-11, 2001, Baltimore, MD, pp. 484-491. This paper won an award as an outstanding paper in the Symposium. An updated version, with new data, was published in the IEEE Transactions on Components and Packaging Technologies, V-25, Number 4, Dec. 2002, pp. 677-683. A talk sponsored by the IEEE CPMT society was given in San Jose in May 2003.

- The two step non-contact gold deposition process used on some of the original SEMATECH wafer copper etched the copper surface, whereas other gold deposition methods were

SOLDERS AND SOLDERABILITY MEASUREMENTS FOR MICROELECTRONICS

GOALS

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free (Pb-free) solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

CUSTOMER NEEDS

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pb-free solders has been specified in the 2002 iNEMI, 2003 IPC, and 2003 ITRS Roadmaps. The European Community (EC) directives on Waste Electrical and Electronic Equipment (WEEE) and the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) take effect in mid 2006. U.S. manufacturers must comply with these requirements in order to compete in the global market. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the International Electronics Manufacturing Initiative (iNEMI) working group on Pb-free solder alloys. It was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on copper (Cu) leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure tin (Sn) tend to grow "whiskers," however, which can cause shorts across leads. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important, and tests which ascertain the tendency to form whiskers are much needed. NIST co-chairs the iNEMI Sn Whisker Modeling Group and is an active participant in the iNEMI Accelerated Sn Whisker Test Group.

TECHNICAL STRATEGY

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. For example, a thermodynamic database has been developed and publicly distributed for modeling the processing behavior of lead-free solder systems. These databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will continue to be expanded and distributed via the web. We also provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations. In addition, a much-needed guide to interpretation of thermal analysis data will be produced.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (filamentary whiskers typically 1 μm diameter and several mm long) can grow from the plating and cause electrical shorts and failure. Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus on Pb-free Sn-rich deposits with alloying additions that might retard whisker formation. The Sn-Cu system was selected for compatibility reasons, since Sn-Cu-Ag is likely to be the Pb-free solder of choice for industrial application. The substitution of a different solute for Pb in the Sn-rich deposit was proposed to also retard whisker growth. A detailed microstructural comparison of deposits with high and low whiskering tendency has been conducted. Sn grain size, shape, and residual stress have been measured and correlated to whisker growth (Fig. 1, pg. 118).

DELIVERABLES: Add pages for constituent binary and ternary phase diagrams containing Antimony to the Metallurgy Division Web book. 4Q 2005

DELIVERABLES: Make the easy-to-use lever rule equilibrium and Scheil solidification interface for solder solidification available on the web; make more complex thermodynamic programs available for download. 4Q 2005

DELIVERABLES: Finish Best Practice Guide for Differential Thermal Analysis. 4Q 2005

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William Boettinger
Ursula Kattner
Kil-Won Moon
Maureen Williams

"I consider your [NIST Metallurgy Division] group a key asset to industry in making these decisions on the soundest possible scientific basis. There is no comparable body of expertise anywhere in the world that matches that found in your group."

Dr. George T. Galyon (IBM)
-Chairman, NEMI Tin Whisker Modeling Committee

DELIVERABLES: Electrodeposit Sn and Sn-Cu on W and Zn substrates to determine whisker tendency. Sn does not form intermetallic with these substrates. 4Q 2005

ACCOMPLISHMENTS

- 1) An easy-to-use lever rule equilibrium and Scheil solidification GUI interface has been prepared for solder solidification calculations. The code allows the user to select the default NIST thermodynamic data base or a user defined data base. The user selects a composition in either weight or atomic percent and chooses an equilibrium or Scheil calculation. Results are presented in either graphical or tabular form showing the starting temperature of solidification and the final freezing temperature as well as the phase that occur as eutectic microconstituents.
- 2) NIST remains a co-chair in the iNEMI Sn Whisker Modeling Group (working closely with members ChipPAC, Cookson, Delphi Delco, FCI Framatome, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas

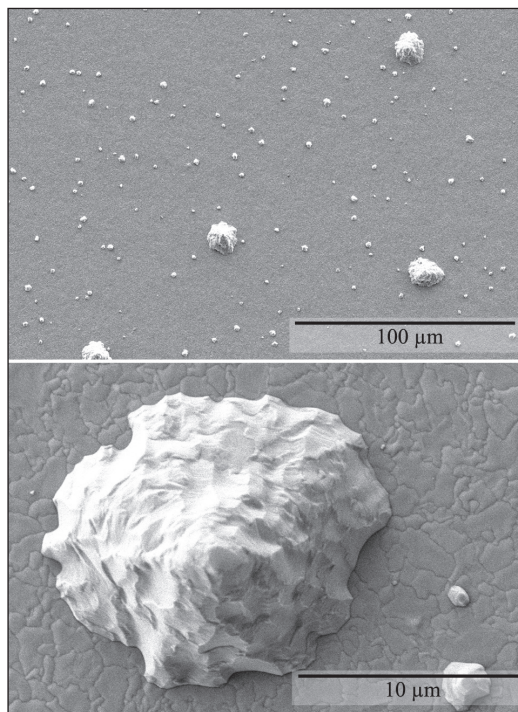


Figure 1. Low and high magnification SEM micrographs of the electrodeposit surface of a 16 μm thick pure Sn electrodeposit on a cantilever beam showing bimodal size distribution of conical hillocks. Such hillocks form to relieve compressive residual stress. Whiskers form when grain boundaries in the deposit are pinned by precipitates.

Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics) and is an active participant in the iNEMI Accelerated Sn Whisker Test Group.

- 3) JEDEC Solid State Technology Association (formerly known as the Joint Electron Device Engineering Council), excepted and published the iNEMI test protocol “Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes” as JEDEC Standard JESD22A121 in May 2005. NIST researchers provided input for this protocol.
- 4) A major accomplishment of this year is the submission of a manuscript to *Acta Materialia* entitled, “Hillock and Whisker Formation in Sn, Sn-Cu and Sn-Pb Electrodeposits.” The paper presents measurements of compressive stress in the electrodeposits and how the different microstructure of the deposits effect whisker growth. Relief of the compressive stress occurs by uniform creep for Sn-Pb because it has an equiaxed grain structure. Localized creep in the form of hillocks and whiskers occurs for Sn and Sn-Cu because both have columnar structures. Compact hillocks form for the Sn deposits because the columnar grain boundaries are mobile. Contorted hillocks and whiskers form for the Sn-Cu deposits because the columnar grain boundary motion is pinned by intermetallic precipitates.
- 5) Some reports suggest that restraining and cracking of the Sn oxide surface film are necessary steps in the nucleation of Sn whiskers. However, results at NIST, accepted for publication in the *Journal of Electronic Materials*, showed little support for this mechanism. For instance, we observed whiskers only on bright Sn-Cu electrodeposits but not on pure bright Sn electrodeposits on pyrophosphate Cu substrates. Thus, in order to understand the role of the deposit surface, the Sn oxide surface film and surface structures were analyzed by Auger and EBSD. Especially, in Auger analysis, residuals of the Sn oxide surface film were observed after Ar^+ ion cleaning. This feature allowed us to discriminate the Sn whisker growth with or without the oxide surface film. In EBSD analysis, grain and eruption orientations of the Sn deposit were characterized, and the results were discussed in metallurgical terms in order to correspond to the Sn whisker growth.

COLLABORATIONS

International Electronics Manufacturing Initiative; Lead-free Solders and Reliability. Co-Chair of the Sn Whisker Modeling Group and a member of the Accelerated Sn Whisker Test Group.

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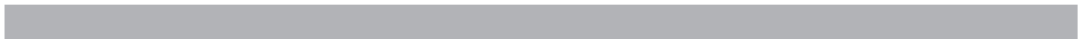
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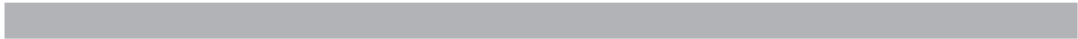
PROCESS METROLOGY PROGRAM

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.



GAS PROPERTY DATA AND FLOW STANDARDS FOR IMPROVED GAS DELIVERY SYSTEMS

GOALS

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition and the calibration of mass flow controllers (MFCs). As the data are acquired, they will be posted to an online database.

NIST also will develop primary standards for gas flow in the range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry (10^{-6} mol/s \approx 1.3 standard cubic centimeters per minute (sccm)).

CUSTOMER NEEDS

The 2003 *International Technology Roadmap for Semiconductors* (ITRS) emphasizes that the grand challenge for front-end processes is “material limited device scaling.” The Modeling and Simulations section reinforces this theme: “Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases ... are needed.” Meeting this challenge will require improvements in MFCs for the deposition and etching of diverse new materials. Thermal MFCs meter a wide variety of toxic, flammable, and corrosive gases over a large range of flow rates. Elements necessary for improved MFCs will be accurate models of gas properties and reliable physical standards for gas flow.

Participants at an industry workshop at NIST identified the gases and properties of highest priority, and they recommended publishing the property values in a public, Web-based database. The gases include process gases, “surrogate” calibration gases, and binary mixtures of process and carrier gases. The identified properties and required uncertainties include the following.

- heat capacity at constant pressure $\pm 0.1\%$
- equation of state (gas density) $\pm 0.1\%$
- viscosity $\pm 0.5\%$
- thermal conductivity $\pm 0.5\%$

The workshop also required the following uncertainties for physical standards for gas flow.

- primary standards for gas flow $\pm 0.025\%$
- transfer standards for gas flow $\pm 0.1\%$

TECHNICAL STRATEGY

We are measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have relative standard uncertainties of 0.01 %. Measurement conditions range as high as 425 K and 1500 kPa (or to 80 % of the vapor pressure for condensable gases). Figure 1 shows an example of such data. The speed-of-sound data are used to determine the ideal-gas heat-capacity $C_p^0(T)$ with the targeted uncertainty of 0.1 %. The pressure and temperature-dependences of $u(T, p)$ are correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the virial equation of state for the density $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than 0.1 % for density, 10 % for viscosity, and 10 % for thermal conductivity from 200 K to 1000 K.

Technical Contacts:

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Michael R. Moldover

“I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry. It was virtually exactly what I was searching for.”

Bob Rathfelder,
Project Engineer,
Parker Hannifin

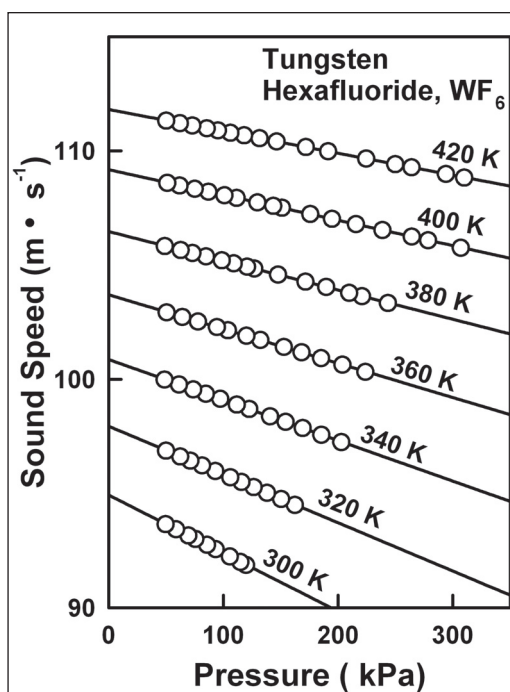


Figure 1. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

We also are developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 % as specified by the industry workshop. Figure 2 shows a second-generation acoustic viscometer made from Monel. Throughout the project, the results will be made available to industry through publications in professional journals, presentations at professional meetings, and entries in an on-line database at <http://properties.nist.gov/semiprop> (see Fig. 3).

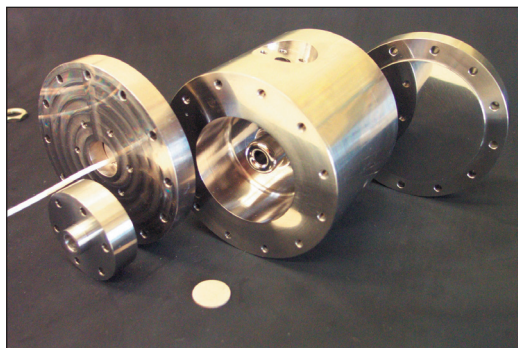


Figure 2. Second-generation acoustic viscometer made from Monel for use with corrosive gases.

Tungsten Hexafluoride

WF₆

M.W. [1]

N.B.P. [2]

T.P. [2]

297.84

290.25 K

275.0 K

P_c [3]

T_c [3]

V_c [3]

4.57 MPa

452.7 K

0.1 m³/kmol

Return to

[Gas Index]

[Fluid Source Group]

[Process Measurements Division]

[NIST Home]

[SEMI]

[NISTP]

T	C _p ^o (T)	Vapor Pressure	B(T)	dB/dT	C(T)	dc/dT	λ	η
K	R	MPa	cm ³ /mol ³	cm ³ /mol ³ ·T ⁻¹	cm ⁶ /mol ²	cm ⁶ /mol ² ·T ⁻¹	mW/(m·K)	μPa·s
Estimated Uncertainty	1%/10%	1%	Gas densities are calculated to better than 0.1% over the temperature and pressure ranges of the reference.				10%	10%
Reference	[47]	[6]	[5]	[5]	[5]	[5]	[5]	[5]
205	11.84	0.19	-2001.6	5951.2	-4658932	47121716	-	-
210	12.00	0.34	-1864.5	5441.0	-3653771	36754361	-	-
215	12.16	0.58	-1741.8	4994.1	-2884907	28924191	5.2	14.17
220	12.32	0.95	-1631.6	4600.8	-2291407	22949084	5.3	14.41
225	12.48	1.53	-1532.2	4252.9	-1829413	18345717	5.6	14.64
230	12.64	2.39	-1442.1	3943.9	-1466994	14767456	5.7	14.88
235	12.80	3.62	-1360.3	3668.3	-1180656	11962851	5.9	15.11
240	12.95	5.37	-1285.7	3421.6	-952936	9747555	6.0	15.35
245	13.10	7.79	-1217.5	3199.8	-770738	7985050	6.2	15.58
250	13.25	11.08	-1154.9	2999.9	-624150	6573288	6.3	15.81
255	13.40	15.47	-1097.3	2819.0	-505611	5435305	6.5	16.05
260	13.55	21.22	-1044.2	2654.8	-409306	4512569	6.6	16.28
265	13.70	28.66	-995.0	2505.4	-330733	3760214	6.8	16.51

Figure 3. Sample page from on-line database located at <http://properties.nist.gov/semiprop/>.

We have developed a diverse series of primary standards for gas flow. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10⁻³ mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5–9 atmospheres. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle. The second and third standards have a standard

uncertainty of 0.02 %. Figure 4 demonstrates the accuracy of the flow standards.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations, such as MFC manufacturers. Although a flow meter manufacturer often uses its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at fabrication facilities and MFC manufacturers. The second-generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography. It has been used for comparisons with metrological institutes of other countries as well as manufacturers of flow meters. Its standard uncertainty is 0.03 %. The third-generation standard improves convenience by combining the quartz capillary with commercial instrumentation to measure pressure and temperature.

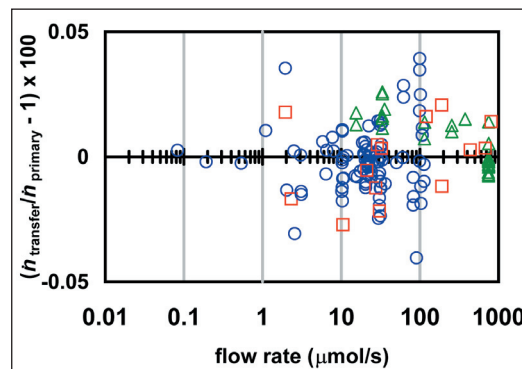


Figure 4. Comparison of three primary flow meters. The transfer standard compared the constant-pressure flow meter (circles) with the gravimetric flow meter (squares) and a constant-volume flow meter (triangles). (1 μmol/s ≈ 1.3 sccm.)

DELIVERABLES: Install new spherical resonator for measuring the speed of sound in the hazardous gases facility. 2Q 2005. Calibrate resonator by 3Q 2005.

A cylindrical resonator was used to study nine process gases, but it must be replaced due to contamination. A spherical resonator has been fabricated and will be installed in the hazardous gas handling facility. The spherical resonator will be

capable of producing higher accuracy measurements than the cylindrical resonator.

DELIVERABLES: Develop improved model of acoustic viscometer by 2Q 2005, develop model of acoustic thermal conductivity resonator by 3Q 2005.

The second-generation Greenspan viscometer incorporates lessons learned from the previous device, thereby allowing an improved acoustic model. The model of the thermal conductivity acoustic resonator will need to be tested and further developed from calibration measurements.

DELIVERABLES: Install second-generation Greenspan viscometer in hazardous gas facility by 1Q FY2005; write and test automation software by 1Q FY2005. Install gas thermal conductivity device in test facility by 2Q FY2005; write and test automation software by 3Q FY2005.

The improved Greenspan viscometer will be installed in the existing hazardous gas handling facility and the software running the apparatus modified. The thermal conductivity acoustic resonator needs to be incorporated into the facility to provide temperature and pressure control, and the computer code developed to run the system.

DELIVERABLES: From the speed-of-sound measurements, determine the ideal-gas heat capacity and equation of state for each species. Calibration gases by 2Q 2005, octafluoro-cyclobutane by 3Q 2005, and ammonia 4Q 2005.

DELIVERABLES: Measure the transport properties in the semiconductor process gases identified by the customer. Calibration gases by Q1 2005, octafluoro-cyclobutane by 3Q 2005, ammonia 4Q 2005.

Each new resonator must be calibrated with test gases such as helium and argon. After calibration and the appropriate safety assessments, the measurements of the semiconductor process gases will begin.

DELIVERABLES: Update on-line database by 4Q 2004, publish viscosity measurements in NF_3 and N_2O by 2Q 2005.

The measurements will be disseminated through papers in professional journals, talks given at professional meetings, and the on-line database.

DELIVERABLE: Submit to archival journal a paper on primary gas flow standards by 1Q 2005.

DELIVERABLE: Repackage transfer standard based on commercial measurement package by 2Q 2005.

The third-generation transfer standard will use commercial instrumentation to measure the pressures and temperature of gas flowing through a quartz capillary. The commercial instrumentation will improve the flow meter's convenience, and the quartz capillary will be the similar to that of the second-generation standard. Using the same capillary and model will ensure an uncertainty of 0.1 %. An improved design based on preliminary tests will improve the reliability of the capillary package.

DELIVERABLE: Test prototype Coriolis flow meter for gases by 2Q 2005.

Coriolis flow meters are the only devices that measure directly mass flow rate instead of a secondary quantity such as velocity or heat loss. The prototype flow meter is designed to measure the small Coriolis forces induced by flows less than 1000 sccm.

DELIVERABLE: Draft SP-250 for gas flow calibrations by 3Q 2005.

The SP-250 document will be used to establish a routine calibration service at NIST for gas flows in the range from 10^{-7} to 10^{-3} mol/s (0.1 to 1000 sccm).

ACCOMPLISHMENTS

- We designed and assembled a second-generation Greenspan viscometer. Its Monel construction allows the study of corrosive process gases.

- We measured the speed of sound in the process gases Cl_2 , NF_3 , and N_2O . Typically, the standard uncertainty of the speed of sound was less than 0.01 %. From these data the ideal-gas heat-capacity was determined to within 0.1 %, and an equation of state was developed to predict the gas densities to within 0.1 %. Viscosity was measured in these three gases plus CF_4 and C_2F_6 with an uncertainty of approximately 0.5 %.

- We continued to provide immediate access to our results by updating the database of gas properties at <http://properties.nist.gov/semiprop/>.

- We verified the accuracy of the primary flow meters by comparing the lower and upper ends of their ranges with other, overlapping NIST flow meters. Near both the lower end (0.3 sccm) and the upper end (1000 sccm) the agreement of 0.03 % was within the mutual uncertainty of the comparison.

■ We used the second-generation transfer standard and a prototype of the third-generation transfer standard to make a comparison of gas flows with a manufacturer of mass flow controllers.

■ We improved the temperature control of the constant-pressure primary flow meter to 0.01 K. We used additional temperature and volume measurements to further characterize this primary standard.

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LOW CONCENTRATION OF HUMIDITY STANDARDS

GOALS

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

CUSTOMER NEEDS

As discussed in the 2004 International Technology Roadmap for Semiconductors (ITRS) in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 115 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes. The 2004 ITRS also includes greater emphasis on epitaxial processes that use gases as source materials, including SiGe and III-V semiconductor requirements in Tables 55a (for power amplifiers) and Table 121 (extension of physical models to III-V semiconductors).

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

TECHNICAL STRATEGY

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can

be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

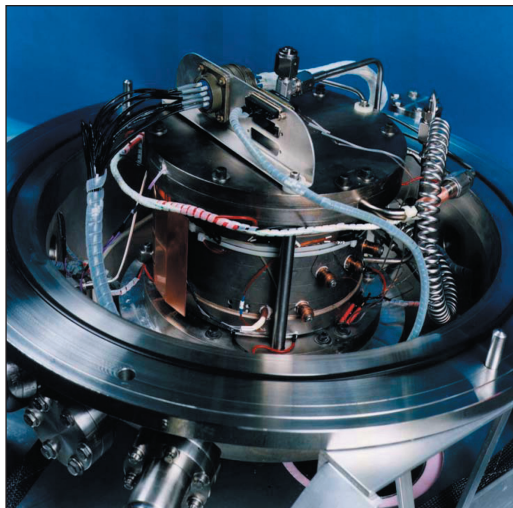


Figure 1. NIST Low Frost-Point (humidity) Generator.

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2), serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it has been used to characterize water vapor measurement and generation systems at the research and development stage as well as commercial devices.

Technical Contacts:

J. T. Hodges
D. Ripple
K. Bertness

“The LFPG is the ‘Gold’ standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard.”

Suhas Ketkar,
Air Products and Chemicals

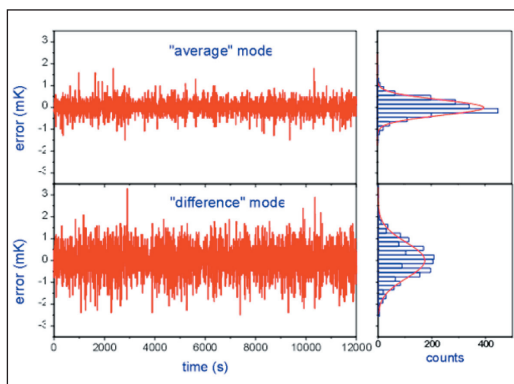


Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We have constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. Experience with the system has revealed several limitations of traditional implementations, including deviations of the output from the equation generally used to predict the temperature dependence of the permeation rate.

DELIVERABLES: Complete uncertainty analysis of permeation-tube calibration system. 3Q 2005. Complete study of temperature dependence of permeation tubes. 1Q 2006.

2. The basis for the LFPG as a humidity standard is knowledge of the temperature-dependent ice vapor pressure. The most commonly used correlation is that developed by Wexler of NBS. By generating a single moisture concentration either directly with the LFPG, or by diluting the water vapor/gas mixture produced by the LFPG with dry gas, we have validated the Wexler correlation.

DELIVERABLES: Quantitatively analyze and publish measurements of dilution tests. 4Q 2005

3. The LFPG is currently limited to generating greater than 3 nmol mol⁻¹ of water vapor in N₂ based on the minimum achievable temperature of the saturator, and knowledge of the ice vapor

pressure discussed above. We have recently demonstrated a new strategy for pmol mol⁻¹-level humidity generation using dry-gas dilution of the water vapor/gas mixtures produced by the LFPG output streamified. Presently, we are establishing the uncertainties and optimal methodologies for this technique.

DELIVERABLES: Document methods and uncertainty of extending the LFPG to pmol mol⁻¹ levels of humidity generation. 4Q 2005

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct rovibrational absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line intensities. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below 10¹⁰ molecules cm⁻³. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method. CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized single-mode cavity ring-down spectroscopy (FSSM-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the

frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity (see Fig. 3).

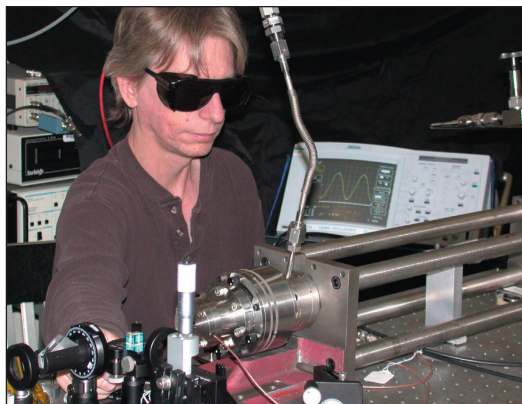


Figure 3. Frequency-stabilized CRDS system.

Using the existing FSSM-CRDS apparatus, appropriate transfer standard generators and hygrometers, we will link H_2O transition line intensities to thermodynamic-based LFPG. Taking advantage of the high spectral resolution afforded by FSSM-CRDS, various line shape effects such as speed-dependent pressure-broadening and collisional narrowing of these transition line shapes by various media will also be quantified.

DELIVERABLES: Link H_2O transition line intensities to LFPG for water vapor concentration measurements in the range 10 nmol mol^{-1} to $100 \text{ } \mu\text{mol mol}^{-1}$ and measure line shape effects in N_2 and other gases. 3Q 2005.

5. Moisture contamination is a serious problem in phosphine, arsine, silane, ammonia, and similar gases used in the epitaxial growth of high-purity semiconductor layers. Semiconductor device manufacturers have expressed frustration with the irreproducibility of source material purity from vendor lot to vendor lot. The critical concentrations of the impurities are not well known; however, it is believed that $>10 \text{ nmol/mol}$ oxygen or water in most process gases is undesirable. Optical methods for measuring the moisture impurity concentrations combine high sensitivity and straight-forward traceability through the LFPG absorption line strength measurements. In collaboration with researchers in the NIST Chemical Science and Technology Laboratory, researchers in the NIST Electronics and Electrical Engineering Laboratory have developed a CRDS system linked with a semiconductor crystal growth system to measure H_2O at very low concentrations in semiconductor source gases and to correlate

the process gas impurities with crystal properties. The system is being used to measure the lineshape, absorption coefficients, and frequency of optical transitions for water, phosphine, and ammonia in the vicinity of 935 nm and 1380 nm. This information is critical to facilitate the use of high-sensitivity spectroscopy techniques in these gases. The laboratory is equipped to allow safe handling of toxic gases such as phosphine and arsine, enabling collaborative experiments with industry on direct measurements of moisture in those gases. The CRDS capability should ultimately lead to improvements in semiconductor source gas purity, which will allow crystal growers to choose less expensive growth conditions without sacrificing optical emission efficiency and yield in LEDs, semiconductor lasers, and photodetectors.

DELIVERABLES: Modify CRDS system for parallel tests with commercial instrumentation and conduct joint experiments on H_2O in phosphine. 3Q 2005

Measure phosphine absorption lines in vicinity of H_2O transition line at 943.082 nm and compare to previous H_2O lines explored for overlap with phosphine. If new line offers superior sensitivity, measure pressure broadening coefficients for H_2O in phosphine. 4Q 2005

ACCOMPLISHMENTS

■ We have constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and high-sensitivity quartz crystal microbalance (QCM). The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a precisely controlled stream of purified N_2 . The diluent gas flow rate is adjusted so that the



Figure 4. New PTG calibration apparatus.

water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1 %, which is significantly superior to traditional gravimetric methods.

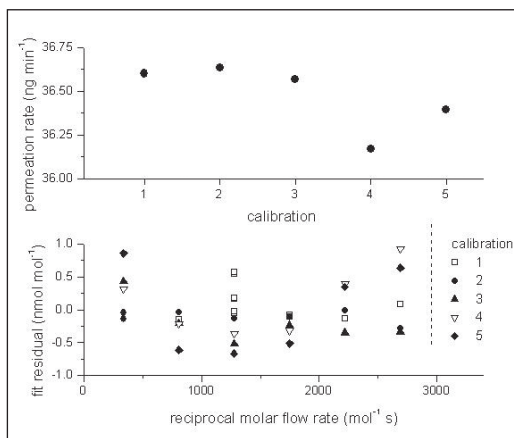


Figure 5. Calibration repeatability (top) and deviations from the fitting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

■ A new strategy for pmol mol^{-1} (ppt) -level humidity generation has been successfully implemented. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above. A check of the consistency of the ice vapor pressure correlation used at NIST was performed over the temperature range between $-95\text{ }^{\circ}\text{C}$ to $-82\text{ }^{\circ}\text{C}$. A nominally constant humidity test point of 14 parts per billion (ppb) was produced by diluting water

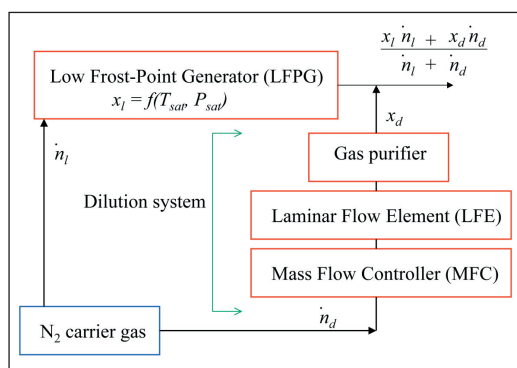


Figure 6. Proposed dilution system for extending the LFPG operating range to pmol mol^{-1} levels.

vapor / nitrogen mixtures from 14 ppb to 140 ppb with purified nitrogen. Measurements obtained using a quartz crystal micro-balance produced the same humidity value for all points, within the expected uncertainty of the system of analyzer and connecting tubing.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 7, indicate that the background contribution to H_2O from system components downstream of the LFPG was less than 0.2 nmol/mol . These measurements also demonstrated that linearity deviations of the LFPG output H_2O mole fraction are less than 0.1 nmol/mol .

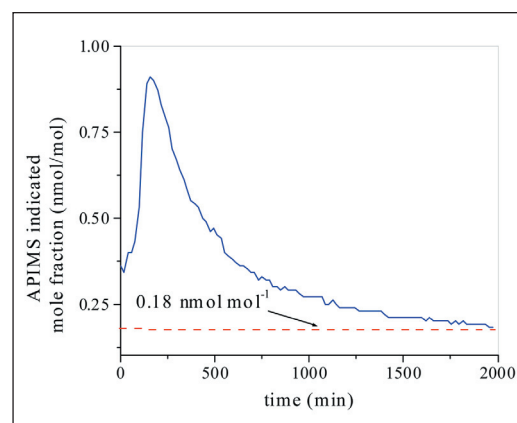


Figure 7. APIMS measurement of LFPG background H_2O concentration showing decay to steady state level.

■ We have successfully developed an FSSM-CRDS system to study the optical absorption of trace levels of water vapor with a resolution and accuracy unobtainable with other techniques. The system is based on a near-infrared continuous wave diode laser emitting over the range 917 nm to 943 nm. The gas sampling system is optimized for high-precision measurements of trace water vapor

concentration. The flow system has all-metal seals, low dead volume, and active mass flow rate and pressure regulation. Background levels $< 0.5 \text{ nmol mol}^{-1}$ (background equivalent) have been demonstrated. The FSSM-CRDS method was used to probe water vapor absorption transitions in the 936-nm spectral region. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line intensities less than 1 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N_2 as the buffer gas). These results illustrate that the spectral resolution and linearity of the FSSM-CRDS method enable precise quantification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determination of number density and line intensity that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm accessible with the near-ir diode laser used in this system.

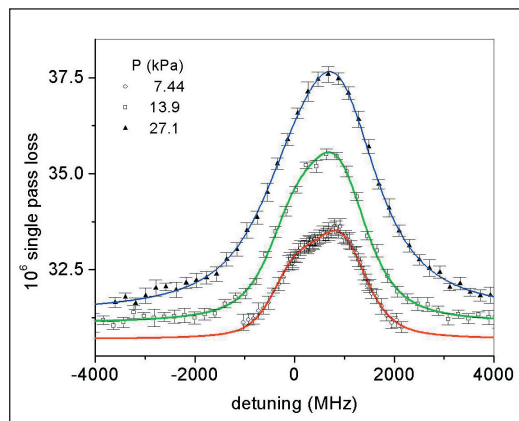


Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

We have used a similar FSSM CRDS system to measure water vapor concentrations in the toxic gas phosphine in the 935-nm spectral region. Testing of five strong water absorption lines in this region indicated that the least overlap with phosphine lines, and hence the highest sensitivity to water contamination, is present for the line at 943.082 nm. Future experiments will characterize

this line for pressure broadening coefficients and ultimate sensitivity limits. Figure 9 shows a typical H_2O spectrum obtained with the automated FSSM-CRDS system and comparison with previously published measurements.

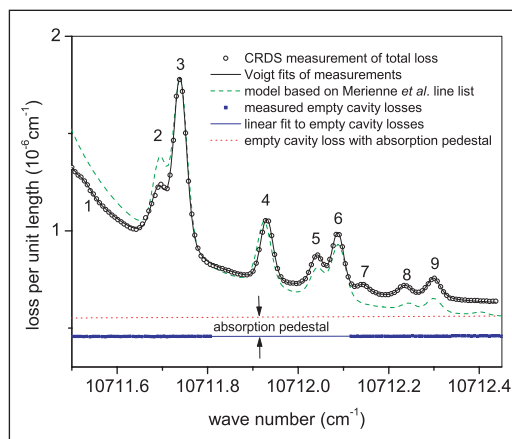


Figure 9. Survey spectrum of water vapor obtained with frequency stabilized CRDS apparatus. The numbers correspond to peaks of individual absorption transitions.

COLLABORATIONS

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

Matheson Tri-Gas, Mark Raynor and Hans Funke; CRDS measurements of trace moisture in phosphine.

Tiger Optics, Yu Chen; CRDS measurements of trace moisture in phosphine.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

Tiger Optics, Calvin Krusen ; evaluation of commercial CRDS technology.

Air Products and Chemicals Inc.; CRDS measurements of trace H_2O in corrosive process gases.

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TEMPERATURE MEASUREMENTS AND STANDARDS FOR RAPID SEMICONDUCTOR PROCESSING

GOALS

The goal is to develop the technologies required to enable the improved accuracy of temperature measurements in semiconductor wafer processing as prescribed in the International Technology Roadmap for Semiconductor (ITRS).

Our project, initiated in 1997, has resulted in improved calibration wafer technology based on thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers for in-tool radiation thermometer (RT) calibration, achieving a 2 °C standard uncertainty of measurements in rapid thermal processing (RTP) tools. We have also developed improved procedures for the calibration of lightpipe radiation thermometers and theoretical models for the relationship between the true wafer temperature and the indicated radiance temperature. With the completion of this work, we are now focusing on: 1) collaborating with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements, 2) developing new resistance sensors for the range 300 to 600 °C, and 3) understanding measurement errors when calibration wafers are used in non-isothermal environments.

CUSTOMER NEEDS

The measurement needs of the semiconductor manufacturing industry have been stated in the ITRS. The requirement is for measurement and control of RTP tools to ± 2 °C during dopant anneal with calibrations traceable to the International Temperature Scale of 1990 (ITS-90). In the 2004 edition of the ITRS in the section on "Metrology Difficult Challenges" the roadmap states "Better sensors must be developed for ... wafer temperature measurement during RTA."

Current needs include better temperature measurement uncertainty in post exposure bake (PEB) processing of resists and in rapid thermal processing (RTP) of wafers including silicide formation in the temperature range of 300 °C to 700 °C. Understanding differences of temperature readings between different instrumented wafers is also a high priority.

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation.

This community forms our project's Common Interest Group (CIG), 20 companies meeting annually since 1997. They serve as a bridge between research and practice, provide advice on shaping objectives, and generate opportunities for technology transfer. We have had our NIST patented thin-film thermocouple wafer evaluated at the ISMT (Sematech)/ University of Texas RTP LPRT test facility and at Vortek Ltd. manufacturers of RTP tools. Currently Applied Materials and Atmel, both RTP tool manufacturers, are evaluating the NIST test wafer.

TECHNICAL STRATEGY

Our research is focused on four projects that will enable the semiconductor industry to meet the roadmap requirements: (a) support our industrial collaborators in the use of test wafers with improved thin-film technology to demonstrate in-tool calibration of RTs traceable to the ITS-90, (b) develop new, accurate sensors for the 300 °C to 700 °C range, where commercial sensors are inadequate, (c) investigate effects on measurements of imperfect thermal environments, and (d) develop silicon-wafer emittance standards for improved temperature and emittance measurements.

Cooperative projects with Applied Materials and Atmel industries are investigating the use of the NIST calibration wafers in industrial RTP tools. These evaluations are critical for transferring the NIST developments to the semiconductor processing industry. The NIST TFTC calibration wafer has demonstrated unique capabilities in temperature measurements and in establishing traceability to the ITS-90. We have also prepared a document "Instructions for use of the NIST Thin-Film Thermocouple Calibration Wafer" in response to requests from our CIG. It is being reviewed by our users and will be finalized by 12/31/05.

DELIVERABLES: NIST TFTC calibration wafers and instructions for application of NIST calibration wafer, and joint report with Applied Materials and Atmel on LPRT calibrations. 3Q 2005

Members of our CIG have also asked us to develop calibrated thin-film resistors for wafer temperature measurement from 300 °C to 600 °C. These measurements are needed for more accurate control of the silicide anneal RTP. We have

Technical Contacts:

D. Ripple
B. Tsai

"On behalf of SensArray Corporation, I express our deep gratitude to NIST for significantly contributing to advances in semiconductor lithography process optimization and control. NIST has contributed to improved CD control in lithography processes through the establishment of measurement methods and standards for wafer thermal bake cycle dynamics in resist processing. This support is just in time, as the next area of focus for photo resist processing optimization is bake cycle dynamics. Your work will be of value to every advanced semiconductor factory."

Wayne Renken, President
SensArray Corp.

undertaken the development of precision platinum thin-film RTDs directly on the silicon wafers to improve the uncertainty of *in situ* wafer temperature measurement at these temperatures. Initial results are promising, and have motivated new work concentrating on reducing hysteresis and uncertainty, and on achieving high and repeatable values of the thermal coefficient of resistivity.

DELIVERABLES: Report on the uncertainty and temperature range of thin-film Pt resistor thermometers directly on Si wafers. 3Q 2006

As a first step in determining the sensitivity of a sensor on an instrumented wafer to a non-iso-thermal environment, it is necessary to measure the thermal resistance between the sensor and the silicon substrate. We are developing a technique where the temperature of the silicon wafer is modulated, and the response of the sensor measured synchronously. Simple theoretical models can be fit to the data to ascertain the thermal resistance between sensor and wafer. This technique is envisioned as a useful quality-assurance tool for manufacturers of instrumented wafers.

DELIVERABLES: Paper on measuring the thermal response time of commercial embedded sensors. 3Q 2005.

CIG meetings have been held annually since 1997 for the purposes of assessing and planning project research directions, and for fostering collaborative work with equipment suppliers, chip makers, and instrumentation suppliers. At the 12th International Conference on Advanced Thermal Processing of Semiconductors (RTP'04, Sept., 2004, Portland, OR), the meeting addressed several major needs in temperature measurement. We had requests by our industrial collaborators for test wafer demonstrations and discussions on proposals for establishing emittance standard wafers. At RTP'04 our team organized two regular conference sessions under the theme of traceability of RTP temperature measurements. Papers were presented on TC and RT calibrations methods and thermal modeling. A panel discussed plans for an industry-wide emittance standards initiative. An important contribution by NIST to the initiative is the use of the high temperature properties measurement facilities to generate a reliable, traceable database and to validate optical properties models.

DELIVERABLES: Organize and conduct CIG meeting on traceable temperature measurements at key industry RTP conference. 4Q 2005

ACCOMPLISHMENTS

DEVELOPMENT OF RESISTANCE SENSORS FOR 300 °C TO 700 °C APPLICATIONS

We have explored the performance of platinum resistance thermometers deposited directly on oxide-coated silicon wafers. Our work has measured the effects of thickness and bond coat (Ti or Zr) of the Pt thin films. We have also measured the effect of ambient atmosphere (air or nitrogen) on the hysteresis and thermal coefficient of resistivity, α . The value of α was not sensitive to the annealing temperature or Ti bond-coat thickness, but did depend on the Pt thickness.

CALIBRATION OF LPRTS IN THE RANGE 300 °C TO 700 °C

LPRTs have become mainstream in the temperature measurement in the RTP community. We have calibrated LPRTs for RTP applications using a sodium heat-pipe blackbody between 700 °C and 900 °C with an uncertainty of about 0.3 °C ($k=1$) traceable to the ITS-90. Recently, cable-less LPRTs (CLRTs) offer a decisive advantage to enable radiometric measurements at lower temperatures than traditional LPRTs. New application of CLRTs can eliminate 2.0 °C or more uncertainty from the calibration scheme. We have used the NIST RTP Test Bed to perform intercomparisons between the TFTCs and the new low-temperature (300 °C to 700 °C) CLRTs. Our study has established calibration uncertainties for comparison of CLRTs against the TFTCs *in situ*, and has established uncertainties for model-corrected CLRTs calibrated against blackbodies.

LIGHTPIPE PROXIMITY

We designed an experimental and analytical study to quantify the lightpipe proximity effect and provide a model for industrial users of LPRTs to correct their LPRT readings. The experiments employed TFTC wafers, our RTP test bed, and LPRT readings to characterize the effects of lightpipe proximity on wafer temperatures. We found that the wafer temperature can be depressed more than 20 °C by positioning the lightpipe tip too close to the wafer. These results were presented in a paper for the 2003 International Conference on Characterization and Metrology for ULSI Technology and at the 2003 10th International Conference on Advanced Thermal Processing of Semiconductors (RTP 03).

TRANSIENT RESPONSE OF TEMPERATURE SENSORS DURING THE POST EXPOSURE BAKE PROCESS

Recent studies on dynamic temperature profiling and lithographic performance modeling of the PEB process have demonstrated that the rate of heating and cooling may have an important influence on resist lithographic response. We conducted an experimental and analytical study to compare the transient response of commercial, embedded platinum resistance thermometer (PRT) sensors with surface-deposited TFTCs. A dual instrumented wafer for PEB evaluation is shown in Fig 1. Experiments were performed on a commercial module using wafers instrumented with calibrated type-E TFTCs and commercial PRTs.

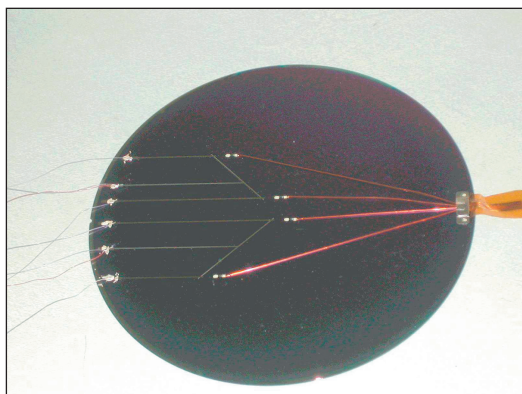


Figure 1. Wafer instrumented with PRTs and type-E thin-film thermocouples.

We measured the temperature of 200 mm Si wafers in a commercial-type PEB module using both embedded PRTs and thin-film thermocouples (TFTCs) through a typical thermal cycle from ambient, to 150 °C, and back to ambient. The transient response of the TFTCs led the PRT sensors, indicating a PRT lag (typically) of 2 °C on heating and up to 4 °C on cooling for several seconds. The wafer time constants for response were strongly affected by the air gap distance between the wafer and hot plate as expected. Thermal models were presented that showed estimates for heating time constants in good agreement with experimental data. Lithography simulation results were presented that showed the effects of transient and offset temperature profiles on CD variations.

CALIBRATION OF PRT SENSORS FOR INSTRUMENTED WAFERS

Calibration of PRTs that have been imbedded in instrumented wafers presents a challenge for the manufacturer: the wafers are much larger than commonly calibrated thermometers, the calibration process cannot contaminate wafers intended for use in a semiconductor-processing facility, and the uncertainty requirements for PEB applications are fairly demanding (standard uncertainty of approximately 0.01 °C). To validate the methods used in industry, a commercial instrumented wafer was calibrated both by NIST and by the manufacturer in the range 15 °C to 95 °C. The results were well within the stated manufacturing tolerance of the wafer and our expectations for the sensors used on the wafers.

EMITTANCE STANDARDS INITIATIVE

During the RTP 2003 Meeting in Charleston, SC, a whole session was dedicated to the introduction of the emittance standards initiative. The session was opened by comments from Steve Knight, the NIST OMP Director, who explained the role of NIST in the initiative. Three talks focused on NIST's role in the initiative and explained the NIST room-temperature reflectance facility, the NIST high-temperature emittance facility, and experimentally validated optical property models for semiconductor materials. The climax of the meeting occurred when a panel of experts in the RTP industry discussed the need for creating emittance standards with measurements traceable to NIST and explained what the standards would entail. A summary of conclusions and action items were listed, and the final outcome was the unanimous desire and support for creating emittance standards, as voiced by the panel. Invitations were issued to five different RTP manufacturers and users, who had expressed a need for emittance standards. To date, four of the five vendors have already submitted sets of silicon wafer standards for measurement. The high-temperature facility is being set up to commence characterization of the standards.

LASER-REFLECTOMETER RADIATION THERMOMETER

A Laser-Reflectometer Radiation Thermometer (LRRT) employs a reflectometer to measure normal reflectance and Kirchhoff's Law to calculate the emissivity. The measurements of the emissivity and the radiance temperature can be

combined to determine the true surface temperature. Although alignment was very sensitive and frequent *in-situ* emissivity calibrations with the LRRT was necessary, the measured emissivity values differed from NIST measurements with the Spectral Tri-function Automated Reference Reflectometer (STARR) facility by less than 2 %, while the measured temperatures differed with the NIST thin-film thermocouples by less than 4 °C. With improvements in the LRRT, it is possible to take advantage of the emissivity measurement to make a more accurate temperature measurement of the wafer during processing.

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PLASMA PROCESS METROLOGY

GOALS

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

CUSTOMER NEEDS

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the 2004 update to the International Technology Roadmap for Semiconductors (ITRS) identifies a need for better, more predictive modeling of the impact of equipment on process results (Modeling and Simulation section, page 11, Table 122c). To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, the dependence of these properties on processing equipment, and the effect of these properties on process results, further progress in model development and validation is required. The ITRS also identifies a need for development of robust sensors and process controllers (Metrology section, page 2, Table 115) which are able to convert large quantities of raw data into information useful for improving manufacturability and yield.

TECHNICAL STRATEGY

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semiconductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

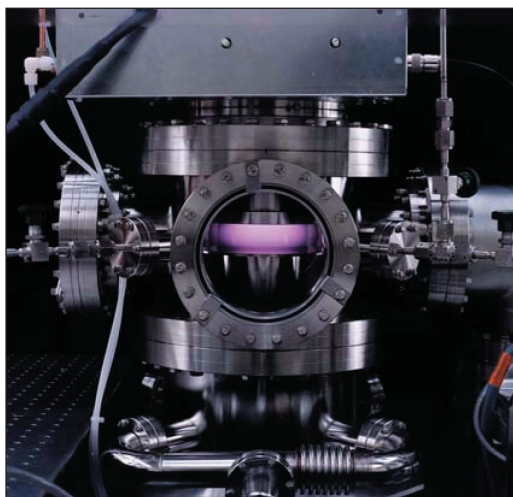


Figure 1. One of the inductive, high-density plasma reactors used in our experimental studies.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. An electrical measurement technique developed at NIST for use in process monitoring and

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“NIST is one of the leaders in plasma processing related research in the U.S. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools.”

Peter Ventzek
Motorola

“The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries.”

Bing Ji,
Air Products and
Chemicals, Inc.

control applications continues to be the subject of further testing and validation. This technique relies on noninvasive, nonperturbing measurements of the radio-frequency (rf) current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of the plasma and its sheaths. To validate the technique, experiments in an rf-biased, inductively coupled plasma reactor have been performed both with and without silicon wafers loaded in the reactor. Plasma potentials, sheath voltages, total ion currents, and ion energy distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. The technique has been used to monitor long-term drift in ion energy and total ion flux. We have also monitored the more rapid changes that occur when the pressure, power, and gas flow are perturbed in ways that mimic equipment faults. Future efforts are directed towards demonstration of the usefulness of the technique in industrial plasma reactors. We have begun a collaboration with an industrial company in which we will perform tests in a prototype commercial reactor equipped with an electrostatic chuck. The tests will evaluate the validity and usefulness of the NIST-developed electrical measurements, models, and analysis techniques in the commercial reactor.

DELIVERABLES: Evaluate the validity and utility of rf measurement techniques, electrical models, and analysis techniques in a commercial plasma reactor. 2Q 2006

2. A new method for measuring electron number density in plasmas, the wave cut-off method, has recently been developed at KRISS, the Korea Research Institute of Standards and Science. The technique can be used to characterize spatial variations in the electron density without many of the disadvantages of traditional Langmuir probe measurements. Information provided by the wave cut-off technique, if it is shown to be of sufficient reliability and accuracy, would be of use in the further development and testing of plasma models. It would also provide a better understanding of important electron collisions in plasmas as well as the factors that influence plasma spatial uniformity. We will be collaborating

with a guest researcher from KRISS to implement the wave cut-off technique in our laboratory and to evaluate its accuracy and usefulness.

DELIVERABLES: Implement and evaluate the wave cut-off method for measuring electron density in plasmas. 2Q 2006

3. Many industrial plasma etchers are equipped with optical emission spectrometers, which have proven useful for endpoint detection, fault detection and classification, and automatic process control. At present we are planning and initiating experiments in which optical emission measurements will be combined with the noninvasive electrical measurements described in item 1, above. Optical emission complements the electrical measurements by providing information about drift or other changes in the chemical species within the plasma—information that would be difficult or impossible to obtain solely from electrical measurements. We will evaluate whether data provided by optical emission can be used by the electrical analysis algorithms to obtain increased accuracy in ion current and ion energy monitoring. We also plan to assess the relative merits of optical and electrical detection of various types of process drift, equipment faults, and other changes such as etch endpoint.

DELIVERABLES: Compare sensitivity and utility of optical emission and electrical techniques for monitoring drift in etching reactors. Evaluate improvements gained by combining electrical and optical emission measurements. 4Q 2005

4. Dual frequency capacitively-coupled plasma (CCP) sources are becoming increasingly important in semiconductor manufacturing processes, however, there appear to exist only limited amounts of published data on these plasma sources. Most experimental papers concentrate solely on the source etching characteristics, and numerous theory papers on the dual-frequency sources show few comparisons with actual experimental data. We will address several issues related to dual frequency sources, concentrating on how the sheath is affected by the dual frequencies. How does applying the two rf frequencies to a single electrode compare with applying the frequencies to separate electrodes? How does varying the two frequencies modify the plasma? How independent is the ion energy control and plasma production? We will obtain time-resolved (0.5 ns) spectrographic data from the entire plasma. This data will be combined with measurements of the voltage and current

waveforms. In addition, plasma density will be measured by either microwave interferometry or a plasma frequency cut-off technique.

DELIVERABLES: Measure time-resolved (0.5 ns) spatially-resolved optical emission and plasma electrical characteristics in dual frequency plasmas to determine the effect of dual frequency on plasma characteristics. 2Q 2006

ACCOMPLISHMENTS

■ The NIST-developed, noninvasive, model-based electrical technique for monitoring ion energy and total ion flux has recently been validated in actual etching conditions in CF_4/Ar plasmas (Fig. 2). Unlike previous validations, performed with no wafer present, the recent validations were performed with silicon wafers — oxidized and bare — loaded into the reactor. The wafer, as well as the contact between the wafer and the electrode on which it rests, both contribute an electrical impedance which, if unaccounted for in the model, can cause errors in the ion energy distributions and total ion flux obtained from the noninvasive technique. At low rf bias frequencies < 100 kHz, the contributed impedance was large, resulting in substantial errors in the noninvasive results. Nevertheless, at bias frequencies of 1 MHz or higher, which are more typical of semiconductor manufacturing, the wafer and wafer contact contribute only a few ohms of impedance, resulting in an uncertainty in noninvasive ion energies of only a few electron volts. The speed of the analysis algorithms has also recently been greatly increased, making it possible to monitor changes in ion energy and total ion flux with a time resolution on the order of 1 second. In recent demonstrations,

the speeded-up technique has been used to monitor small changes in ion energy and total ion flux that occur over the course of a “normal” oxide etch, as well as larger changes that occur when the pressure, power, and gas flow were perturbed in ways that simulate equipment faults.

■ Sub-millimeter wave absorption spectroscopy is being developed as a plasma diagnostic to identify and monitor species in etching plasmas (Fig. 3). Sub-mm wave spectroscopy can monitor the crucial chemical species in a plasma and provide the necessary feedback for understanding plasma processing. This technique was used to measure radical densities in several fluorocarbon: oxygen: argon etching plasmas. The etching rate of SiO_2 in these types of plasmas exhibit a local maxima as a function of the oxygen to fluorocarbon ratio. The sub-mm absorption measurements in C_4F_6 and C_4F_8 containing discharges showed increasing CF and CF_2 radical densities with decreasing oxygen to fluorocarbon ratios for ratios below the SiO_2 etching maximum. In addition, absorption measurements of CO and COF_2 indicate that surface etching of the wafer plays an important role in the CO, but not the COF_2 , radical production. The influence of wafer coatings on the plasma was investigated by comparing the radical densities with different photoresist coated wafers (two types of 157 nm photoresist and an I line photoresist) in an etching plasma. No significant difference was observed between the CF densities for the different wafer coatings, but there was a significantly higher CF_2 density with the I line photoresist than the 157 nm photoresists tested. Time-resolved density measurements demonstrated that plasma conditions were changing during the etching of a single wafer. Both CF

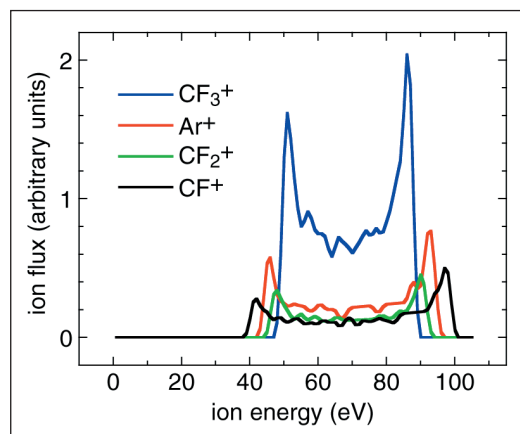


Figure 2. Ion energy distributions from noninvasive electrical measurements, determined in real-time during an oxide etch in an Ar/CF_4 plasma.

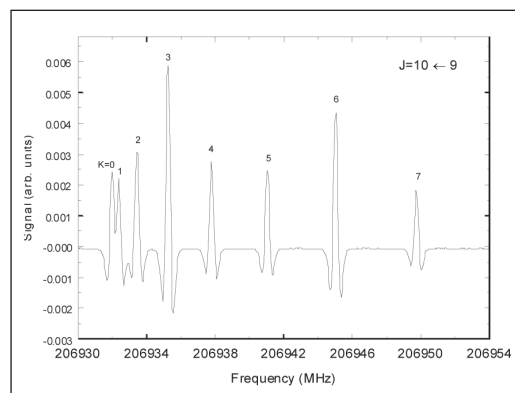


Figure 3. Sub-millimeter wave absorption spectrum of CHF_3 in a high-density, inductively coupled plasma.

and CF_2 demonstrated a gradual rise for the first ~100 seconds followed by relatively constant levels which is probably due to the development of fluorocarbon layers within the plasma etching chamber. The density of CHF_3 showed a strong spike at the start of the discharge which rapidly decayed to a low level during the remainder of the wafer etch, even though no hydrogen containing feed gases were being used. The hydrogen is probably originating from the dissociation of residual water vapor in the vacuum chamber. Together these measurements illustrate the usefulness of sub-mm spectroscopy for providing a useful understanding of plasma radicals and its potential as a process monitoring tool.

■ We have also developed the capability to measure spatially resolved 2-D temperature maps in fluorocarbon plasmas using planar laser-induced fluorescence (PLIF) of the CF radical (Fig. 4). Several PLIF images are measured, each probing a different rotational level to give a 2-D map that is related to the CF population in the probed rotational state. With the relative population for several rotational levels known at each location, a rotational temperature map is calculated and assumed to be equivalent to the gas temperature under these conditions. We have measured temperature maps in CF_4 plasmas as a function of pressure and power, with and without silicon wafers present. Simultaneously, CF density images were obtained. Under our conditions, radial variations in temperature from 10 K to 90 K were observed. Axial temperature gradients were also observed to be quite large, especially under our highest pressure conditions (800 mTorr or 107 Pa). The strongest temperature gradients were consistently found near the cooled electrode surfaces. These variations can have strong implications. Species density measurements that probe a specific rotational level can be misleading if the population of the chosen rotational level is not constant within the temperature range investigated. In addition, gas density in hotter regions will be lower, and this must not be interpreted as a chemical effect. Especially near surfaces, where species density fluxes are often interpreted as indicating surface chemistry, one must be aware of the implications of these temperature effects. In addition, understanding temperature is important for modeling, since chemical reaction rates are often a function of temperature.

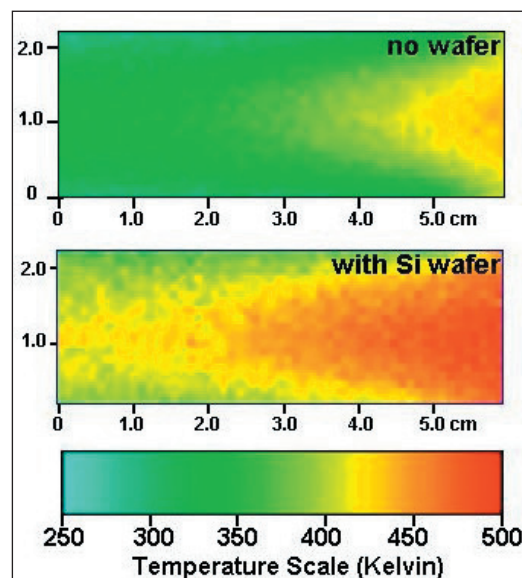


Figure 4. Temperature maps of a capacitively coupled CF_4 plasma at 200 mTorr; with and without a silicon wafer.

■ Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST “Electron Interactions with Plasma Processing Gases” database (<http://eeel.nist.gov/811/refdata/>) (Fig. 5). This Web site has experienced tens of thousands of hits throughout its history.

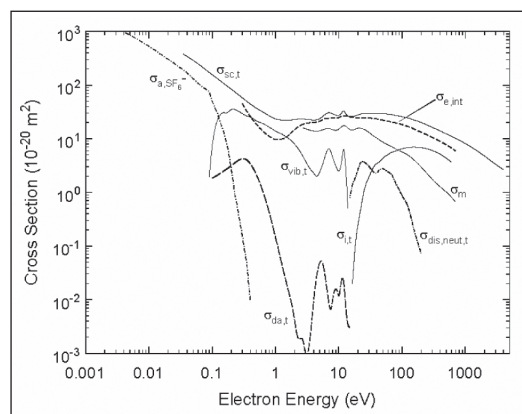


Figure 5. Recommended electron cross section data for SF_6 (shown here) and many other plasma processing gases are available at <http://eeel.nist.gov/811/refdata/>.

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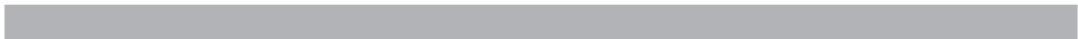
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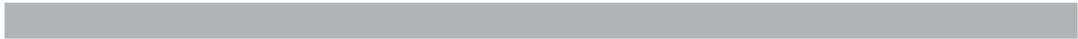
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ANALYSIS TOOLS AND TECHNIQUES PROGRAM

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. The need for new analytical techniques and tools has increased as the components in the transistors approach the low nanometer level and the number of transistors per chip approaches 1 billion. The development of tools capable of characterizing the structures produced in the laboratories as well as those needed to confirm the manufacturing process require significant improvements; although those used for production also require significant speeds not to slow down the commercial manufacturing. This latter condition may require some sacrifices in the resolution and accuracy of those tools. In addition, more significant modeling that allows us to bridge those areas where measurements can be done to those where knowledge is needed from, but measurements cannot be done are critical.



THIN-FILM X-RAY METROLOGY FOR MICROELECTRONICS

GOALS

This multi-year collaborative effort between SEMATECH and NIST will provide the semiconductor community with the methodology for accurate thin film characterization using X-Ray Reflectometry (XRR).

CUSTOMER NEEDS

In recent years, the semiconductor industry has driven scientific advancement towards processing nanometer-scale material coatings with unprecedented uniformity in thickness, composition control, and unique electrical and mechanical properties. Nanotechnology represents the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film processing technologies, the X-ray diffraction user community and instrument manufacturers have collaboratively developed techniques such as High-Resolution X-Ray Diffraction (HRXRD) and X-Ray Reflectometry (XRR) that permit the quantitative profiling of thin film characteristics, such as thickness, density profile, composition, roughness, and strain fields. With the XRR method in particular, parameter modeling by conventional methods can be an intractable problem, involving deconvolution of instrument response, data model theory, model selection, and model refinement/fitting, which has prevented the realization of the technique's potential in the characterization of nano-dimensional thin film structures. This program addresses the mounting industry call for accuracy in thin film characterization (in particular; thickness, density, and roughness determination).

TECHNICAL STRATEGY

This fundamental XRR study involves two parallel characterization projects being performed on identical, temporally stable, multilayer artifacts supplied by SEMATECH. The NIST project consists of in-house XRR and HRXRD characterization with Système International (SI) traceable measurement instrumentation and SI traceable, first principles data modeling including Bayesian analysis providing refinement of instrumental and model parameters as well as structural model selection. In parallel to this NIST measurement effort, SEMATECH will measure or have measurements performed using commercial "in-line"

XRR instrumentation and NIST will analyze these data using commercial software to address limitations to commercial instrumentation and software modeling. Combining results from both studies will ultimately allow accuracy traceability and error estimation for commercial instrumentation. This work will also address theoretical XRR modeling limitations and compare software model refinement and model selection approaches. The multi-year collaboration will provide the community with total error budget estimations for a given XRR structural analysis approach and instrumentation. This work will take approximately three years to address the issues discussed [FY's 05, 06, and 07]. The progress in FY05 includes a comprehensive, first principles development of the XRR theory necessary for traceable modeling of data and a first round of measurements on artifacts by commercial and NIST instrumentation.

NIST XRR Study – The NIST project consists of two parallel research components: 1) the development of SI traceable measurement instrumentation, 2) the creation of an SI traceable, first principles data analysis approach (see Fig. 1).

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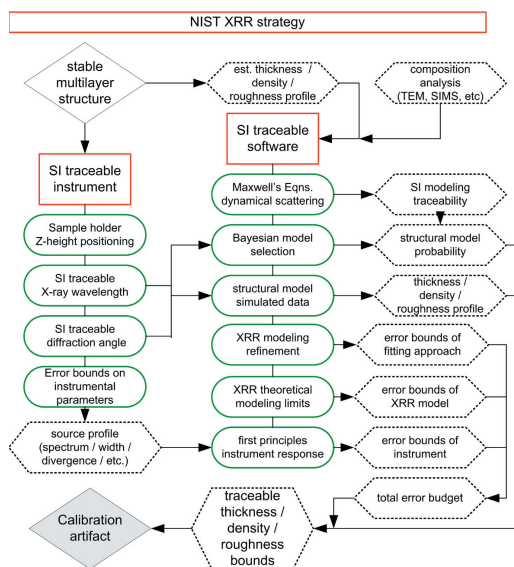


Figure 1. NIST XRR strategy. Measurements and modeling of temporally stable test structures will be performed on the NIST Ceramics Division Parallel Beam Diffractometer – an SI traceable instrumentation constructed for certification of XRD, HRXRD, and XRR Standard Reference Materials.

NIST has made previous efforts in developing in-house instrumentation capable of SI traceability for conventional XRD, HRXRD, and XRR techniques. Over the past seven years, NIST has constructed the Ceramics Division Parallel Beam Diffractometer (CDPBD) for SI traceable measurements of Powder XRD, Epitaxial HRXRD, and thin-film XRR artifacts for the Standard Reference Materials (SRM) program (Fig. 2). SI traceability in lattice parameter (XRD) or film thickness (XRR), d , requires simultaneous traceability in X-ray wavelength, λ , and diffraction angle, θ , following Bragg's law of diffraction: $2d = n\lambda / \sin(\theta)$.

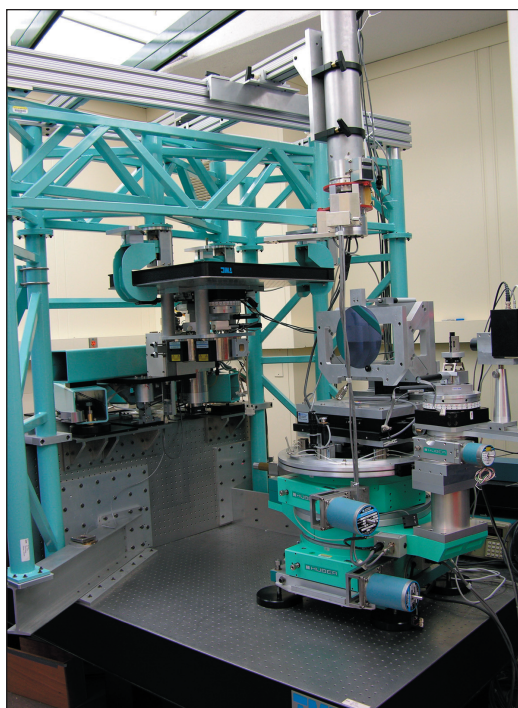


Figure 2. Ceramics Division Parallel Beam Diffractometer (CDPBD). Showing the divergent X-ray source (center left), monochromator for generating parallel/monochromatic X-rays (upper center), rotation stages for measuring diffraction angles (lower right) and receiving optics/detector (center right). In order to achieve accuracy in angle measurements and X-ray wavelength stability, numerous design features of varying complexity are present ranging from a “floating” platform holding the X-ray source to a hanging second rotation stage designed specifically to rotate the cables for the diffraction rotation stages.

The present NIST instrument development project involves addressing SI traceability aspects for both the diffraction angle and wavelength measurement in the CDPBD. Establishing SI traceability of the diffraction angle requires implementing optical encoding on the two rotation stages used to move the sample and detector. The optical encoder errors are then “mapped” using an external angle reference to generate SI traceability error bounds for each axis. The rotation stages presently have accuracy bounds of $\pm 2.0 \mu\text{rads}$ (± 0.4 arc seconds). Calibration experiments and collaboration with encoder manufacturers is currently underway to achieve an approximate one order of magnitude improvement in accuracy by next year [FY06 deliverable]. Determining SI traceability in wavelength involves constructing a stable, well modeled optics assembly to convert angular and energy divergent radiation from an X-ray source into parallel, monochromatic radiation for use in diffraction. The CDPBD uses a monochromator with Si (220), 2/4-bounce channel-cut crystals to filter the direct source into a source of highly parallel, single energy X-rays. SI traceability in X-ray wavelength from our source will be performed using an SI traceable reference crystal (with measured relative uncertainty of 3 in 10^{-8}). The X-ray wavelength for our instrumentation will have a relative uncertainty of ≈ 1 in 10^{-7} [FY06 deliverable]. The accuracy error bounds and instrument parameters from the wavelength and angle determination studies will provide an overall instrument response function which will be incorporated into NIST XRR profile modeling. The same instrumental parameters will establish guidelines for response profile modeling of commercial instrumentation [FY07 deliverable].

NIST is currently developing first principles, SI traceable XRR software to analyze data and refine model and instrument response parameters. XRR analysis is essentially an “inverse problem” wherein we select input parameters for a “guessed” structural model. This model is then used to simulate data that is compared with measured data and “Goodness of Fit” parameters are determined. This process is repeated until a “best fit” or best “Goodness of Fit” is found and the “best fit” model parameters become the “refined” model parameters used to describe the real structure. Three major questions limit the effectiveness of this current XRR modeling approach: 1) How do we accurately simulate the data using a structural model? 2) How do we know which structural model describes the

measured structure? 3) How do we accurately compare simulated and measured data? The NIST software development effort will attempt to answer each of these questions.

To address the model data simulation issue, we are currently developing XRR theory from Maxwell's equations and explaining all approximations and constraints required for the XRR modeling method. This approach will combine XRD, HRXRD and XRR in the same fundamental modeling theory and allow for SI traceability in derived refined parameters [FY05 deliverable]. To address the question of model accuracy, we are implementing a Bayesian/Maximum Entropy analysis approach to determine the probability that a given structural model correctly describes a given data set. This model selection component is essential to determining the validity of initial structural assumptions in any XRR analysis [FY06 deliverable]. Addressing the third question is of considerable interest with current commercial refinement approaches which often use dissimilar "chi squared" or model/simulation minimization criterion for overall refinement "figures of merit" such that comparison between refinement software packages is impossible. NIST will perform a rigorous analysis of current refinement approaches (such as genetic algorithms which are popular in commercial software for their speed advantage, Markov Chains Monte Carlo, simulated annealing, etc.) and of applicable minimization criterion to develop a consistent refinement approach for NIST modeling [FY07 deliverable].

NIST/SEMATECH XRR Study – The NIST/SEMATECH project consists of measurements and analysis from commercial instrumentation to allow comparison and calibration transfer from NIST SI traceable measurements and analysis (Fig. 3).

The NIST/SEMATECH project combines measurements with commercial "in line" XRR instrumentation with complimentary compositional analysis results as feedback for comparison with NIST measurements performed in parallel on the same artifacts. The measurement and modeling work at NIST will provide SI traceable XRR measurements and parameter analysis for artifacts and potential candidate SRMs. The collaboration work with SEMATECH allows interface and calibration transfer between NIST SI traceable measurements and "in-line" instrumentation. NIST will then use results from NIST SI traceable measurements, SEMATECH commercial

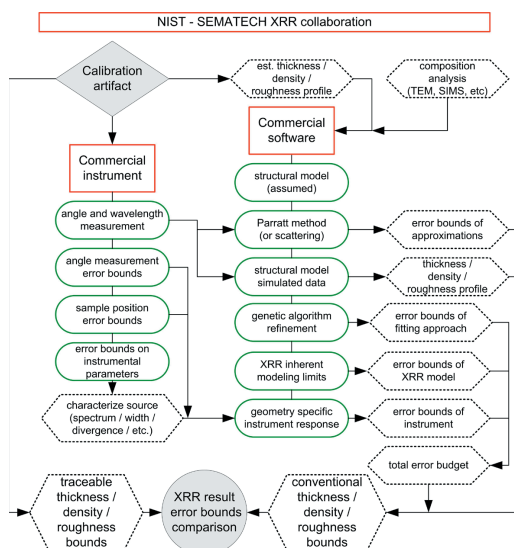


Figure 3. NIST – SEMATECH XRR strategy. Measurements of temporally stable test structures at SEMATECH will be performed on "fabrication-line-based" instrumentation and then analyzed at NIST using commercial software. These results will then be compared with NIST traceable results to provide calibration of commercial instrumentation.

measurements and modeling, and NIST SI traceable XRR modeling, to quantify error bounds and overall error budgets on the accuracy and precision possible from commercial instrumentation and commercial modeling software.

Calibration and accuracy determination of commercial instrumentation are the primary goals of this collaboration. To achieve these goals, we need to develop accurate instrument response functions for commercial instrumentation being calibrated. The instrument response function for commercial instrumentation may be the dominant term in the overall accuracy budget for XRR measurements. To address instrumentation effects on accuracy, work must be performed with different commercial XRR system geometries to discover the mechanical alignment parameters that dominate the error budgets of each system. This will require cooperation from instrument vendors to provide the necessary information or provide detailed instrument response functions directly. The incorporation of instrument response parameters into NIST modeling will allow for comparison between traceable measurements at NIST and measurements on commercial instrumentation in the field. The NIST instrument response function information will be developed through our instrument traceability study discussed earlier. We can then combine specific instrument "corrections"

to the accuracy error budget and use a calibration artifact such as a temporally stable thin film structure measured on the commercial instruments and at NIST to provide instrument calibration and stability monitoring [FY07+ deliverable].

Project Deliverables – The final project results available to SEMATECH will include XRR error budget estimations based on NIST XRR software and the calibration artifacts necessary for optimizing the performance of commercial “in-line” and laboratory XRR instruments. Accuracy and precision estimations provided by NIST software will determine the limitations of XRR applicability for arbitrary multilayer systems on commercial XRR instrumentation. Calibration artifacts measured on NIST SI traceable instrumentation will allow routine system monitoring, alignment calibration, and instrument response function comparisons to ensure commercial instrument precision and stability. These deliverables will dramatically improve the precision and accuracy of conventional XRR characterization of multilayer structures which exhibit well-established composition and uniformity [FY07+ deliverables].

Our deliverables schedule for the calendar year 6/2005-6/2006 time frame follows:

DELIVERABLES: First Principles roughness analysis. 1Q 2006

DELIVERABLES: Approximate Bayesian model selection method. 2Q 2006

DELIVERABLES: NIST analysis of SEMATECH measurements. 2Q 2006

DELIVERABLES: Report comparison of measurement results from ISMT and NIST instruments on same artifacts. 2Q 2006

ACCOMPLISHMENTS

The CDPBD has recently been moved to our new equipment space in the Advanced Measurements Laboratory (AML at NIST) which is currently providing instrument temperature stability of ± 0.02 °C. Preliminary calibration of the angle encoders requires enhancements to current control electronics [4Q 05] to achieve target accuracy [by FY06]. First principles XRR theory development with emphasis on justifying approximations present in commercial XRR software will be completed this year [2Q 05]. Preliminary measurements of SEMATECH artifacts measured by both conventional and NIST traceable XRR systems will be completed this year [2Q 05].

FY05 Technical transfer: minimum thickness determination – Preliminary studies into theoretical limitations of XRR modeling have been completed this spring [2Q FY05] and have provided an approach to establishing the lower thickness limit for which the XRR technique provides useful results. First, data are simulated for a structure similar to the material that is being measured. Second, this simulated data are refined using commercial software. Third, the deviation between simulation input and model output indicates where XRR refinement of real data will fail. This approach can include actual measurement “noise” and real data collection ranges, so that the limits of different instrumentation effects and measurement times can also be analyzed. Figure 4 shows a study result for simulated HfO_2 on Si showing the regime where modeling fails to refine simulation thickness. Deviation provides the “minimum thickness” for which the XRR technique can be used for analysis in this structure. For the measured scan range, modeling fails for thickness < 0.8 nm.

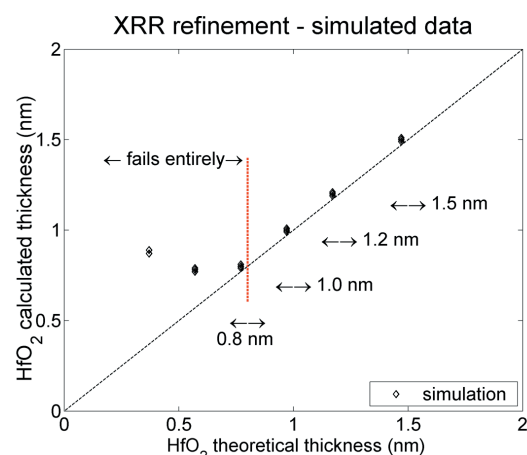


Figure 4. NIST Empirical determination of “minimum thickness.” Simulated data which closely mimics a structure to be measured is modeled using commercial XRR refinement software. The thickness where modeling fails to determine the simulation thickness provides the “minimum thickness” where XRR analysis will provide accurate results on measured data. This analysis must be performed for each structure to be measured, and for the data range/noise levels present in the measured XRR data.

COLLABORATIONS

ISMT, Metrology – P.Y. Hung & Alain Diebold

PTB, Precision Metrology – Peter Thomsen-Schmidt

Bede Scientific Inc. – Keith Bowen & Matthew Wormington

Bruker AXS – Arnt Kern & Alan Coelho

Jordan Valley Semiconductors – Dileep Agnihotri

Technos International – Henry Yeung

D. Windover and J. P. Cline, “Calibration standards for X-ray metrology systems using a traceable high-resolution diffractometer” – poster at American Vacuum Society, Baltimore, MD, November, 2003.

RECENT PUBLICATIONS AND PRESENTATIONS

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N. Armstrong, W. Kalceff, J. P. Cline, and J. Bonevich, “A Bayesian/Maximum Entropy method for certification of a nanocrystallite-size NIST Standard Reference Material” – Ch. 8 in *Diffraction analysis of the microstructure of materials*, pp. 187-227, Ed. P. Scardi and E.J. Mittemeijer, Springer-Verlag, Berlin, ISBN: 3-540-40519-4, 2004.

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N. Armstrong, M. Leoni, M. Scardi, “Some concerns regarding the Wilkens’ model for dislocation line broadening” – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic, September, 2004.

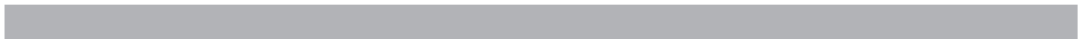
N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, “Status of the NIST Nanocrystalline Size SRM - 1979” – invited presentation at Size-Strain 4: EPDIC 9, Prague, Czech Republic, September, 2004.

N. Armstrong, J. P. Cline, W. Kalceff, and A. Dowd, “Bayesian characterization of nanoparticles from line profile” – presentation at Denver X-Ray Conference, Denver, CO, August, 2004.

N. Armstrong, W. Kalceff, J. P. Cline, J. Bonevich, P. A. Lynch, C. C. Tang, S. A. Thompson, “X-ray diffraction characterization of nanoparticle size and shape distributions: -- Application to bimodal distributions” – Proceedings of the 28th Annual Condensed Matter & Material Meeting, Wagga, Australia, February, 2004.

J. P. Cline and S. T. Mixture, “Alignment & Standards” – workshop at Denver X-Ray Conference, Denver, CO, August, 2003.

D. Windover and J. P. Cline “Goniometer angle calibration for traceability using the method of circle closure” – poster at Denver X-Ray Conference, Denver, CO, August, 2003.



ELECTRON MICROSCOPE TOMOGRAPHY OF ELECTRONIC MATERIALS

GOALS

Enable the use of three-dimensional imaging for thick samples using commercial scanning transmission electron microscopes (STEM). Typical samples include porous low- κ dielectrics, two-layer interconnect samples, and photonic band gap materials.

CUSTOMER NEEDS

The NTRS/ITRS has recognized the need for three-dimensional imaging of interconnects for several years. In this study, our principle objective is to determine the morphology of pores in low- κ dielectric material. Two aspects of the pore distribution are critical: (a) the largest pores may lead to failure of the dielectric (*e.g.*, short circuits), and (b) the connectivity of the pores is important to understand the transport of chemicals during the fabrication of the interconnect.

The potential solutions and major challenges for interconnect are discussed in the 2004 International Technology Roadmap for Semiconductors Update on pages 2 and 17 of the Interconnect Section. Minimization of size effects, 3-D characterization of low- κ void intersection with sidewalls, pore size distribution and barrier roughness are some of the important issues in porous low- κ measurements.

TECHNICAL STRATEGY

1. First, we will upgrade an existing commercial transmission electron microscope to be able to obtain high angle STEM images with a full quantitative understanding of the input and output signals. Noise reduction is also a key issue.

DELIVERABLES: Hardware fabrication for extraction of bright field and dark field STEM detector amplifier chain gain and offset. 2Q 2005

2. In parallel, we will develop theoretical and computational expertise for the understanding of STEM signals associated with multiple scattering of electrons.

DELIVERABLES: 3-D Monte Carlo simulation code in Java and Jython for prediction of energy-dispersive X-ray signals with full 3-D geometrical complexity including electron transport and X-ray absorption effects. 1Q 2005

3. We will obtain a tilt series and perform a tomographic — analysis of a photonic band gap system an artificially periodic polymer structure.

4. We will perform a similar analysis on a low- κ dielectric material.

DELIVERABLES: Code for 3-D Reconstruction with Bayesian Statistics for the Projective Multiple Scattering Regime. 2Q 2005.

Levine (2003) demonstrated by computer simulation that it was possible to reconstruct polymer samples with a thickness well in excess of 1 micrometer if multiple scattering effects were accounted for. In this project, we will generalize the Bayesian tomographic reconstruction algorithm known as the Generalized Gaussian Markov Random Field, introduced by Bouman and Sauer in 1993, to generalize the transmission function from Beer's law to a general function of the integral of a material parameter, *i.e.*, to permit the inclusion of multiple scattering effects. Also, the program will run in 3-D, rather than 2-D in the Bouman-Sauer implementation.

DELIVERABLES: Tomographic study of a low- κ dielectric material. 3Q 2005

The porous low- κ dielectric will pose more of a challenge, particularly for alignment, because of its random nature. Hence, it will be studied second.

ACCOMPLISHMENTS

■ To date, we demonstrated the ability to obtain three-dimensional information using a scanning confocal transmission electron microscope on integrated interconnect samples several micrometers (Frigo, Levine, and Zaluzec, 2002) as well as the ability to obtain three-dimensional information on integrated circuit interconnect samples using a commercial scanning transmission electron microscope (Levine *et al.*, 2003).

■ We performed a 3-D reconstruction of a photonic crystal supplied by Lucent Technologies (see Fig. 1, pg. 152), based on data taken on our in-house STEM.

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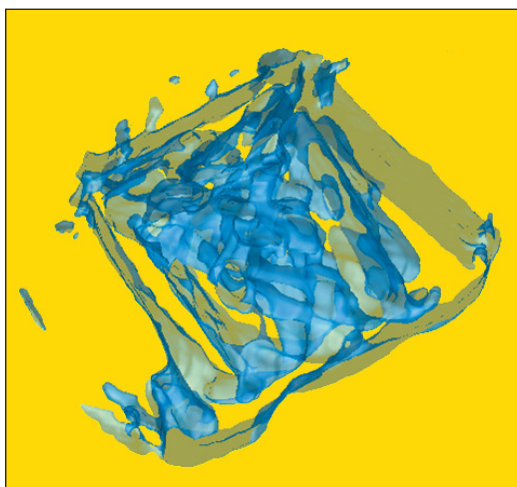


Figure 1. Tomographic reconstruction of a photonic band gap sample. An interconnecting network of material and void is present in the center of the figure. The bands on the outside are from the platinum overlayer added to protect the sample during preparation by a focused ion beam.

■ We simulated the observed STEM scattering and energy-dispersive X-ray signal from a 3-D phantom containing interconnect materials over an angular range of 180 degrees (Fig. 2).

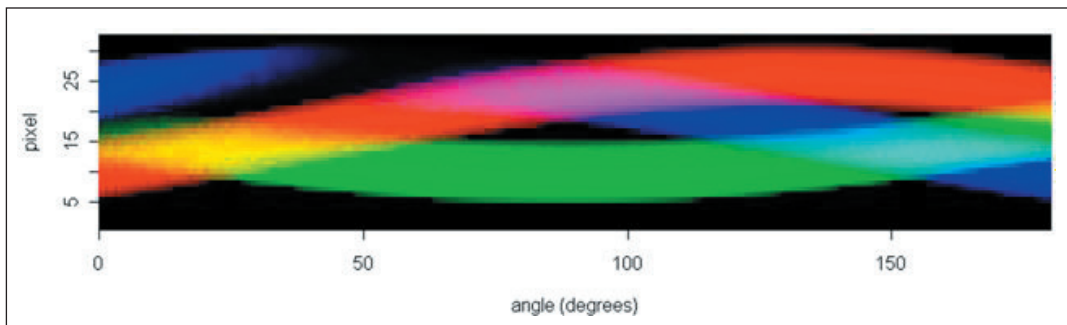


Figure 2. 3-D Java Monte Carlo simulation of interconnect phantoms and observed X-ray emission (Cu=red Al=blue SiO₂=green) from 0 degree to 180 degree tilt.

COLLABORATIONS

International Sematech, Brendan Foran, preparation of low- κ samples, electron microscopy.

Chris Soles and Hae-Jeong Lee, NIST, MSEL, Polymers Division; low- κ samples

Accurel, Inc. Preparation of focused ion beam sections from low- κ samples

Lucent Technologies, Shu Yang; preparation of photonic band gap material.

RECENT PUBLICATIONS

S. Frigo, Z. H. Levine, and N. J. Zaluzec, "Submicron imaging of buried integrated circuit structures using a scanning confocal electron microscope," *Appl. Phys. Lett.* **81**, 2112 (2002).

Z. H. Levine, "Tomography in the Multiple Scattering Regime of the Scanning Transmission Electron Microscope," *Appl. Phys. Lett.* **82**, 3943 (2003).

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HIGH-RESOLUTION MICROCALORIMETER X-RAY SPECTROMETER FOR CHEMICAL ANALYSIS

GOALS

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator.

CUSTOMER NEEDS

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now Analytical Laboratory Managers Council (ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

"Promising new technology such as high-energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMS located in the clean room." **2003 International Technology Roadmap for Semiconductors**

TECHNICAL STRATEGY

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Arrays of X-ray microcalorimeters are being tested, and the development of technologies for large-format arrays is in process. To meet the needs of the semiconductor industry, it is nec-

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essary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg for collaborative use in studying problems of interest to the industry (Fig. 1), and to work with other partners in disseminating the technology.

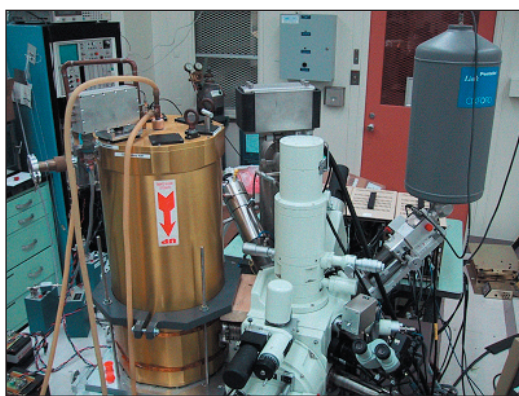


Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Prepare for the eventual transfer of an array microcalorimeter system. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry.

2. Continued improvements in microcalorimeter energy resolution are desirable for the rapid analysis of chemical shifts. However, for many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors) are not as important as an increase in the maximum count rate and collection area. Both the collection area and count rate can be improved by the implementation of multipixel arrays of detectors. Arrays of X-ray microcalorimeters are now being fabricated and tested. The perfor-

mance of these arrays should be similar to that of earlier, successful single pixels.

DELIVERABLES: Achieve high-resolution operation of a close-packed X-ray microcalorimeter array to demonstrate the increase in collection area and count rate achievable with arrays.

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive ^3He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES: Demonstrate the cooling of an electrically-separate piece of thin-film electronics using a tunnel-junction refrigerator that could be coupled to a simple ^3He refrigerator.

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated. The integration of this multiplexer with X-ray microcalorimeters is a crucial step towards the deployment of large sensor arrays. The operation of such an integrated system under X-ray illumination will allow its capabilities to be measured and routes to improvement to be determined.

DELIVERABLES: Demonstrate multiplexed operation of microcalorimeters under X-ray illumination. Characterize multiplexer performance and design next-generation system.

ACCOMPLISHMENTS

■ We fabricated and tested a new generation of microcalorimeters that incorporate additional normal metal regions to suppress internal noise. In addition to being more stable and easier to bias, the energy resolution of these microcalorimeters is significantly improved. We demonstrated a world record energy resolution of 2.4 eV FWHM at 5.9 keV (see Fig. 2).

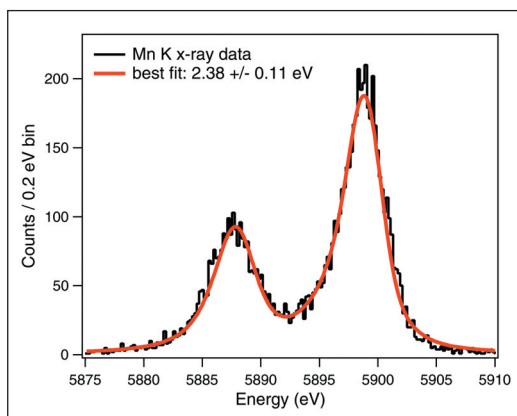


Figure 2. X-ray spectrum from improved NIST microcalorimeter. The FWHM resolution was 2.4 eV for 5.9 keV X-rays.

■ We continue to support the microcalorimeter system installed on a CSTL scanning electron microscope in Gaithersburg, Maryland. We recently upgraded the infrared blocking filters, the magnetic shielding, the pulse acquisition hardware, the detector bias hardware, and the microcalorimeter itself. The new detector is more stable, easier to bias, and has better spectral resolution than the previous unit. We are collaborating with CSTL researchers on further improvements to the stability and ease-of-use of the system.

■ We recently demonstrated the ability to read out eight TES microcalorimeters in a single multiplexed amplifier channel with 3.8 eV FWHM energy resolution (Fig. 3). The detectors were fast, having a signal decay-time constant of about 150 microseconds. Combining this result with closed-form calculations and a new Monte-Carle software package that performs a detailed simulation of our SQUID multiplexer, we can reliably predict the future performance of the multiplexer system. In particular, with only evolutionary improvements to the basic architecture, our time-division SQUID multiplexer will be able to readout 32 detectors per channel with 4 eV resolution or better. Planned improvements include increased open-loop system bandwidth, well-matched pulse rise and fall times, lower SQUID noise, and optimization of the coupling between microcalorimeters and SQUIDs. We are now preparing to demonstrate multiplexed operation of a 3x32 high-resolution microcalorimeter array.

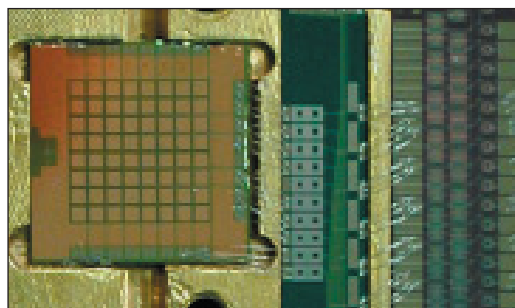


Figure 3. Photograph of an 8x8 array of microcalorimeters. Each microcalorimeter has a 1.5- μm -thick Bi absorber. The middle chip is a filter chip. The chip on the right is a SQUID multiplexer.

■ We have continued work on an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK. If successful, this refrigerator could greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small and inexpensive ^3He systems coupled to the solid-state refrigerator. The device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. We have previously demonstrated refrigerators able to cool themselves from 260 mK to 130 mK with cooling powers well matched to microcalorimeter X-ray sensors. Recently, we demonstrated refrigerators able to cool bulk material as well as electrically separate pieces of thin-film electronics, such as a X-ray microcalorimeter (Fig. 4). The solid-state refrigerator is

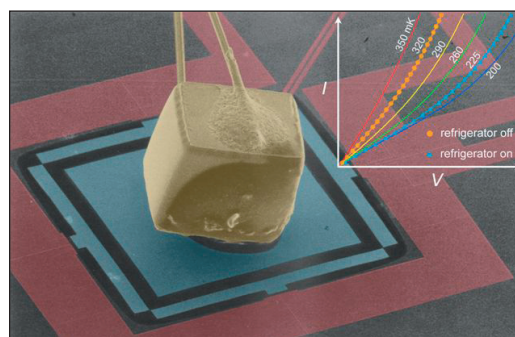


Figure 4. Colorized micrograph of solid-state refrigerator. A cube of germanium (yellow) located on a suspended, micromachined membrane is cooled by four pairs of normal-insulator-superconductor tunnel junctions. The ratio of the volumes of the germanium and the junctions is the same as the ratio of the volumes of the Statue of Liberty and an ordinary person (about 11,000). Macroscopic wires (at upper left) contact the germanium to measure its resistance; these are cooled as well.

fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. We recently cooled a thin-film payload from 320 mK to 225 mK. This work has been featured twice on the cover of *Applied Physics Letters* and once on the cover of *Physics Today*.

■ The NIST microcalorimeter EDS holds the world record for energy resolution for an EDS X-ray detector of 2.0 eV at 1500 eV, which is over 30 times better than the best high resolution semiconductor-based detectors currently available (Fig. 5). This energy resolution was measured using a glass prepared by Dale Newbury of NIST to use as a test standard for EDS.

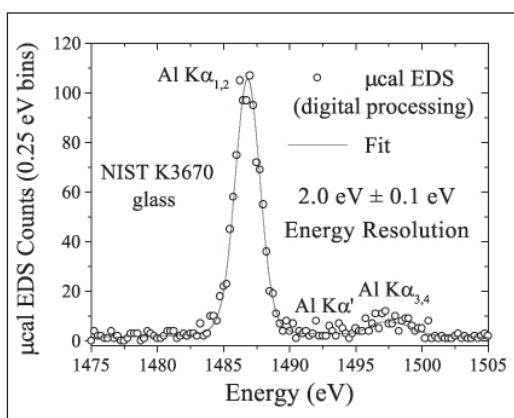


Figure 5. The Al-K α region of a microcalorimeter EDS spectrum of the multielement NIST K3670 glass. The acquired spectrum is shown as well as a weighted least-squares fit of the Al K α and satellite lines convolved with a Gaussian instrument response, yielding an energy resolution of $2.0 \text{ eV} \pm 0.1 \text{ eV FWHM}$.

■ We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 (see Fig. 6). An aluminum film was deposited on part of a sapphire substrate. A microcalorimeter EDS was used to measure the X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about 0.2 eV) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the

data-collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

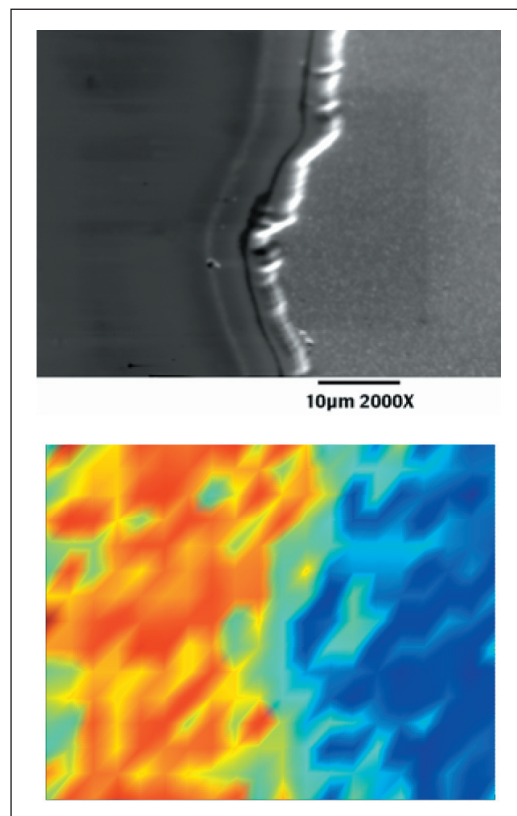


Figure 6. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al K α peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is $\sim 0.2 \text{ eV}$.

COLLABORATIONS

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

RECENT PUBLICATIONS

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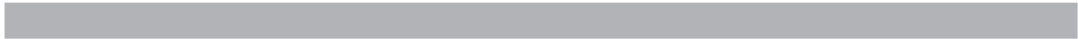
C. D. Reintsema, J. A. Beall, S. Deiker, W. B. Doriese, G. C. Hilton, K. D. Irwin, S.W. Nam, L. R. Vale, J.N. Ullom, Y. Xu, J. Beyer, M. Huber, "A Time-Domain SQUID Multiplexer System for Read-Out of Superconducting Transition-Edge Sensor Arrays," *Ext. Abstracts, 2003 Intl. Superconductive Electronics Conf. (ISEC)*, Jul 07-12, 2003, Sydney, Australia.

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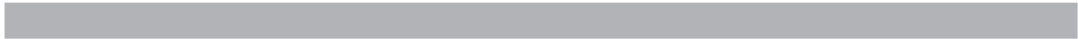
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DEVICE DESIGN AND CHARACTERIZATION PROGRAM

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as FINFETs, fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other exotica such as carbon nanotube and molecular device structures need to be characterized. Another addition to the portfolio is the emerging field of organic materials electronics. To this end we have initiated a new program, “Device Design and Characterization.” One project that has to be highlighted because it will impact all the projects in the portfolio over time is the Advanced Measurements Nanofabrication Facility Support project. With the completion of the Advanced Measurements Laboratory on the Gaithersburg, Maryland campus, we have begun to populate a cleanroom facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.



DEVICE CHARACTERIZATION AND RELIABILITY

GOALS

The goal of the Advanced Device Characterization and Reliability Project is to improve and develop reliability and electrical characterization tools for advanced CMOS technologies. Deliverables include test methods, diagnostic procedures, reliability data, electrical characterization methods, physical models for wear-out, and methodologies to determine energy band diagrams for metal/high- κ systems.

A specific focus is to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (*i.e.*, the gate dielectric, SiO_2 , and the gate electrode, doped polycrystalline Si), which has served the industry for 35 years, must now be entirely replaced with one having a higher capacitance and lower power dissipation. Gate dielectrics having higher dielectric constants than SiO_2 will replace SiO_2 , and metal electrodes will replace polycrystalline silicon. The enormous complexity of selecting the proper combinations of new gate dielectrics and gate metal electrodes can only be attacked using combinatorial materials methodologies. Therefore, we will be implementing this technology.

CUSTOMER NEEDS

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) with effective thickness values of 1.4 nm, or less, being projected in 2004, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 must be replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates or metal silicates.

Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO_2 of this thickness, a high permittivity gate dielectric (*e.g.*, Si_3N_4 , HfSi_xO_y , ZrO_2) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO_2 and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO_2 , very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

TECHNICAL STRATEGY

There are two main focus areas for this project:

- Developing electrical and reliability characterization techniques for ultra-thin SiO_2 and high dielectric constant gate dielectrics.
- Develop combinatorial (fast, local) measurement techniques to measure appropriate electrical properties on gate stacks consisting of new gate dielectric and gate metal electrode materials.

The first focus area is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, threshold voltage V_t instability, defect generation rates and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of

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the characterization schemes will first be developed on the simpler ultra-thin oxide and oxidenitride dielectrics and then be applied to the metal oxide and silicate dielectrics for a variety of high- κ samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

DELIVERABLES: Study of Negative Bias Temperature Instability in HfO_2 transistors under pulsed bias stress. 1Q 2005

DELIVERABLES: Perform CV test methodology for extracting metal/high- κ work function from various high- κ metal gate systems, 2Q 2005

DELIVERABLES: Provide test technique(s) and analysis to quantify electrical trap densities at multiple interface stacks by 3Q 2005.

DELIVERABLES: Compare metal work function measurements with measurements performed with other techniques including internal photo emission and scanning Kelvin probe microscopy on ternary metal systems produced by combinatorial techniques. 3Q 2005

DELIVERABLES: Identify suitable metal gate electrode compositions, based on barrier height and thermal stability criteria, for use with state-of-the-art gate dielectrics (e.g., Hf-Si-O-N). 4Q 2005

ACCOMPLISHMENTS

NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI) STUDIED FOR HfO_2 P-MOSFETS

The contribution of gate oxide bulk traps to NBTI degradation of HfO_2 devices was evaluated and compared with SiO_2 control samples. The ΔV_{th} and oxide trap generation of HfO_2 and SiO_2 devices show a dependence on gate pulse repetition frequency as shown in Fig. 1. Besides interface traps, bulk traps also influence the NBTI degradation of HfO_2 , and this influence is also dependent on the stress conditions. At dc stress conditions, the bulk trap generation is comparable to that of interface traps, and thus plays an important role for the ΔV_{th} , however it becomes negligible at higher pulse repetition frequencies. In addition

to the different frequency response, the bulk trap generation also shows a different temperature dependence than the interface traps. We found that interface traps generation has much higher activation energy than bulk traps, which also explain the different temperature dependences of ΔV_{th} at dc and high frequency stress conditions.

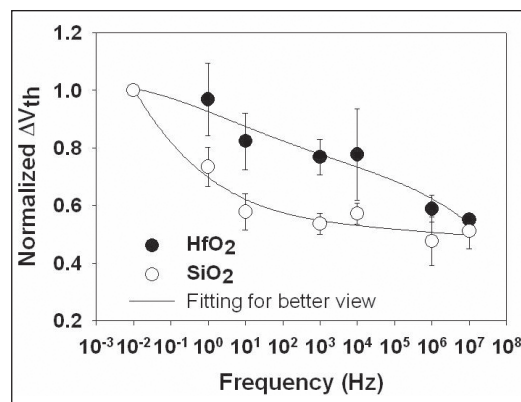


Figure 1. Plot comparing NBTI induced threshold voltage shift versus pulse repetition frequency for SiO_2 and HfO_2 films.

MECHANISTIC STUDY OF PROGRESSIVE BREAKDOWN IN SMALL AREA ULTRA-THIN GATE OXIDES

A study was completed to investigate two competing post soft breakdown modes observed in ultra-thin gate oxides. One breakdown mode features a conducting filament that is stable until hard breakdown occurs and a second mode features a filament that continually degrades with time. Figure 2 shows an example of an unstable breakdown filament. The figure shows the current versus time characteristic for a 2 nm thick gate oxide sample. After dielectric breakdown, the current becomes noisy and eventually increases with time. The acceleration factors are different for each mode, indicating different physical mechanisms are involved in the evolution and formation of the final hard breakdown event. Unstable filaments that result from the first soft breakdown progressively degrade and change physical structure until their leakage current becomes unacceptably large. A set of voltage and temperature acceleration parameters different from oxide wear-out are necessary to project the leakage current with time.

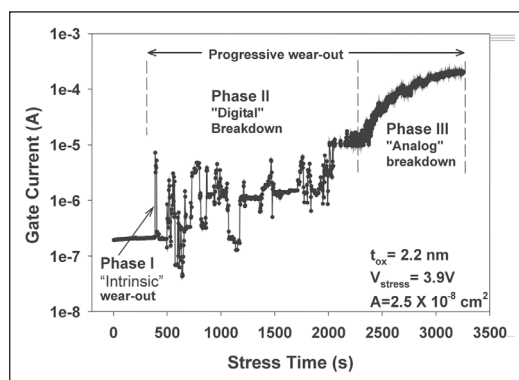


Figure 2. A typical current vs time characteristic for a 2 nm thick gate oxide that has experienced soft breakdown with the formation of non-stable conducting filament.

COMBINATORIAL METHOD FOR STUDYING TERNARY METAL GATE SYSTEMS

Combinatorial methodologies were used to identify, from large candidate metal alloy systems, those alloys that possess the right combination of electrical properties and thermal stability required for metal gate electrodes. The C-V and I-V characteristics of hundreds of capacitors, each with a different metal gate alloy composition, were then automatically measured. A CV simulation program was then used to extract capacitor parameters. Figure 3 shows V_{fb} data, extracted from C-V plots using the simulation program, for Nb-Pt-W alloys deposited on a 6 nm HfO_2 film. Note the distinct variations in V_{fb} that can be discerned as a function of composition in the ternary system.

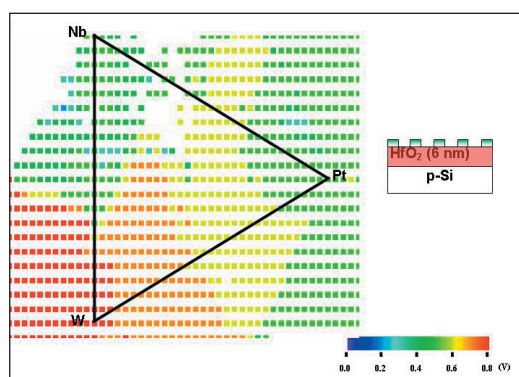


Figure 3. Two dimensional plot showing the variation of CV flatband voltage for a ternary metal system (Nb-Pt-W/ HfO_2) deposited by combinatorial techniques.

MODIFIED CHARGE PUMPING TECHNIQUE TO EXTRACT SPATIAL DISTRIBUTIONS OF TRAPPING CENTERS IN HfO_2/SiO_2 STACKED DIELECTRICS

Analysis methodology for charge pumping (CP) data was developed and applied to extract the spatial depth profile of traps in the SiO_2/HfO_2 gate stacks. This analysis indicates that by changing CP measurement parameters it is possible to probe traps at different depth inside the dielectric as shown in Fig. 4. Spatial profile of traps reveals three separate regions of trap location: in SiO_2 interface, SiO_2/HfO_2 interaction region, and an HfO_2 film.

From the simulation result it has been shown that interface trap density during CP characterization is not equal to the total trap density in high- κ gate stacks. It is also shown that the probable range of traps in the dielectrics is affected by the pulse parameters. These results are essentially important when experimental data from different electrical characterization techniques are compared. By using the proposed analysis, trap spatial profiles in the high- κ gate stacks with different SiO_2 interfacial layer thickness can be studied. The results clearly show the change of trap density from the SiO_2 layer to the SiO_2/HfO_2 interaction region and finally the HfO_2 layer. Although an accurate depth position of traps cannot be determined due to unknown values of certain dielectric parameters, the relative shift of the trap depth profile is consistent with the difference of the interfacial layer thickness in different SiO_2/HfO_2 stacks.

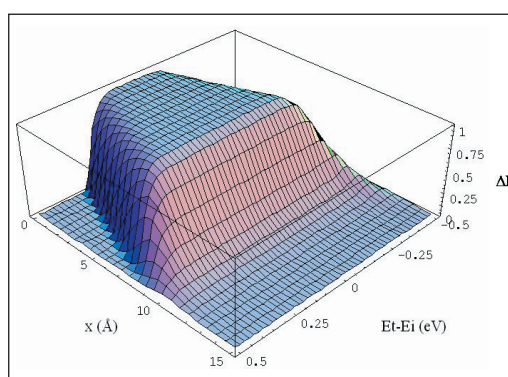


Figure 4. 3-D ΔF contour simulation result. ΔF is equal to one within the trapezoidal plateau that indicates the region having the maximum probability been probed.

STANDARDS COMMITTEE PARTICIPATION

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

COLLABORATIONS

IBM, Alternative Gate Dielectrics

N.C. State University (oxynitrides, nitrides, ultra-thin SiO₂), alternative gate dielectrics

SEMATECH Characterization of metal gate high- κ systems.

Sharp Microelectronics, Characterization of Hafnium-oxide dielectric films

Rutgers University, Characterization of high- κ gate dielectrics

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides

University of Maryland, College Park, ultrathin gate oxide reliability

U. Texas at Austin, Optical properties of ZrO₂ and HfO₂ for use as high- κ gate dielectrics

RECENT PUBLICATIONS

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E. M. Vogel and D. Heh, "Depth profiles of electrically active defects in high- κ gate stacks using charge pumping," *Advanced Gate Stack Engineering working Group Biannual Meeting*, Austin Texas, 2005.

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NANOELECTRONIC DEVICE METROLOGY

GOALS

The overall goal of the Nanoelectronic Device Metrology (NEDM) task is to develop the metrology that will help enable new nanotechnologies (such as Si-based quantum devices, molecular electronics) to supplement and/or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. Two related goals are the optimization of Si-based single-electron devices for one-electron logic, and the development of ultra-sensitive nanotransistor devices to observe charge reconfigurations in biological systems. Another targeted goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably (see Fig. 1).



Figure 1. Curt Richter loads a molecular electronic sample for electrical characterization.

CUSTOMER NEEDS

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) shows no known solutions in the short term for a variety of technological requirements including gate dielectric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to

augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approach are molecular electronics and Si-based quantum electronic devices. Molecular electronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches used in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Alternatively, research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology. Finally, there is a large potential set of customers for ultra-sensitive charge electrometry of biological systems. Many diseases result from changes in protein structure or folding. We will investigate whether such changes can be elucidated through capacitive coupling to nearby nanotransistors.

In all these cases, our project has the capability to offer early guidance to these emerging fields and to assist companies in pursuing productive areas and rejecting problematic ones. Because these fields are not yet mature, as our relatively moderate efforts progress, they can yield large payoffs for the customers.

TECHNICAL STRATEGY

- Develop the electrical and physical metrology of Si-based nanoelectronics. The focus is on the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

DELIVERABLES: Complete systematic investigation of carrier mobility in Si-nanowire FETs nanofabricated from SOI wafers; prepare and submit manuscript.
1Q 2005

Technical Contacts:

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Eric M. Vogel
Neil M. Zimmerman

DELIVERABLES: Report process flow and characterization of prototypical enhancement-mode Si-nanowire FETs based upon Schottky-barrier contacts; prepare and submit manuscript. 3Q 2005

- Develop geometries and architectures that maximize flexibility and operating temperature of single-based single-electron devices.

DELIVERABLES: Complete and publish an experimental and theoretical study comparing charge offset drift in metal-based and Si-based SET transistors and/or the static charge offset problem in Si-based SET transistors. 1Q 2006

- Develop robust molecular test structures in order to use them to measure the electrical properties of molecules. The measured electrical properties will be correlated with systematic characterization studies by a variety of advanced analytical probes and the results used to determine charge conduction mechanisms and in the validation of predictive theoretical models (see Fig. 2 and Fig. 3).

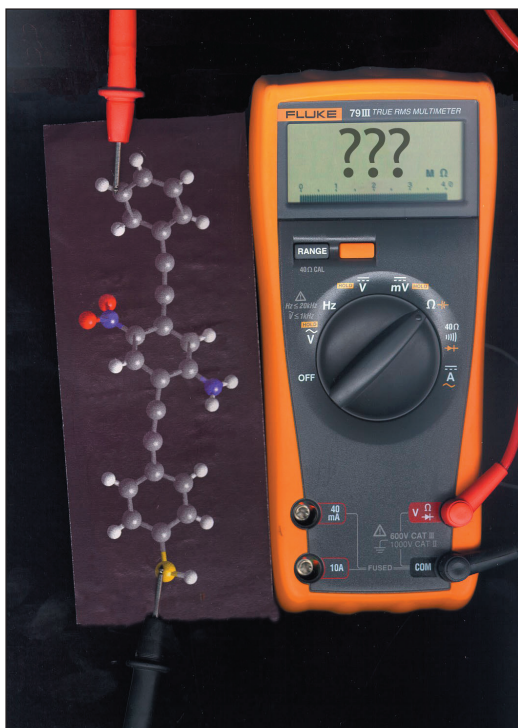


Figure 2. The concept behind molecular electronic test structures.

DELIVERABLES: Develop and demonstrate FTIR-based technique to characterize top-metal/molecular interfaces. Investigate initial metal/molecule interfaces. Prepare and submit manuscript. 3Q 2005

DELIVERABLES: Develop a “nano-gap capacitor” to characterize charge polarization in molecular electronic molecules. 2Q 2006

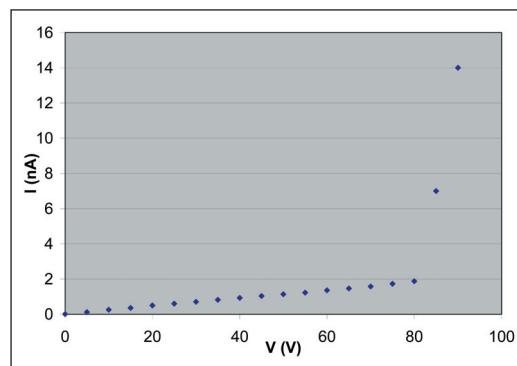


Figure 3. Air breakdown measurement in a capacitor with a gap of $1\ \mu\text{m}$. The gap is deduced from the capacitance value. The sharp increase in current shows the start of air breakdown at about $80\ \text{V}$ across the capacitor. Note that the gap of $1\ \mu\text{m}$ is about equal to the mean free path of electrons in air at room temperature, so that this result does not lie on the standard Paschen curve.

- Determine the ultra-sensitive charge electrometry capabilities of Si-nanotransistors through measuring the sensitivity and its relationship to device structure. A longer term strategy is to assess how the sensitivity is affected by biological structures in solution (see Fig. 4).

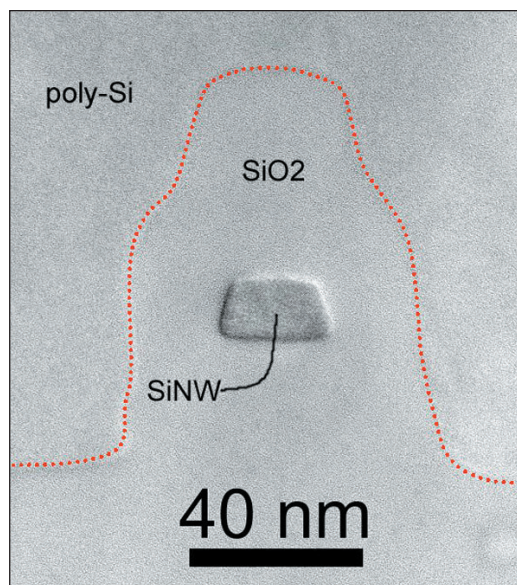


Figure 4. Si nanowire field-effect transistor.

ACCOMPLISHMENTS

- *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated.* Dr. Sang-Mo Koo and colleagues have demonstrated that silicon nanowire (SiNW) field effect transistors (FETs) fabricated by a standard ‘top-

down' approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel ($1000 \text{ cm}^2/\text{Vs}$) is found to be two times higher than that of the reference MOSFET of large dimension ($W > 1 \text{ }\mu\text{m}$). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today's standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors.* We have shown that SiNWs with Schottky contacts can be used as enhancement-mode FETs with an excellent on/off current ratio. The process does not require any source and drain doping or silicide formation, thereby allowing for a simple process without thermal annealing. Silicon nanowire field-effect transistors (SiNWFETs) were fabricated with a highly simplified integration scheme to function as Schottky barrier transistors with excellent enhancement-mode characteristics and a high on/off current ratio $\sim 10^7$. SiNWFETs show significant improvement in the thermal emission leakage ($\sim 6 \times 10^{-13} \text{ A}/\mu\text{m}$) compared to reference FETs with a larger channel width ($\sim 7 \times 10^{-10} \text{ A}/\mu\text{m}$). The drain current level depends substantially on the contact metal work function as determined by examining devices with different source-/drain-contacts of Ti ($\approx 4.33 \text{ eV}$) and Cr ($\approx 4.50 \text{ eV}$). The different conduction mechanisms for accumulation- and inversion-mode operation were determined and confirmed by comparison with two-dimensional numerical simulation results. Schottky barrier FETs are of great interest in their own respect as an alternative to traditional doped source and drain device structure, because sub-100-nm range scaling encounters fundamental problems including high leakage current and parasitic resistance. Schottky barrier FETs have

a number of advantages including simple and low-temperature processing, good suppression of short-channel effects, and the elimination of doping and subsequent activation steps. These features are particularly desirable for SiNW devices because they can circumvent difficult fabrication issues such as an accurate control of the doping type/level and the formation of reliable ohmic contacts (see Fig. 5).

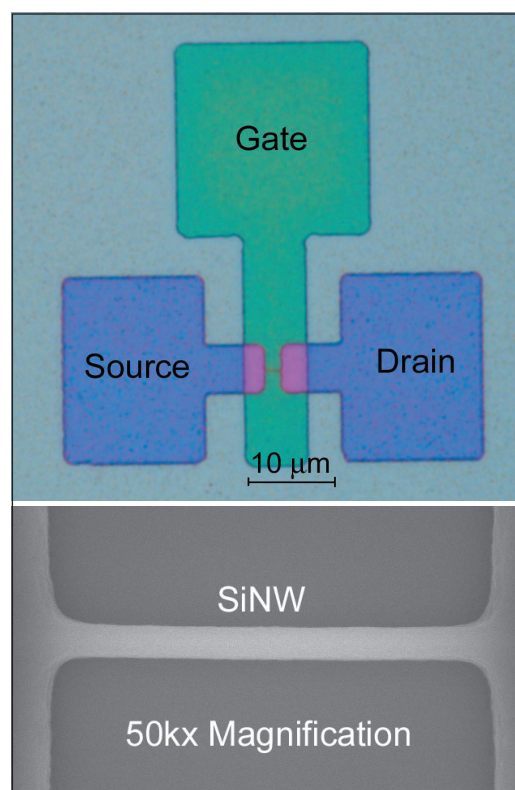


Figure 5. A SiNWFET based upon Schottky-barrier source/drain contacts.

■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements.* Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nanotechnology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental setup. Electrical (current-voltage, or IV) measurements

of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of molecular electronic devices are often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what will may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Novel approach to investigate buried metal-organic interfaces for molecular electronics.* We have developed and used a novel approach to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples as prepared encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance. Two different chemical processes were utilized to attach nm-thick alkane films to the Si substrates: a conventional silanization process for films on thin oxides and a novel process previously optimized at NIST for direct attachment to silicon. Molecules on silicon are of interest as active electronic layers and for surface engineering. Monolayers bound directly to silicon are expected to have less interfacial capacitance than those on oxides, be more amenable to further processing, and be resistant to degradation due to the nature of the strong covalent bond. Results were presented at the 7th International Molecular Electronics conference

and a manuscript was submitted to the journal *Nanoletters*.

FY OUTPUTS

COLLABORATIONS

NTT, Akira Fujiwara, Si-nanowire metrology

Hewlett-Packard, R. Stanley Williams et al., Interface properties of molecular electronic test structures

NIST Divisions 836, 837, 838, Dr. Roger van Zee et al., Molecular Electronics Competence Project

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures

RECENT PUBLICATIONS

Richter, C.A., D.R. Stewart, D.A.A. Ohlberg, R.S. Williams; "Electrical Characterization of Al/AIO_x/Molecule/Ti/Al Devices," *Appl. Phys. A* 2005, 80, 1355–1362. (March 2005)

Hacker, C.A.; Anderson, K.A.; Richter, L.J.; Richter, C.A.; "Comparison of Si-O-C interfacial bonding of alcohols and aldehydes on Si(111) formed from dilute solution with ultraviolet irradiation" *Langmuir* **21**(3), 882-889 (2005).

Koo S.-M., A.-F. Fujiwara, J.-P. Han, E. Vogel, C. Richter, and J. Bonevich, "High Inversion Current in Silicon Nanowire Field Effect Transistors" *Nano Lett.*, Vol. 4, 2107-2111, Nov. 2004.

Richter L. J., C. S. Yang, P. T. Wilson, C. Hacker, R. D. van Zee, J. J. Stapleton, D. L. Allara, J. M. Tour, "Optical Characterization of Oligo(phenylene-ethynylene) Self-Assembled Monolayers on Gold," *J. Phys. Chem. B.*, Vol. 108, No. 33, pp. 12547-12559 (19-AUG-2004).

Hacker C.A., J. D. Batteas, J. C. Garno, M. Marquez, C. A. Richter, L. J. Richter, R. D. van Zee, C. D. Zangmeister, "Structure and Chemical Characterization of Self-Assembled Mono-Fluoro-Substituted Oligo(phenylene-ethynylene) Monolayers on Gold," *Langmuir*, Vol. 20, No. 15, pp. 6195-6205 (22-JUN-2004).

Richter C. A., C. Hacker, L. J. Richter, E. M. Vogel, "Molecular Devices Formed by Direct Monolayer Attachment to Silicon," *Solid State Electronics*, Vol. 48, pp. 1747-1752 (17-JUN-2004).

POWER SEMICONDUCTOR DEVICE METROLOGY

GOALS

The goals of the project are to develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices.

CUSTOMER NEEDS

There are significant technical requirements for more efficient, higher voltage power semiconductor devices. The application needs range from more efficient power supplies for computers and consumer appliances, to electric automobile power converters, to more efficient long distance high voltage power transmission. Rapid technical advances are occurring in the development of new power semiconductor materials and designs to address these needs. With the introduction of these new materials and designs comes new requirements for characterizing the performance and reliability of the fabricated devices.

The most exciting, and potentially revolutionary, development in this area is the rapid progress in the development of wide band-gap semiconductor materials for power semiconductor devices. Wide band-gap semiconductors such as silicon-carbide (SiC) have long been envisioned as the material of choice for next-generation power devices. Recent advances in single crystal SiC and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the introduction of SiC power Schottky diode products in the 400 V to 1200 V range and led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 15 kHz power switching capability.

“In 2004, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: “his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/compact power supplies, and higher efficiency power distribution/transmission systems.”

Several industry and government programs are currently underway to accelerate the development and application insertion of SiC power semiconductor devices. The goal of the DARPA Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE)

is to develop half-bridge modules with 15 kV, 110 A, 20 kHz capability in the next few years. The emergence of HV-HF devices with such capability is expected to revolutionize utility and military power distribution and conversion by extending the use of Pulse Width Modulation (PWM) technology, with its superior efficiency and control capability, to high voltage applications.

The Electric Power Research Institute (EPRI) also identified the benefits of HV-HF semiconductor technology, which include advanced distribution automation using solid-state distribution transformers with significant new functional capabilities and power quality enhancements. In addition, HV-HF power devices are an enabling technology for alternative energy sources and storage systems. The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements.

TECHNICAL STRATEGY

The strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and techniques where suitable ones do not exist for characterizing critical electrical and thermal properties of devices and ICs. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameters to aid in application insertion. NIST is taking a lead role in developing the device metrology and performance metrics necessary for both the DARPA and EPRI efforts and the new industries envisioned by these programs. NIST is also pioneering electrical and thermal measurement methods for HV-HF devices.

[The Project] ... continues to lead industry needs by providing state-of-the-art capability for the measurement of unique power device characteristics at critical operating conditions.”

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

Technical Contact:
A. Hefner

PERFORMANCE, RELIABILITY, AND APPLICATION CHARACTERIZATION FOR DARPA-WBST-HPE DEVICES AND MODULE PACKAGES

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable Solid State Power Substations (SSPS) for future Navy warships. Current distribution approaches being considered for the next generation of aircraft carriers and destroyers employ a 13.8 kV AC power distribution that is stepped down to 450 V AC by using large (6 ton and 10 m³) 2.7 MVA transformers. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing this transformer with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phase 2–3 program for 2005 through 2008.

METROLOGY FOR MAPPING SiC POWER BIPOLAR DEVICE DEGRADATION

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for bipolar structures is an observed degradation in the electrical characteristics over time. The degradation occurs from latent defects such as Basel Plane Dislocations that result in the formation and growth of stacking faults activated by excess carrier recombination. The defects cause severe current nonuniformities to occur, resulting in on-state voltage, switching, and thermal performance degradation.

DELIVERABLE: Develop automated stress and degradation monitoring systems to assess degradation of SiC devices after 10,000 hours of operation. 4Q 2005

DELIVERABLE: Utilize NIST one-of-a-kind high speed thermal image measurements to characterize SiC power diode conduction uniformity performance before and after stress conditions and correlate results with light emission stacking fault measurements (with NRL). 4Q 2005

METROLOGY FOR NONDESTRUCTIVE SWITCHING FAILURE

Power devices undergo their greatest electro-thermal stress under switching conditions. There are

a number of known catastrophic failure mechanisms that occur as a device is switched off with an inductive load. NIST has developed a nondestructive system to test for the failure limits under inductive switching, has done extensive research on Si device failure limits, and will extend that work to include SiC power devices.

DELIVERABLE: Perform unclamped inductive switching measurements for SiC MOSFETs and IGBTs produced by DARPA WBG program. 4Q 2005

CIRCUIT SIMULATOR MODELS FOR SiC POWER SWITCHING DEVICES

Parameter extraction is a critical component in developing and using device models in circuit and system simulations and in establishing performance benchmarks for new device technologies. For new devices, not only must new models be developed, but methods must be modified and new ones developed for extracting the parameters for the models.

DELIVERABLE: Utilize NIST IMPACT model parameter extraction tools to characterize SiC power MOSFETs and IGBTs introduced by the DARPA WBST-HPE program. Provide models for use in simulating SSPS. 4Q 2005

ACCOMPLISHMENTS

- *Extended capabilities of IMPACT parameter extraction software.* The capabilities of the parameter extraction software, *IMPACT*, were extended to include MOSFETs (in addition to IGBTs) and three prototypes of SiC material (in addition to Si). This was done in collaboration with the University of Puerto Rico, Mayaguez, and two SURF (Summer Undergraduate Research Fellow) students.

- *High voltage curve tracer and reverse recovery systems.* The development of a 25 kV variable pulse width curve tracer for both 2 and 3 terminal devices was completed. Safety protection and an interlock system have been tested and qualified. A high voltage reverse recovery test system with 3 kV, 15 A capability was also developed. These systems are critical components in the SiC power semiconductor device metrology tasks.

- *Played a major role in planning and evaluating progress of DARPA Wide Bandgap Power Device program.* Developed the metrology, measured device deliverables to government from DARPA contractors, and used NIST data to provide assessment of program to DARPA director.

- *Initiated new program with EPRI to develop solid state power distribution transformers using ultra high voltage semiconductor devices.* The goal is to replace all existing power distribution transforms with Intelligent Universal Transformers that provide better control of the power grid, provide power factor correction at point of use, improve power quality, and enable plug-and-play insertion of alternate energy sources. NIST aided in mapping existing power semiconductor technologies for this application and in establishing an EPRI road map for development of ultra-high-voltage semiconductor devices.

- *Played a major role in initiating and planning a new DARPA/Navy SiC shipboard power distribution program.* The program involves insertion of power distribution technologies enabled by ultra-high-voltage semiconductor devices into next generation more electric Navel carrier, destroyer, and submarine platforms.

- *Completed development of SiC power MOSFET model and completed development of IMPACT extraction tools for SiC power device model parameter extraction.* Performed parameter extraction for SiC MOSFETs produced by DARPA WBG program and validated simulations.

- A paper with Al Hefner as lead author and including other NIST authors David Berning, Colleen Ellenwood, and Adwoa Akuffo won the William M. Portnoy Award. This paper was presented by David Berning at the IEEE 39th Annual Meeting of the Industry Applications Society in October 2004. The award is issued by the Power Electronics Devices and Components Committee, and is recognition for both the paper and the presentation. The title of the paper is "Characterization of SiC PiN Diode Forward Bias Degradation" by Allen Hefner, Ty McNutt, Adwoa Akuffo, Ranbir Singh, Colleen Ellenwood, Dave Berning, Mrinal Das (CREE), Joseph Sumakeris (CREE), and Robert Stahlbush (NRL).

FY OUTPUTS

COLLABORATIONS

Avanti Inc., Parameter extraction for IGBT library component models

Avanti Inc./University of Arkansas, SiC power device modeling

Avanti Inc./UPRM, Characterization and modeling of electronic packages for thermal model library component models

NIST Division 812, Electronic Materials Characterization Project/Advanced MOS Device Reliability and Characterization Project, Benchmarks for quantum-mechanical device simulation

NIST/CREE, Development of SiC MOSFET electro-thermal model

Participants for DARPA contract (including NRL, ARL, Virginia Tech, CREE, University of Arkansas, Rockwell, etc.), Wide bandgap power device program

Rockwell Science Center/NIST, Development of SiC transistor models

University of Maryland, Metrology for multi-technology System-on-a-Chip (SoC)

Virginia Polytechnic Institute and State University, SiC power device utilization

EXTERNAL RECOGNITION

Allen R. Hefner, elected IEEE Fellow "for contributions to the theory and modeling of power semiconductor devices"

RECENT PUBLICATIONS

Allen Hefner, Ty McNutt, Adwoa Akuffo, Ranbir Singh, Colleen Ellenwood, Dave Berning, Mrinal K. Das, Joseph J. Sumakeris, and Robert Stahlbush, "Characterization of SiC PiN Diode Forward Bias Degradation," Volume: 2, 3-7 Oct. 2004, Pages:1252-1260.

J. Reichl, D. Berning, A. Hefner, and J-S. Lai, "Six-Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation," IEEE Applied Power Electronics Conference, Anaheim, CA, Feb. 2004.

R. Singh, A. R. Hefner Jr., "Reliability of SiC MOS Devices," Journal of Solid-state Electronics, Vol. 48, No. 10-11, pp. 1717-1720 (24-JUNE-2004).

T. R. McNutt, A. R. Hefner Jr., A. Mantooth, J. Duliere, D. W. Berning, R. Singh, "Silicon Carbide PiN and Merged PiN Schottky Power Diode Models Implemented in the Saber Circuit Simulator," IEEE Trans. Power Electronics, Vol. 19, No. 3, pp. 573-581 (01-MAY-2004).

D. W. Berning, J. V. Reichl, A. R. Hefner Jr., M. Hernandez, C. H. Ellenwood, J. Lai, "High Speed IGBT Module Transient Thermal Response Measurements for Model Validation," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 1826-1832 (12-OCT-2003).

X. Huang, P. Elton, J. Lai, A. R. Hefner Jr., D. W. Berning, S. Chen, T. Nehl, "EMI Characterization with Parasitic Modeling for a Permanent Magnet Motor Drive," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, Oct. 12-16, 2003, Salt Lake City, Utah, pp. 416-423 (12-OCT-2003).

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R. Singh, K. G. Irvine, D. C. Capell, J. T. Richmond, D. W. Berning, A. R. Hefner Jr., J. W. Palmour, "Large Area, Ultra-high Voltage 4H-SiC PiN Rectifiers," IEEE Trans. Electron Devices, Vol. 49, No. 12, pp. 2308-2316 (01-DEC-2002).

R. Singh, D. C. Capell, A. R. Hefner Jr., J. Lai, J. W. Palmour, "High-Power 4H-SiC JBS Rectifiers," IEEE Trans. Electron Dev., Vol. 49, No. 11, pp. 2054-2063 (01-NOV.-2002).

J. J. Rodriguez, J. V. Reichl, Z. R. Parrilla, A. R. Hefner Jr., D. W. Berning, M. Velez-Reyes, J. Lai, "Thermal Component Models for Electro-Thermal Analysis of Multichip Power Modules," Proc., 2002 IEEE Industry Application Society, IEEE Industrial Applications Society Meeting, Oct. 13-18, 2002, Pittsburgh, Pennsylvania, pp. 234-241 (24-OCT.-2002).

ORGANIC ELECTRONICS METROLOGY

GOALS

Organic electronic devices are increasingly being incorporated into electronics packaging and are projected to revolutionize integrated circuits through new applications that take advantage of low-cost, high-volume manufacturing, nontraditional substrates, and designed functionality. A critical need exists for new diagnostic probes, tools, and methods to address new technological challenges. Their adoption will be advanced considerably by the development of an integrated and interdisciplinary suite of metrologies to correlate device performance with the structure, properties, and chemistry of critical materials and interfaces. NIST will guide the development of standard test methods and provides the fundamental measurements needed for the rational and directed development of materials and processes to realize the potential of organic electronics.

CUSTOMER NEEDS

An exciting array of new devices and applications are now possible with the development of electronic devices using organic materials because they are amenable to low-cost, high-volume manufacturing, incorporation on flexible substrates, and designed functionality (Fig. 1). Completely new technologies are under development including printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification tags. At this stage, new materials and processes are evolving rapidly to optimize device performance, ease processing limitations, and demonstrate frontier applications. However, systematic progress in organic electronics is challenging because of the enormous range of potential materials (from polymers to nanocomposites) and manufacturing methods (roll-to-roll printing, fluidic self-assembly, micro-contact printing, laser ablative printing, and ink-jet printing).

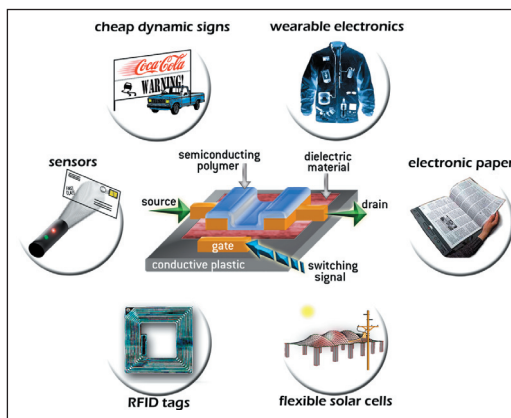


Figure 1. Schematic representation of potential organic electronics applications.

A key technical barrier is the lack of correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. Without this knowledge, guided improvements in materials and processing design are not possible and meaningful standard test protocols cannot be developed. Characterizing the chemically complex (mostly carbon-based) soft interfaces found in organic devices is critical to proper interpretation of charge transport through molecules rather than single crystal structures. Identifying individual contributions to performance variations requires metrology unavailable to device manufacturers and spanning multiple disciplines: device physics, material electronic structure, chemistry, and materials science.

TECHNICAL STRATEGY

The initial focus of the NIST program is on the organic field effect transistor (OFET) because, as in the silicon industry, the transistor is the basic building block for active devices. The fundamental framework, characteristics, and issues that arise during OFET development are transferable to other organic electronic devices because of commonalities in architecture and interfaces. NIST is engaged in complementary activities to address the primary technical barriers facing the adoption of organic electronics: 1) unique measurements of organic materials and interfaces for both a) structure and chemistry and b) electronic properties; and 2) the development of an integrated measurement test platform to correlate device performance with the structure and properties of

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active organic materials. This test platform can also be used to transfer measurement technology to device development laboratories.

1. Interfacial structure and chemistry fundamentals: The basic OFET consists of thin layers (30 nm to 60 nm thick) of disparate materials including the organic semiconductor, dielectric, interconnect, electrode, and substrate. OFET performance and operational stability critically depend upon charge transport and material interactions between inorganic and organic materials, particularly at semiconductor/dielectric and semiconductor/metal interfaces. Detailed interfacial structure information (electronic structure, molecular orientation, interfacial roughness, interfacial chemistry), correlated with electronic properties is required to predict performance.

We are developing a suite of powerful measurement methods including X-ray, neutron, and optical probes capable of *in-situ* nondestructive characterization of critical organic interfaces. Changes in interfacial structure, chemistry, and orientation are correlated with OFET device evaluation. Near-edge X-ray Absorption Fine Structure (NEXAFS) spectroscopy and nonlinear optical techniques are ideally suited for nondestructive characterization of organic interfaces for chemistry, orientation, and structure. NEXAFS can distinguish chemical bonding in the light elements, measure the orientation of interfacial molecules, and separately measure surface versus bulk chemistry simultaneously. Second order nonlinear optical spectroscopies, such as sum frequency generation (SFG), are particularly appropriate for probing the buried semiconductor/dielectric interface. Interfacial structure (width, roughness) between OFET layers must also be measured in order to interpret performance variations. X-ray and neutron reflectometry are powerful thin film characterization methods for determination of the interfacial profile between layers.

DELIVERABLES: Develop measurement protocols and analysis tools to quantify confidence levels in molecular orientation and chemical conversion with NEXAFS spectroscopy. 4Q 2004

DELIVERABLES: NEXAFS measurements of chemical conversion, molecular orientation, and defect density of soluble oligothiophenes with varying number of repeat units. 2Q 2005

DELIVERABLES: Complete FTIR, UV-Vis, and spectroscopic ellipsometer measurements of the structural changes in P3HT films induced by annealing above the melt temperature. 3Q 2005.

DELIVERABLES: Complete NEXAFS measurements of evaporated small molecules onto silicon surfaces as a function of film thickness and deposition temperature. 4Q 2005

2. Electronic property fundamentals: The response of organic electronic materials to electrical fields must also be measured to separate device architecture artifacts and intrinsic material properties. Model sandwich test structures have been designed to individually test the frequency response of semiconducting and dielectric materials employed within organic electronic ensembles. Capacitance and conductance measurements will be performed at frequencies up to 12 GHz to determine the dielectric properties of these materials. These results will be compared with traditional metrics such as current or capacitance versus voltage curves as functions of temperature, layer thickness, or contact metals. With new information (electronic and interfacial), we will elucidate mechanisms underlying the many anomalous phenomena observed in OFETs, such as permanent bias instability and the true nature of carrier mobility distribution, both of which are opaque to traditional metrics.

DELIVERABLES: Construct samples and evaluate feasibility of frequency measurements of P3HT. 1Q 2005

DELIVERABLES: Measure the electrical properties of conductive polymer dispersions such as Poly(3,4-ethylene dioxythiophene) : poly(styrene sulfonic acid) (PEDOT:PSS) as a function of processing. 2Q 2005.

3. Integrated measurement platform: To directly compare OFET performance with its interfacial structure and chemistry, test structures have been fabricated on a single substrate that will include both active devices and pre-defined measurement regions. By employing our methods using these custom platforms, we will identify motifs that develop after processing and during operation that critically affect OFET performance. The use of an integrated substrate removes variations that may affect measurements performed separately. Specific test structures optimized to transfer information to industrial laboratories will be developed. We plan to provide electrical measurement protocols that will identify electronic signatures representative of performance-influencing structural changes and meaningful standard test methods.

DELIVERABLES: Design and fabricate OFET test structures with varying channel lengths and widths. 4Q 2004

DELIVERABLES: Measure field effect hole mobility, threshold voltage, and on/off ratios for P3HT OFETs spin-cast onto the test structure. 2Q 2005

DELIVERABLES: Evaluate correlations between structural measurements and device performance of P3HT films prepared with varying solvents or with varying spin-coating speeds. 4Q 2005

ACCOMPLISHMENTS

■ Near-edge X-ray absorption fine structure (NEXAFS) spectroscopy was applied to several classes of organic electronics materials to investigate the electronic structure, chemistry, and orientation of these molecules near a supporting substrate. In collaboration with the University of California-Berkeley, NEXAFS spectroscopy was used successfully to quantify the simultaneous chemical conversion, molecular ordering (Fig. 2), and defect formation of soluble oligothiophene precursor films for application in organic field

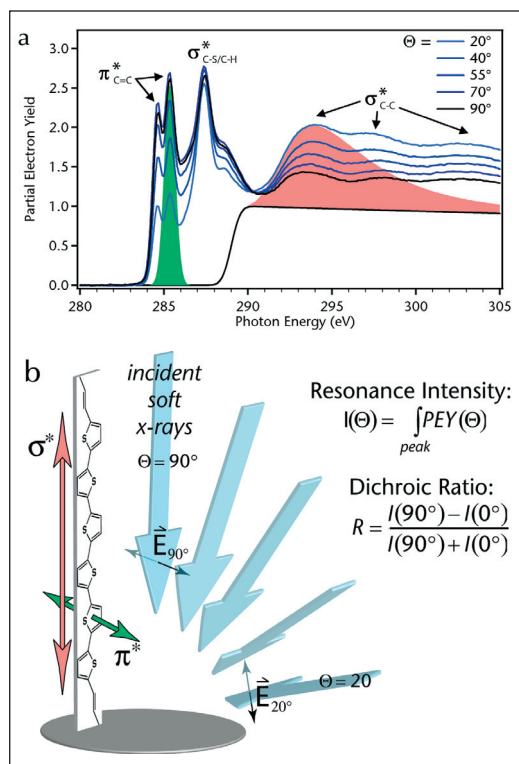


Figure 2. a, NEXAFS carbon K-edge spectra collected at changing incident angles from a film annealed at 200 °C. The green area indicates the oligothiophene π^* resonance used to determine planar orientation while the pink area indicates the σ^* resonance used to determine long axis orientation. b, Image depicting the orientation and spatial orientations of its primary K-edge carbon resonances. Blue arrows indicate incident polarized soft X-rays with electric field vectors extending normal to the plane of photon polarization.

effect transistors. Variations in field-effect hole mobility with thermal processing are directly correlated to the orientation and distribution of molecules within 3 nm to 20 nm thick films.

■ Poly(3,4-ethylene dioxythiophene): poly(styrene sulfonic acid) (PEDOT:PSS) films, a conductive polymeric material, exhibit a complex structure of interconnected conductive PEDOT domains in an insulating PSS matrix that controls its electronic properties. This structure is affected by a water rinse, which removes a large quantity of PSS with negligible PEDOT loss. Upon PSS removal, film thickness is reduced by 35 %, the film DC conductivity is increased by 50 %, and a prominent AC relaxation is eliminated. These results show that the removed PSS is unassociated with the PEDOT and that the interconnected conductive domains are not substantially altered by the removal of a significant fraction of the insulating material. However, the facile removal of acidic PSS may benefit organic light emitting diode fabrication by reducing acid attack on transparent electrodes and lead to more robust performance in switching circuits from the extension of the working frequency range.

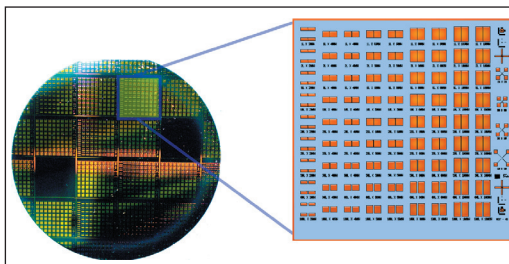


Figure 3. Photo of an organic field effect transistor (OFET) test bed designed and fabricated at NIST. The test bed consists of bottom contact transistors on a silicon dioxide dielectric with a doped silicon wafer as the gate. The structure includes variations in channel length and width as well as large open areas for structural characterization.

■ Organic FET test structures have been designed and fabricated onto silicon wafers with variations in transistor channel length and channel width (Fig. 3). Devices constructed using organic semiconductors such as poly (3-hexyl thiophene) (P3HT) have been tested for their electrical characteristics such as the field effect hole mobility, on/off ratios, and threshold mobilities. Variations in mobility, for example, are observed with changes in processing variables such as annealing temperature and casting solvent. Ongoing studies are focused on correlations between the microstructure of P3HT and device performance.

COLLABORATIONS

Polymers Division, MSEL – C. K. Chiang, Oleksiy Anopchenko, Kenji Kano, Brandon Vogel, Youngsuk Jung, R. Joseph Kline, Bryan D. Vogt, Hae-Jeong Lee, Wen-li Wu

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Stanford University – Mang-mang Ling, Zhenan Bao

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NIST ADVANCED MEASUREMENT LABORATORY

NANOFAB

GOALS

The NIST Advanced Measurement Laboratory (AML) Nanofab will:

- enable fabrication of prototypical nanoscale test structures, measurement instruments, standard reference materials, electronic devices, MEMS, and bio-devices critical to NIST's Strategic Focus Areas (Nanotechnology, Homeland Security, Healthcare) and the Nation's Nanotechnology Needs
- provide access to expensive nanofabrication tools, technologies and expertise in a shared-access, shared-cost environment to NIST and its partners
- foster internal collaboration in Nanotechnology across NIST's Laboratories
- foster external collaboration in Nanotechnology with NIST's partners.

CUSTOMER NEEDS

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in the face of heightened global competition, NIST is constructing one of the most technologically advanced facilities in the world—the Advanced Measurement Laboratory, or AML. The NIST Nanofab (Fig. 1) is one of five buildings in the AML at the Gaithersburg, MD campus. The AML Nanofab will provide researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices.

TECHNICAL STRATEGY

The AML contains two above ground instrument buildings, two completely below ground metrology buildings, and one Class 100 clean room building that will house the NIST AML Nanofab. The AML will provide NIST with superior vibration, temperature and humidity control, and air cleanliness. The NIST AML Nanofab has approximately 1000 m² of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wafers) that will be installed over the upcoming year. This includes

furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, four reactive ion etchers (SF₆/O₂, FI Metal, Cl Metal, Deep), five metal deposition tools (three thermal, one e-beam, one sputterer), contact lithography (front- and back-side alignment), converted SEM e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, etc.). We are also in the process of procuring a state-of-the-art e-beam lithography system with mask making capability, and nanoimprint lithography.

Technical Contacts:

E. M. Vogel
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Figure 1. The NIST AML Nanofab silicon Reactive Ion Etcher.

The NF will be operated as a shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, will be permitted to independently operate the equipment (Fig. 2). The tools will be operated in a manner such that a wide variety of materials can be processed. The facility will be directed by NIST's Semiconductor Electronics Division. Unlike other nanofabs, the NIST AML nanofab is unique in that it is located next to the most advanced metrology tools in the world, and its

focus will be on fabricating nanoscale structures necessary for metrology and standards in support of the semiconductor industry, nanotechnology, biotechnology, and homeland security.



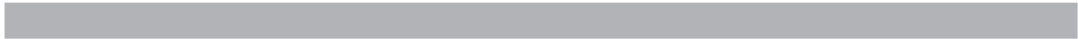
Figure 2. A user in the NIST AML Nanofab.

DELIVERABLES: Facility fully operational by 1Q 2006.

SYSTEM DESIGN AND TEST METROLOGY PROGRAM

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution pose additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.



METROLOGY FOR SYSTEM-ON-A-CHIP (SoC)

GOALS

One of the key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry is the development of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying embedded-sensor (ES) virtual-components (VCs) compatible with the System-on-a-Chip (SoC) integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC CAD libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, low-cost, smart homeland security and environmental sensor systems. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based (MicroElectroMechanical System) VCs into SoCs.

The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards, verification standards and high-level models of system components. The NIST MEMS-based integrated gas-sensing VC is used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies is used to facilitate the adoption of these MT-VCs into new Homeland Security and Industrial applications.

CUSTOMER NEEDS

Recent advances in high density CMOS integration and the ability to co-integrate MEMS-based sensor devices enables cost effective complex system designs fabricated on a single chip. The need for standards arises when the system-on-a-chip is designed using IP (Intellectual Property) cores from multiple vendors. These cores must be compatible for design success, thus demanding standards in the area of interoperable interfaces, models and verification strategies for multi-technology SoC designs.

The SoC design challenges include managing increasing system complexity, achieving system-level verification, and bridging the separate disciplines of system architecture and chip design. These challenges are being overcome with the use of platform-based design approaches that emphasize design reuse, i.e. the development of ES-VCs that can be used as cost-effective building blocks for SoC devices, and standards for ES-VC IP interoperability with the SoC design flow.

The direct customers for this infrastructure building will be the makers of system design software, ES-SoC IP designers, SoC manufacturers and systems designers. This is generally recognized by the chip designers, manufacturers, and EDA tool developers:

"What is the most recent development that promises to truly enable a system on a chip? It is the ability to combine CMOS and MEMS structures into one process flow."

Randy Frank and Dave Zehrbach, Motorola, in *Sensors Online*, 1998

"Definitely, System-on-a-chip is the driving paradigm in our space, and there are some fundamental differences in culture and engineering mentality as well as some new technical skills that need to be developed in engineering. At the highest level, system-on-a-chip implies that you need to think like a system designer but implement like a chip designer, and those traditionally have been different disciplines..."

Shane Robison, Executive Vice President of Engineering, Cadence Design Systems, Inc. EDAcade.com

TECHNICAL STRATEGY

1. To successfully develop ES-VCs for SoC design methodology, the first step in this multi-step process is to develop the ability to make the ES-VC devices via a standard CMOS compatible process. To exercise this capability we have chosen a MEMS microhotplate based embedded gas-sensor, including operational amplifiers, decoders, and an analog-to-digital converter (ADC) to process the data.
2. The second step is to make ES-VCs compatible with the standard digital SoC design methodology. This approach will require ES-VC to

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"... SoC is the driver for convergence of multiple technologies not only in the same system package but also potentially in the same manufacturing process."

The International Technology Roadmap for Semiconductors, 2003.

incorporate digital interface circuitry and to have the DFT/BIST (Design For Test/ Built-In Self Test) functionality required by SoC standards. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas-sensor VC described above.

DELIVERABLES: Develop methodologies for designing digital interface shell functionality for ES-VCs and demonstrate their viability via our microhotplate gas-sensor technology. 4Q 2005

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level models (in SystemC/HDL) exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs is at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital Hardware Description Languages and higher-level system description languages such as SystemC. We are also developing methodologies to validate these models. The digital systems industry has standards set by organizations such as OCP-IP, VSIA and OSCI to foster large-scale interchange and interoperability of modular digital IP, and we believe that such standards in ES-VC field are a key factor for the growth of an ES-VC IP industry.

DELIVERABLES: Develop high-level models for microhotplate gas-sensor ES-VCs to facilitate the development of standards for multi-technology SoC top-down design. 2Q 2006

4. Synthesis process is well defined for the digital SoC design and is well supported by a large number of design libraries. Currently the libraries, methodology, and standards for ES_VC synthesis do not exist. We are developing standards and metrologies for ES-VCs that will be compatible with standard digital synthesis tools.

DELIVERABLES: Develop methodology and standards to allow ES-VC to be synthesized by standard MT- synthesis tools and demonstrate their viability via our microhotplate gas-sensor VC. 4Q 2007

5. Scaling digital circuitry is a key capability used by digital designers to reduce costs and ensure compatibility with different fabrication technologies. Since most systems that would use ES-VCs will be predominantly digital, it is important that there be an equivalent scaling ca-

pability for the ES-VCs. To address the need for scaling ES-VCs, we are developing metrologies for digital-compatible scaling processes.

DELIVERABLES: Develop methodologies and standards for an equivalent ES-VC scaling approach and demonstrate its viability via our microhotplate gas-sensor technology. 4Q 2006

6. The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ES-VCs and interface with them via the digital shell.

DELIVERABLES: Develop methodologies for built-in self test of ES-VC devices and demonstrate their viability via our microhotplate gas-sensor technology. 2Q 2007

NIST is a natural home for this work because NIST has advanced measurement capabilities across the spectrum of sensor technologies.

ACCOMPLISHMENTS

■ A monolithic micro-gas-sensor system was successfully designed and fabricated in a standard 1.5 μm CMOS process. The gas-sensor system incorporated an array of four microhotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. Digital decoders selected individual elements of the sensor array and an operational amplifier monitored sensing film conductance. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represented an improvement in sensitivity of two orders of magnitude over existing MEMS-based microhotplate gas-sensors (see Fig. 1).

■ Investigated existing and emerging SoC design methodologies, and adapted digital SoC design tool-flow to enable integration of mixed-signal MEMS VCs.

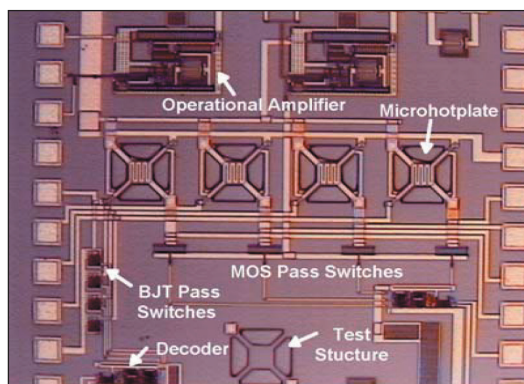


Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

■ A four element gas-sensor VC was successfully designed, fabricated and electrically characterized to demonstrate that the design approach was compatible with SoC design methodology. The performance of the 8-bit ADC exceeded the gas-sensor VC design requirements (see Fig. 2).

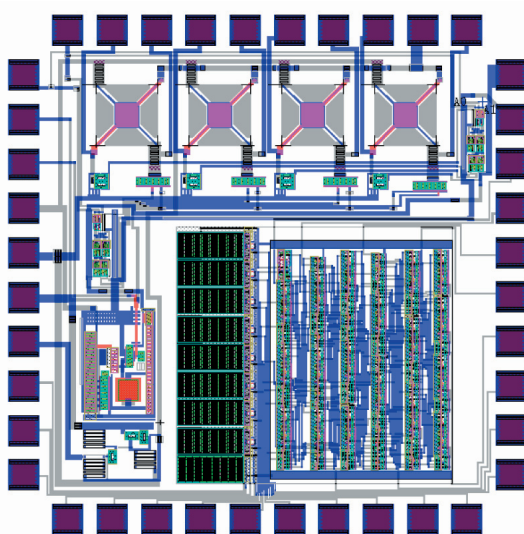


Figure 2. Layout of the four element gas-sensor VC with analog-to-digital control.

■ Electrostatic discharge (ESD) protection structures were added to the gas-sensor and successfully tested. These ESD test structures are based on multi-finger thyristor-type devices and are designed to achieve optimum performance and reduced area (see Fig. 3).

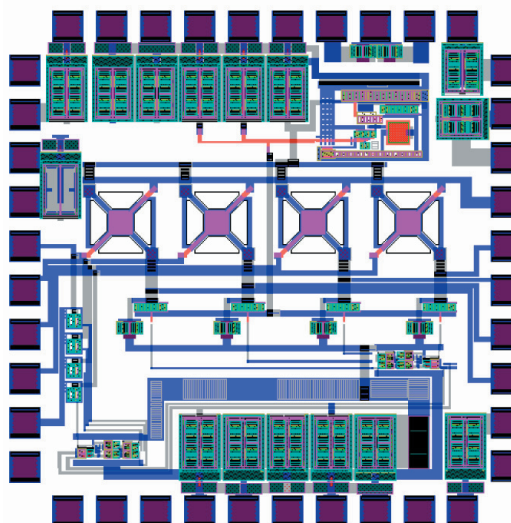


Figure 3. Layout of the four element gas-sensor VC with electrostatic discharge (ESD) protection circuitry.

■ A new post-process etching technique was developed to integrate MEMS devices with standard submicron CMOS processes and a new microhotplate design that scales with standard CMOS structures and voltage levels. This will enable co-integration of MEMS sensor devices with high density submicron digital systems using cost effective standard CMOS foundries. The submicron gas-sensor test chip was characterized. Characterization data showed the new scalable microhotplate will provide the temperature required for gas-sensor operation at 3.3 V (see Fig. 4).

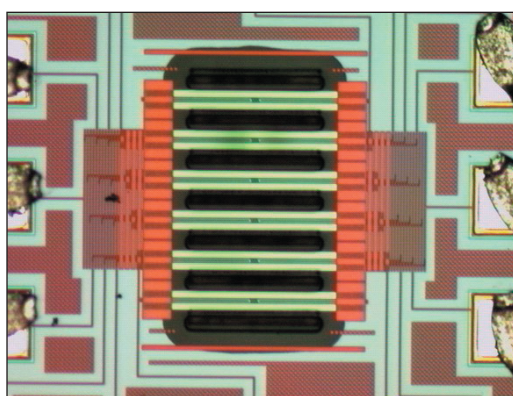


Figure 4. New microhotplate design implemented in standard submicron CMOS technology.

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BIOELECTRONICS METROLOGY

GOALS

There is rapidly growing interest in the application of microelectronics and integrated circuit-based fabrication methods to manipulate and monitor biological processes. This emerging field of bioelectronics will require new competencies in the NIST laboratories to support metrology and standardization. Our goal over the next five years is to develop an internal competency in this field and to establish links with industrial partners in order to position NIST to coordinate the development of a bioelectronics metrology roadmap. Towards this end, we are developing a versatile bioelectronic platform with integrated electronic and microfluidic components that will enable a broad range of quantitative cellular assays, ultimately at the single-cell level. We will characterize the performance of the platform and then use it to study neural (retinal) single-cell response to various toxins. These measurement methods will also facilitate fundamental understanding of the behavior of heterogeneous cell populations and cellular interactions, and will enhance NIST's capabilities to address emerging measurement needs for the medical and pharmaceutical industries. This effort will result in new metrology tools and test methods to support growing commercial industries that use high throughput methods for determining drug efficacy and toxicity.

CUSTOMER NEEDS

Cell-based assays are a primary tool used by the pharmaceutical industry to measure therapeutic drug efficacy and cytotoxicity. These time-consuming and labor-intensive assays currently involve millions of cells in each culture reservoir. This leads to some inherent measurement biases since the collective response only represents the average for the whole population and, for example, cells at different stages of development will respond differently to stimuli. A true paradigm shift is to utilize micro- and nanofabrication technologies to perform these experiments on single cells or small cell clusters in continuous flow microfluidic systems with integrated microsensors and MEMS. Single-cell assays will isolate the parameters affecting cell response and allow the various subpopulations present in bulk cultures to be distinguished. Single-cell assays, when multiplexed, will allow for more rapid identification of drugs and drug targets.

TECHNICAL STRATEGY

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, in varied buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronic, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and to deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electromagnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We will focus our initial research efforts on the study of retinal (neuronal) cells and will later progress to other cell systems.

DELIVERABLES:

Develop an array of micro-electrochemical cells and methods to pattern cells on the array for single-cell electrochemical measurements.

Technical Contacts:

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J. J. Kasianowicz
D. R. Reyes
B. J. Polk

A cellular microenvironment for sustained single cell growth and development;

Microfluidic and microelectronic components on a single platform for delivering precise chemical stimuli to single cells;

Demonstrate the capability to manipulate and stimulate cells within the microenvironment using fluidic, electronic and optical techniques;

New methods for temperature regulation and electronic detection using microwave technologies;

Continuous monitoring of cell growth, development and viability in the presence and absence of therapeutic drugs and chemical toxins.

ACCOMPLISHMENTS

■ We developed a method to adhere retinal cells on micropatterned polyelectrolyte multilayer (PEM) lines adsorbed on poly(dimethylsiloxane) (PDMS) surfaces using microfluidic networks. PEMs were patterned on flat, oxidized PDMS surfaces by sequentially flowing polyions through a microchannel network that was placed in contact with the PDMS surface. Polyethyleneimine (PEI) and poly(allylamine hydrochloride) (PAH) were the polyions used as the top layer cellular adhesion material. The microfluidic network was lifted off after the patterning was completed and retinal cells were seeded on the PEM/PDMS surfaces. The traditional practice of using blocking agents to prevent the adhesion of cells on unpatterned areas was avoided by allowing the PDMS surface to return to its uncharged state after the patterning was completed. The adhesion of rat retinal cells on the patterned PEMs was observed 5 hours after seeding. Cell viability and morphology on the patterned PEMs were assayed. These materials proved to be nontoxic to the cells used in this study regardless of the number of stacked PEM layers. Phalloidin staining of the cytoskeleton revealed no apparent morphological differences in retinal

cells compared with those plated on polystyrene or the larger regions of PEI and PAH; however, cells were relatively more elongated when cultured on the PEM lines. Cell-to-cell communication between cells on adjacent PEM lines was observed as interconnecting tubes containing actin that were a few hundred nanometers in diameter and up to 55 μm in length. This approach provides a simple, fast, and inexpensive method of patterning cells onto micrometer-scale features.

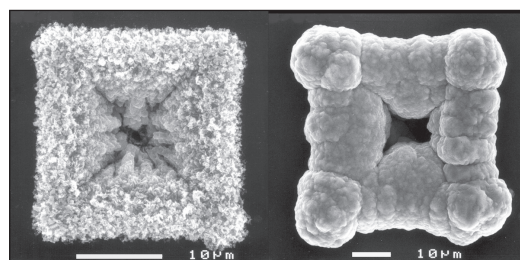


Figure 2. SEM images of two silver nanopores formed by electroplating on micromachined silicon micropores.

■ We developed a method to create nanofluidic restrictions by electroplating silver on micrometer scale pores. Electrodeposition of silver was investigated as a fabrication tool for constricting large ($10^3 \mu\text{m}^2$) vias in silicon substrates while leaving a small opening in the center of the via. Silver reduction from ammoniacal silver nitrate was studied at electrodes of novel geometry (*i.e.*, the edge of the vias) with respect to reduction potential, reduction pulse type, and pulse duration. A variety of crystal nucleation and growth patterns was observed and characterized by scanning electron microscopy. It was found that electroplated silver occluded the vias to leave open areas of less than $1 \mu\text{m}^2$. Such occlusions might be used as restrictions in microfluidics systems, forming a type of solid-state micropore or nanopore.

■ A method for fabricating Ag/AgCl planar microelectrodes for microfluidic applications is presented. Micro-reference electrodes enable accurate potentiometric measurements with miniaturized chemical sensors, but such electrodes often exhibit very limited lifetimes. Our goal is to construct Ag/AgCl microelectrodes reliably with improved potential stability that are compatible with surface mounted microfluidic channels. Electrodes

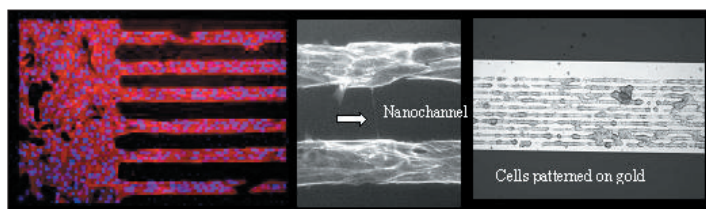


Figure 1. The left and center panels are images of R28 cells retinal patterned using polyelectrolyte multilayers lines adsorbed on poly(dimethylsiloxane). The center panel shows a nanochannel that was spontaneously formed by the cells. The right panel is an image of cells patterned on a gold surface using the polyelectrolyte multilayers.

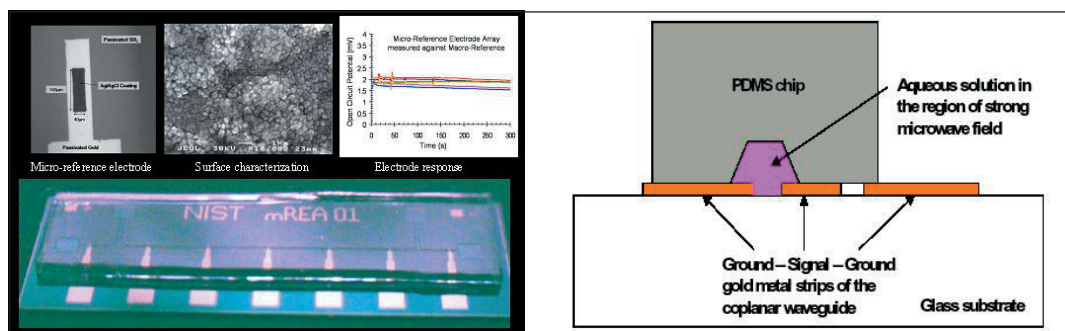


Figure 3. Photographs (left panel) of the NIST micro reference electrode array (mREA) and close-up photo of an Ag/AgCl planar microelectrode, surface, and test. The right panel is a drawing of a fluidic microwave heating assembly showing a gold coplanar transmission line patterned on glass with a poly(dimethylsiloxane) microchannel bonded over it.

with geometric surface areas greater than or equal to 100 square micrometers were fabricated individually and in an array format by electroplating silver, greater than one micrometer thickness, onto photolithographically patterned thin-film metal electrodes. The surface of the electroplated silver was chemically oxidized to silver chloride to form Ag/AgCl microreference electrodes. Characterization results showed that Ag/AgCl microelectrodes produced by this fabrication method exhibit increased stability compared with many devices previously reported. Electrochemical impedance spectroscopy allowed device specific parameters to be extracted from an equivalent circuit model, and these parameters were used to describe the performance of the microelectrodes in a microfluidic channel. Thus, stable Ag/AgCl microelectrodes, fabricated with a combination of photolithographic techniques and electroplating, were demonstrated to have utility for electrochemical analysis within microfluidic systems.

■ Rapid temperature cycling of fluids is essential for increasing the throughput of chemical and biochemical processes and chemical synthesis such as polymerase chain reaction (PCR). In micro total analysis systems (μ TAS), temperature cycling is typically implemented by external heating blocks or by integrated microresistive heating elements (microreactors). In this paper, a new approach for temperature cycling of microfluidic systems is presented that is based on delivering microwave heating energy using a microwave transmission line. A microwave coplanar waveguide is integrated with a surface mounted elastomeric microfluidic channel. We demonstrate that the microwave signal can be tuned to most effectively deliver the heat to the fluid at a frequency of 18 GHz (in agreement with theory) independent of the ionic strength of the

solution. This approach will have application to microwave assisted chemistries which have recently been shown (in macro-scale devices) to have several advantages over conventional resistive heating approaches. These advantages include the ability to deliver heat directly to the fluid (and not to the surrounding medium), requiring lower temperatures to implement a chemical reaction and exhibition of more uniform heating profiles. This paper suggests that those advantages can also be realized in a microfluidic format.

■ We have integrated electrodes within microfluidic devices to carry out AC dielectrophoresis. In this trapping technique, electric fields polarize cells inducing electrostatic forces, which trap the cells against the electrode edges. We have been able to trap cells suspended from bulk cultures within microchannels when flowed past integrated, energized electrodes. We have observed that more than 85 % of cells passing the electrodes were trapped. On the other hand, when electrodes were deactivated, about 70 % of the cells were subsequently detached by solution flow. Deposition of PEMs on the electrodes renders an adhesion layer to further cell attachment. Trapping experiments carried out after PEMs were deposited over the electrodes showed that all immobilized cells remained adherent after the electrodes were deactivated. We have been using AC dielectrophoresis to array cells within a microfluidic channel perpendicular to flow.

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AT-SPEED TEST OF DIGITAL INTEGRATED CIRCUITS

GOALS

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop scanning probe microscopes (SPMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry.

CUSTOMER NEEDS

In the device debug and characterization world, at-speed functional and analog test will continue to serve as a primary vehicle for root cause of design process errors and marginalities (2003 ITRS Test and Test Equipment Section, page 1). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, non-contact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

The need for noninvasive waveform measurements in silicon integrated circuits is discussed in the Test and Test Equipment section, pages 1-5, 2001 (International Technology Roadmap for Semiconductors).

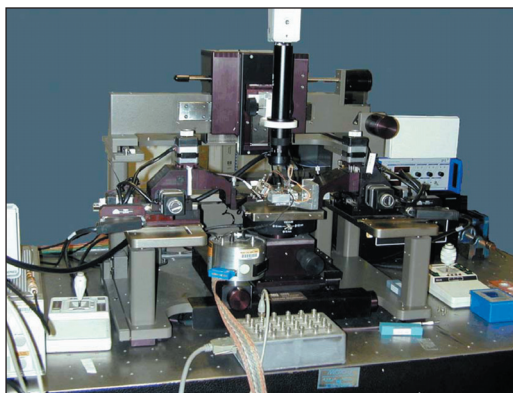


Figure 1. Universal test bed for electric and magnetic field probing on a nanoscale.

TECHNICAL STRATEGY

We will develop calibration artifacts with precisely known high-frequency voltages and circuits suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we are constructing a universal SPM test bed for these probes (Fig. 1). We will then apply our characterization procedures to miniature SPM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we will tie our metrology back to fully characterized electro-optic sampling measurements.

NIST also is working on methods for calibrating and correcting imperfections in waveform measurement equipment that cause distorted or blurred measurements. These effects include instrument response, impedance mismatch, multiple reflections, dispersion, time-base distortion, jitter, and drift. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. For example, Fig. 2 shows measurement of a short bit sequence, transmitted at 10 Gbit/s, and plotted in the form of an eye pattern. Before correction for time-base distortion and jitter (caused by the

Technical Contacts:

D. F. Williams
J. Moreland
P. Kabos
J. Kopanski
P. Hale

“As electronic devices shrink into the nano-meter size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before.”

Travis M. Eiles, Ph.D.
Intel Corp.

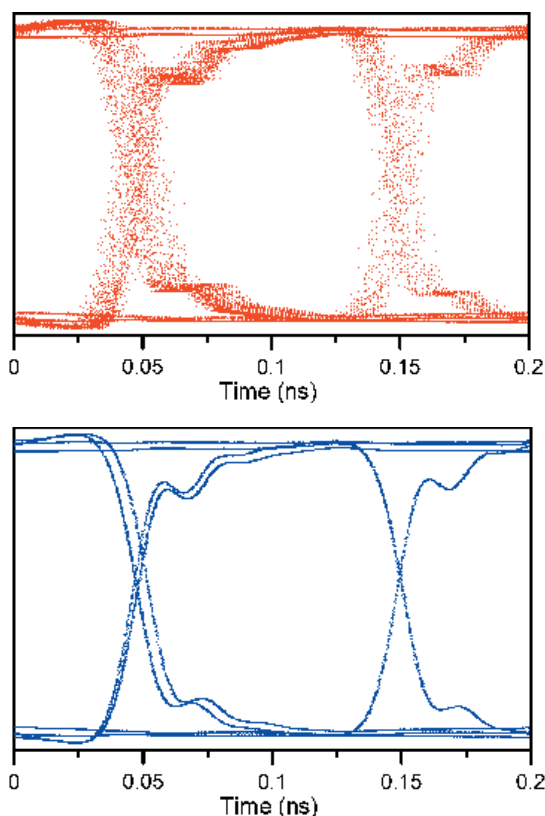


Figure 2. Measurement of 10 Gbit/s eye pattern before (a) and after (b) correction for oscilloscope time-base distortion and jitter using NIST developed techniques.

oscilloscope) the eye pattern is blurred while after correction fine features in the eye pattern, such as pattern-dependant jitter, are clearly revealed. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system.

DELIVERABLE: Test high-impedance probe with single-step 200 GHz EOS calibration. 2Q 2005

DELIVERABLE: Mismatch corrected photodiode impulse response calibration, traceable to the EOS at the 1.00 mm coax plane with covariance matrix that enables point by point time- and frequency-domain uncertainty analysis. 3Q 2005

DELIVERABLE: Measure the magneto-mechanical response of sensors integrated with fiber optic cantilever probe. 4Q 2005

ACCOMPLISHMENTS

- We have designed and tested a prototype sinusoidal waveform standard.
- We have constructed a high-speed electro-optic sampling system.

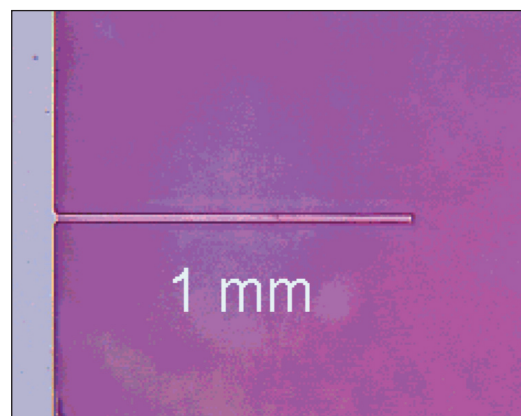


Figure 3. A 1 mm long dielectric bimaterial cantilever AFM probe fabricated at NIST for noninvasively measuring local microwave power.

- We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power (see Fig. 3).
- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements (see Fig. 4).
- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.
- We have constructed an SPM universal test bed.
- We have demonstrated a calibrated measurement of an on-wafer pulsed waveform up to 200 GHz using electro-optic sampling.

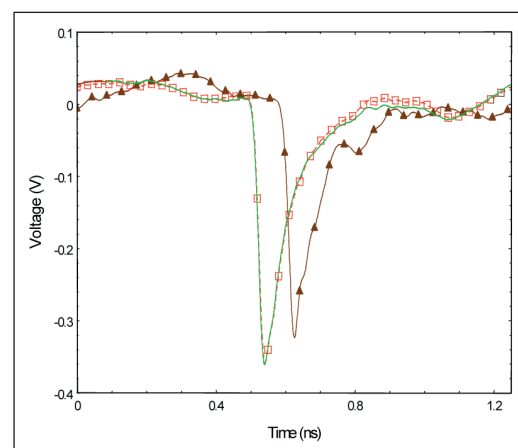


Figure 4. Waveform comparison at the tip of a commercial high-impedance probe. The red curve marked with red squares is the expected waveform. The brown curve marked with triangles is the measured waveform. The green curve is the measured waveform after correction by the new NIST algorithm.

■ We have demonstrated a method for correcting oscilloscope timebase jitter, drift, and distortion.

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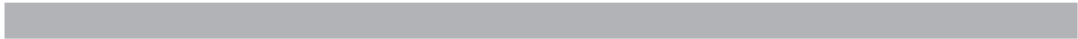
D.F. Williams, P.D. Hale, T.S. Clement, and J.M. Morgan, "Calibrated 200 GHz Waveform Measurement," IEEE Trans. Microwave Theory and Tech., April, 2005.

P. Kabos, H. C. Reader, U. Arz, and D. F. Williams, "Calibrated waveform measurement with high-impedance probes," IEEE Trans. Microwave Theory and Tech., February 2003.

M. D. Janezic, D. F. Williams, V. Blaschke, A. Karamcheti, and C. S. Chang, "Permittivity characterization of low- κ thin films from transmission-line measurements," IEEE Trans. Microwave Theory and Tech. January 2003.

T. S. Clement, P. D. Hale, D. F. Williams, and J. M. Morgan, "Calibrating photoreceiver response to 110 GHz," 15th Annual Meeting of the IEEE Lasers and Electro-Optics Society Conference Digest, Nov. 10-14, 2002, Glasgow, Scotland.

Albrecht Jander, John Moreland, and Pavel Kabos, "Dielectric micromachined calorimeter probe for high resolution microwave power measurements based on ferromagnetic resonance," 15th IEEE Int. Conf. on MicroElectroMechanical Systems, Jan. 20-24, 2002, Las Vegas, Nevada.



THERMAL MEASUREMENTS AND PACKAGING RELIABILITY

GOALS

Provide the microelectronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens that present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal—providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allow us to refine the techniques to make them optimally beneficial to industry, and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, which is essential for technology transfer.

Overcoming thermal limitations has recently become a major issue in CMOS-based microelectronic circuits because: (1) power levels in CPUs have reached the same levels as in power devices; (2) power density nonuniformities are leading to hot spots in microprocessors as well as power ICs; (3) new materials with different thermal properties are being introduced; (4) many new and future technologies (*e.g.*, SOI, 3-D integration) tend to isolate power dissipating elements thermally; and (5) shrinking dimensions and increasing frequency of ICs are causing significant power dissipation in the interconnects. To address these issues, reliable methods for measuring the temperature distribution in ICs and power devices are required.

A broad range of temperature measurement techniques are investigated by this project and several unique temperature measurement system requirements have been identified and demonstrated by NIST. High speed transient thermal imaging methods are being developed for measuring localized heating effects at the semiconductor chip surface. This enables the measurement of transient heating events such as burst operation of IC Functional Unit Blocks (FUBs)

and enables the measurement of transient current constriction failure events in RF and high power devices. Additionally, methods are being developed to evaluate the heat transfer across package layer interfaces using high-speed temperature sensitive parameter (TSP) measurements. This is important for in-situ measurement of heat transfer performance degradation after various levels of thermal stress such as thermal cycling and thermal shock.

CUSTOMER NEEDS

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of thermal responses that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry.

The need to measure operating temperature of a semiconductor device can be divided into the following four broad categories: 1) predicting reliability or operating life of device, 2) measuring material/device thermal properties *in-situ*, 3) confirming or determining the operating limits or thermal performance of a device, and 4) validating thermal models for device, chip and system performance. Thermal measurements on small, <10 μm structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces, such as those seen at solder/intermetallic interfaces and Direct Bonded Copper (DBC) isolation layer is needed for modeling of future package designs.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to “Moore’s Law.” Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate

Technical Contacts:

A. J. Slifka
A. R. Hefner

“I am writing to let you know that NIST has been of great assistance to Cenymer Corporation, one of our portfolio companies. This portfolio company has developed a novel material. Dr. Andrew Slifka at NIST was able to provide the company with thermal measurements that are critically important to Cenymer as it approaches potential customers. It is great to have NIST in the community as a resource to companies like Cenymer.”

*Tim Connor
Sequel Venture Partners*

and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

Measurement of localized and transient heating is also becoming increasingly important in high performance ICs as it is becoming prohibitive to remove the heat that would be dissipated if the entire IC was operated continuously at the full power density level. System techniques that dynamically operate all or part of the chip at reduced power, such as dynamic voltage scaling or clock gating, require experimental evaluation of the rapid transient heating and thermal diffusion from locally heated FUBs. System level power reduction strategies are generally recognized by the ITRS 2003 as necessary for the continual advancement of electronic systems at a rate consistent with "Moore's law."

"The high-performance market sector has experienced a dramatic increase in power over the different generations.... In addition to managing total chip power requirements in excess of 100 Watts, solutions to manage power density and internal hot spots are necessary." ITRS 2003

"Achieving the necessary reliability: New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key." 2003 ITRS: one of the five "Difficult Interconnect Challenges through 2009

"Integration of new processes and structures, including interconnects for emerging devices: Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects." Novel/active devices may be incorporated into the interconnect. 2003 ITRS: one of the five "Difficult Interconnect Challenges beyond 2009

The maximum junction temperatures for chip operation are shown in tables 93 a and b of the ITRS Assembly and Packaging section. Issues concerning the poor thermal conductivity of low- κ dielectrics is discussed on page 34 of the Reliability section.

TECHNICAL STRATEGY

1. Our established program in infrared (IR) (thermal) microscopy and our developing techniques in scanning thermal microscopy, utilizing

the AFM (atomic force microscope), have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as "How high are the temperatures in this MCM (multichip module) during service" to as challenging as "What is the interfacial thermal resistance of an alloy/intermetallic interface." The first was answered using the IR microscope; the second has yet to be answered.

We have just completed our fourth year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability, and have engendered great interest from the Advanced Embedded Passive Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute increase in interfacial thermal conductivity is the first indication of the microcracks and fissures that ultimately may result in failure.

DELIVERABLES: Scanning Probe Microscope (SPM) thermal measurement of aluminum interconnect lines. 2Q 2005 Publication of thermal and electrical measurements. 4Q 2005

2. As the size of packages gets smaller, heat removal becomes a more significant problem. The SPM is being used to develop a technique to measure thermal conductivity of thin films for application to metal interconnect lines. The technique also will be able to measure interfacial thermal resistance between coatings and substrates. The theoretical work on this development is being done in collaboration with Dr. Kevin Cole of the University of Nebraska.

DELIVERABLES: Report via the literature, on measurements of a model film, such as gold or different substrates. 3Q 2005

3. Carbon nanotubes have potential in heat-removal applications and in wear applications. Thermal properties show great promise in this area, if production issues can be addressed. We are currently measuring carbon nanotubes made from different inexpensive processes to determine if heat removal applications are economically and technologically feasible.

DELIVERABLES: Measure interfacial thermal resistance of carbon nanotube-covered copper and baseline copper materials. 2Q 2005

4. Interfacial thermal resistance measurement of the interface between solders and intermetallics supplies a piece to the puzzle of thermal dissipation from high-density packages. The small size of current and future solder bump processes requires higher spatial resolution thermal measurement methodologies.

DELIVERABLES: Measure interfacial thermal resistance of interfaces in in-house and industrial solder alloys. 4Q 2005

5. High speed temperature sensitive parameter (TSP) measurements are required for in-situ evaluation of the heat transport through the interface of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and DBC isolation attach degradation after thermal cycling and thermal shock stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design

DELIVERABLE: Perform thermal cycling and thermal shock stress on DARPA Wide-Bandgap High Power Electronics program devices and American Competitiveness Institute ManTech devices. Use unique NIST high speed, high current TSP system to evaluate die attach and DBC attach integrity before and after thermal stress. 4Q 2006

6. A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high speed transient measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1 μ s time resolution and 15 μ m spatial resolution. The new system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions and enables the measurement of transient heating events such as burst operation of IC FUBs and enables the measurement of transient current constriction failure events in RF and high power devices.

DELIVERABLE: Apply high speed thermal imaging system to characterize localized dynamic heating of FUBs in advanced digital integrated circuits. 2Q 2006

ACCOMPLISHMENTS

■ Completed analysis of measurements on industrial specimens from AEPT using thermal SPM, laser-heated IR microscopy, and Joule-heated IR microscopy. Reported results at GOMACTech 2004 Conference.

■ Thermal measurements have continued on three similar embedded resistor specimens. One specimen each is being measured using laser-heated IR microscopy, Joule-heated IR microscopy, and thermal SPM. The results were analyzed and the techniques compared. All three specimens have been thermally cycled 18 times, and data analysis shows consistency between the techniques. Figure 1 shows relative thermal resistance data as a function of thermal cycling from Joule-heated measurements.

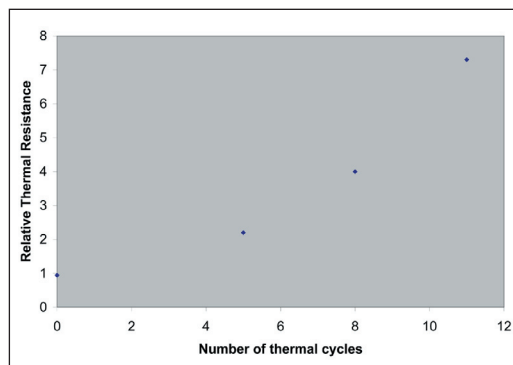


Figure 1. Joule-heated IR microscopy measurements showing relative thermal resistance as a function of thermal cycling.

■ Development of a technique for measuring the thermal conductivity of thin films using the SPM has begun. Most films used in electronics and electronic packaging are so thin that a measurement using even the thermal SPM would be primarily a measurement of the substrate material. With collaboration from Dr. Kevin Cole of the University of Nebraska, work has begun on a theoretical treatment of the data to allow measurement of thin films and the interfacial thermal resistance between the film and substrate. One application for this technique is measurement of thermal properties of interconnect lines. Measurements have begun using a model system, consisting of gold films of various thickness evaporated onto glass substrates. Figure 2 (pg. 196) shows thermal measurement data on films of differing thickness.

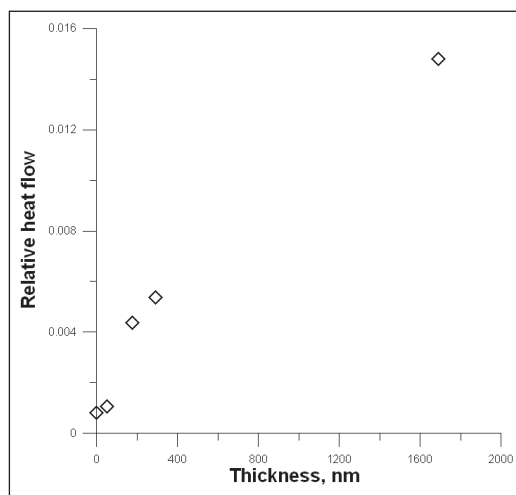


Figure 2. Thermal measurement data on thin gold films on glass substrates.

■ We have been approached by Cenymmer Corporation to make thermal and other measurements on a diamond-like carbon coating that they manufacture. Since these coatings are typically around a micron thick, the thermal SPM is a good tool for this measurement. Cenymmer also is interested in interface materials to allow adhesion of diamond-like carbon coatings to various substrates. This work fits well with our thin-film research, providing specimens with different, controlled interfaces to help solve the problem of analyzing thermal data on thin films and even thinner adhesion layers. Figure 3 shows a measurement result from one of their coatings.

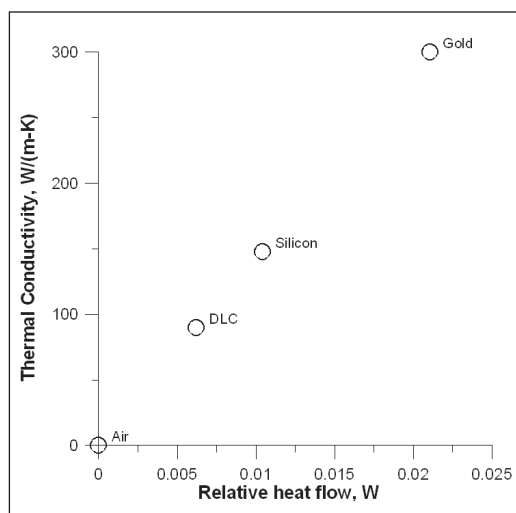


Figure 3. Thermal conductivity measurement of a 1.9 μm thick DLC coating and the comparative measurements of known materials using the same setup.

■ Completed the development of the high speed transient thermal imaging system. The acquisition and data analysis capabilities of this system have been extended to include a burst method and to allow frames from different transient movies to be compared more readily. All functions have been tested and verified.

■ Sequences of thermal images were taken at stages of progressive degradation on SiC diodes, starting with virgin diodes and progressing with the same diodes showing degraded electrical performance. The results show that the current is relatively uniform before degradation and that only 1 % of the chip is conducting all of the current after degradation.

■ We have developed a method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS} , at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter. Under these circumstances, variations in V_{GS} result from equal changes in the threshold voltage. The method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). Under the measurement conditions used, there are concerns about the sharing of current between the chips in the package, but by taking these into account, excellent agreement is obtained between the measured and simulated temperatures (Fig. 4). The module is shown in Fig. 5a and 5b.

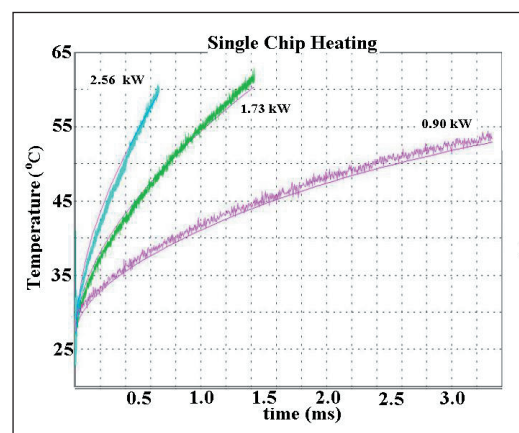


Figure 4. Electrically measured and computer simulated measurement of the temperature of IGBT chip in a power module.

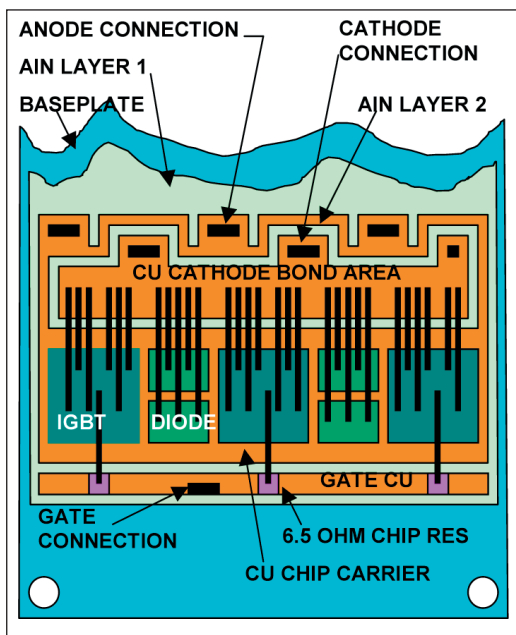


Figure 5a. Drawing of the layout of the IGBT chips within the module.

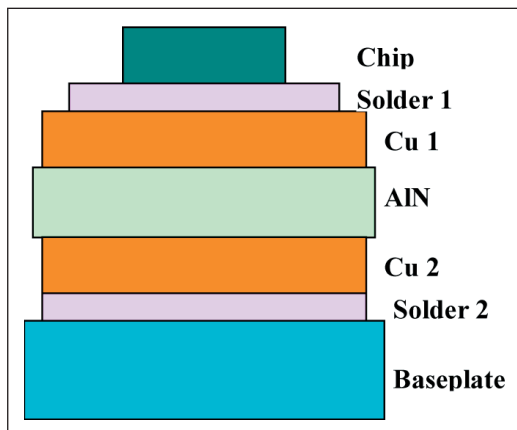


Figure 5b. Drawing of the vertical structure in the power module from one of the chips at the top to the baseplate at the bottom.

- Applied the new high-speed heating response measurement and modeling method to commercial high power IGBT half bridge module, commercial six-pack IGBT module, and prototype NSF Center for Power Electronic Systems Module. Electro-thermal simulations of a full three-phase inverter have been successfully performed, and a paper was completed and will appear at the IEEE Power Electronics Specialist Conference in June 2005.

- An invited presentation, "Semiconductor Device Temperature Measurements," was presented at the 20th IEEE Semiconductor Thermal Measurement and Management Symposium

(SemiTherm) in March 2004. The talk covered the basic physical phenomena of a wide variety of temperature-sensitive devices and material parameters that have been used for measuring chip-level temperatures. The temperature, spatial, and temporal resolutions of each of the three generic measurement types (electrical, optical, and contacting) were emphasized. Power dissipation and excessive temperature have been identified as barriers to the continued shrinking and performance improvements for CMOS and beyond technologies. Perhaps the major issues with temperature measurements for advanced semiconductor chips and novel electronic structures are spatial and temporal resolution. Scanning thermal probes have been shown to have a spatial resolution between 30–50 nm, but they have a relatively slow time response and measurement interpretation is difficult due to the complexity of the physical contact between the probe and the specimen. Optical methods, such as thermoreflectance and Raman spectroscopy, potentially have picosecond time resolution, but they are diffraction limited in their spatial resolution typically to about 1 μm typically. There continues to be much interest in the development of methods for measuring chip temperatures with improved spatial and time resolution.

- Feasibility has been shown of measurements of electronic interconnect lines using the thermal SPM. We are now calibrating the response of the probe tip to temperature.

COLLABORATIONS

AEPT Consortium

DuPont: John Felten

MacDermid: Dennis Fritz

Merix: Bob Greenlee

MicroFab: Virang Shah

SAS Circuits: Richard Snogren, Matt Snogren

Colorado School of Mines: Ivar Reimanis, Saki Krishnamurthy, John Berger

University of Nebraska: Kevin Cole

Cenymex Corporation: Scott Joray

University of Maryland: Bruce Jacob

University of Maryland CALCE Electronic Products and Systems Center: Patrick McCluskey

American Competitiveness Institute (ACI), Navy ManTech center: Barry Thaler

RECENT PUBLICATIONS

Slifka, A. J., Drexler, J. W., "Apparent Mobility of Interfaces in Integral Resistor Material," *Microscopy and Analysis*, pp.19-21 (January 2003).

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J. Rodriguez, Z. Parrilla, M. Veléz-Reyes, A. Hefner, D. Berning, J. Reichl, and J. Lai, "Thermal Component Models for Electro-Thermal Analysis of Multichip Power Modules," in *Conference Record IEEE Industry Applications Society Meeting*, pp. 234-241 (October 2002).

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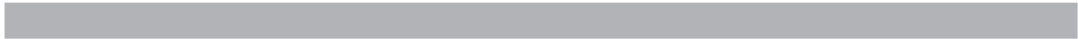
Ortiz-Rodríguez, J. M., Hefner, A. R., Vélez-Reyes, M., and Gonzalez, J., "Electro-Thermal Modeling of the IPEM Generation II in SABER," *CPES Annual Industry Seminar*, April 28-29, 2002.

J. Reichl, D. Berning, A. Hefner, and J-S. Lai, "Six-Pack IGBT Dynamic Electro-Thermal Model; Parameter Extraction and Validation," *IEEE Applied Power Electronics Conference*, Anaheim, CA (Feb. 2004).

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MANUFACTURING SUPPORT PROGRAM

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with International SEMATECH to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the “engineering chain.”



FACTORY TIME SYNCHRONIZATION STANDARDS

DEVELOPMENT FOR E-MANUFACTURING

GOALS

The project's objective is to educate the industry about the requirements, related issues, potential solutions, and standards recommendations to achieve reliable clock synchronization and time stamping capabilities for supporting present and future e-Manufacturing needs.

CUSTOMER NEEDS

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Manufacturing of 300 mm semiconductors will require data to be collected and analyzed from a rising confluence of data streams, due to additional sources previously thought to have little impact on manufacturing. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

One of the projected near term Factory Integration difficult challenges in the International Technology Roadmap for Semiconductors (ITRS) is the:

"Explosive growth of data collection/analysis requirements driven by process and modeling need ..." 2004 ITRS Update, Factory Integration, p. 2.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely manner requires a common, efficient method of merging the data.

The completion of the suite of Equipment Data Acquisition standards promises to create a data explosion. With data collection rates increas-

ing to 10,000 data points per second, one millisecond time stamp accuracy will be required. An inaccurate time stamp potentially renders the data invalid for many data mining and other analysis applications, yet there continues to be a wide variation in time stamping accuracies among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

TECHNICAL STRATEGY

Through collaborations with International SEMATECH Manufacturing Initiative (ISMI), this project will investigate and document key issues related to clock synchronization and time stamping internal to the equipment, where the greatest need for accurate time stamps are required. Current time stamp accuracy capabilities, issues preventing the dissemination of accurate timestamps and industry requirements are being gauged based on inputs from network engineers and information technology (IT) managers from chip manufacturers. Feedback from equipment suppliers also provides insight into current architectural issues preventing tools from providing accurate clock synchronization and time stamping. Software suppliers for process analysis tools will also be able to provide insight on current limitations due to inaccurate time stamps. A review of how other industries relying on process control data have addressed the clock synchronization and time stamping issue will also provide some guidelines of how the semiconductor industry can evolve to adopt an accurate time stamping mechanism.

DELIVERABLES: Document factory and equipment clock synchronization and time stamping recommendations based on semiconductor industry needs and lessons learned from other manufacturing industries. 3Q 2005

To achieve accurate timestamps, it is imperative to have a reliable and accurate clock synchronization methodology. The industry should understand how to obtain and distribute accurate time

Technical Contact:
Y. Li

throughout their factory networks. Network Time Protocol (NTP) and IEEE 1588 Precision Time Protocol (PTP) for industrial sensor networks are two of the key protocols for potential use in the semiconductor industry. A small network of NTP servers will be established to estimate its accuracy capabilities under different configurations to determine the effects of network and processor load on synchronization accuracy. Findings from the experiment will reveal some best methods for NTP use. The project will also continue to follow developments in PTP and participate in the IEEE 1588 User Requirements task force.

DELIVERABLES: Document current clock synchronization technologies by including a cookbook and best practices for NTP and a review of latest developments in IEEE 1588. 4Q 2005

Consistent time stamping formats must also be established, and the project will look at some of the widely used formats available such as ISO 8601. Semiconductor Equipment Materials International (SEMI) standards related to clock models and communication of synchronization and time stamping information will be reviewed to identify the standards to be modified or added to promote accurate clock synchronization among equipment subsystems and within the factory.

ACCOMPLISHMENTS

- A NIST internal report (NISTIR 7184) on “Semiconductor Factory and equipment Clock Synchronization for e-Manufacturing” was published in December 2004.
- The presentation on “*Running Out of Time: Improvements Required in Current Semiconductor and Equipment Clock Synchronization for Supporting Future Real-Time Data Collection*” was given at AEC/APC Symposium in September 2004.
- An educational presentation was given on time synchronization issues and potential solutions at the SEMI International Equipment Engineering Task Force at SEMICON West in July 2004.

COLLABORATIONS

Harvey Wohlwend, Brad Van Eck, Gino Crispieri, International SEMATECH Manufacturing Initiative

ENGINEERING CHAIN MANAGEMENT IN THE SEMICONDUCTOR INDUSTRY

GOALS

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor “Engineering Chain” which provides each partner with the data needed to make business decisions in a timely manner.

CUSTOMER NEEDS

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry’s hopes to reduce time, inventory, and therefore costs.

“It is expected that improvements in manufacturing productivity will play an even greater future role in reducing time to money and getting the most out of factory investment.” 2004 International Technology Roadmap for Semiconductors Factory Integration (ITRS) Overview Update, p.52.

The transition to 300 mm fabs and single-wafer lots has challenged the semiconductor industry in nearly every aspect of production, such as: facility layout; the mix of R&D within a single fab; data analysis of small lots; tool to tool interconnect; automated material handling and tracking of product, non-product wafers and reticles; the division of the production process across a partnership of foundries, designers, production sites, distributors and equipment manufacturers. Chip manufacturers require greater visibility of end product demand to accurately schedule their factories, and require greater technical collaboration with designers, OEMs, and foundries to ensure the manufacturability of the product being designed today using the generation of equipment that will be installed once production starts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2003 ITRS, p. 1.

According to the 2001 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. Intellectual Property (IP) reuse helps companies get complex systems to market quickly by eliminating redundant design effort. Standard formats for IP specifications and tool interfaces for the design of a System-on-a-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

Other information-exchange gaps in design houses include standard data formats for timing and power to expedite timing closure, reduce design iterations, and promote interoperability among best-of-breed software tools.

The industry trend towards outsourcing is leading towards silos of expertise, exactly when technology advances require a multi-disciplinary approach to problem solving. The production process is being conducted across fabs – not only at the traditional point of packaging and test, but mid-stream in the IC fabrication process. As the wafers change hands, so must the information about that wafer which accumulated during its production life cycle.

TECHNICAL STRATEGY

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST’s neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Contribute to the update of the Factory Integration component of the ITRS by co-leading the Engineering Chain Management subteam.
4Q 2005

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current

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areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: Establish a working agreement with ISMT in order to identify top industry IT-standards related needs and develop potential solutions to the current challenges based on cross-industry solutions facing similar issues. 3Q 2005

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Provide technical assistance to facilitate current IT standards development efforts within the semiconductor industry by participating in ISMT and SEMI standards activities. 4Q 2005

ACCOMPLISHMENTS

- Created a tutorial on how to improve the semiconductor standards development process through the use of XML and UML. This tutorial

has been taught as a class at both NIST and various SEMI standards workshops.

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.

- NIST has been co-leading the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Initial efforts are being made to determine the scope and identify the challenges of creating an effective Engineering Chain.

- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

COLLABORATIONS

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

International SEMATECH (ISMT)

NIST/SEMATECH e-HANDBOOK OF STATISTICAL METHODS

GOALS

The goal of the *NIST/SEMATECH e-Handbook of Statistical Methods* project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the *e-Handbook* readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

CUSTOMER NEEDS

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

TECHNICAL STRATEGY

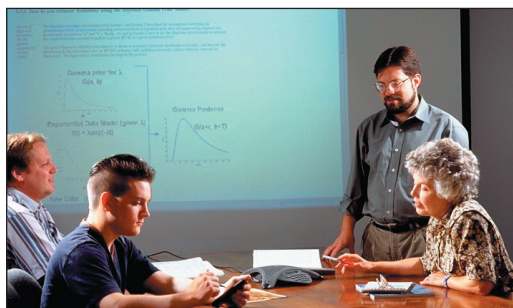
NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES: Update and maintain the e-Handbook on-line, and continue to distribute the e-Handbook on CD for off-line use. 4Q 2005

ACCOMPLISHMENTS

Since release of the final version, work has focused on publicizing the *e-Handbook*, responding to user feedback, and developing a compact disk version for off-line use. The web version of the e-Handbook averages approximately 1 million hits per month and over 6,000 e-Handbook compact disks have been distributed to industrial, government, and academic users all over the world over the last two years. Publicity on the e-Handbook has appeared in *Science*, *Quality*

Digest, *MicroMagazine.com*, *States News Service*, *National Science Digital Library Report for Math, Engineering, and Technology*, and *American Statistician*.



NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

COLLABORATIONS

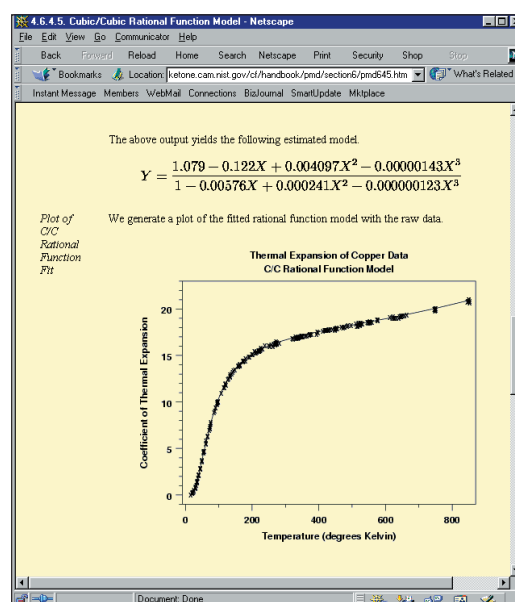
International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

RECENT PUBLICATIONS

NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, <http://www.nist.gov/stat.handbook/>.



Page from a case study in the process modeling chapter of the Handbook.

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"I reviewed the e-Handbook on the net and I am very impressed with the content, organization and consolidation of the statistical methods."

Jack Lewis
Microchip Technology Inc.

ABBREVIATIONS AND ACRONYMS

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mesures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CPU	Central Processing Unit
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing

DUV	deep ultraviolet
EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectroscopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling

NGL	next generation lithography
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-a-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM®	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope

TFTC	thin-film thermocouple
TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy

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